1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
F		480829	PRODUCTION RELEASED	01/10/07	?

PAGE	CONTENTS
1	TITLE PAGE AND CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	POWER BLOCK DIAGRAM
4	PCB NOTES AND HOLES
5	MPC7447A MAXBUS INTERFACE
6	MPC7447A DATA/NC PINS/BOOTBANGER
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE/BOOTROM
10	DDR MEMORY MUXES
11	400PIN STACKED DDR SODIMM CONNECTOR
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS/1.5V LDO
16	INTREPID DECOUPLING
17	USB 2.0 INTERFACE (uPD720101)
18	CARDBUS INTERFACE (PCI1510)
19	M11 AGP INTERFACE & SPREAD SPECTRUM
20	EXTERNAL TMDS (DUAL TMDS - SIL178)
21	M11 LVDS/TMDS/GPIO & GPU VCORE
22	M11 POWER

PAGE	CONTENTS
23	VIDEO CONNECTORS - INVERTER,DVI, LVDS,S-VIDEO
24	SPIDEY,PWR BUTTON,ALS
25	MMM & BATTERY CURRENT SENSE CIRCUIT
26	INTERNAL CONNECTORS-AIRPORT,HDD,ODD
27	FAN CONTROLLER,SW MODEM,SERIAL DEBUG SOUND/LEFT USB/BLUETOOTH
28	GIGABIT ETHERNET INTERFACE
29	FIREWIRE PHY
30	FIREWIRE PORTS
31	PMU
32	BATTERY CHARGER AND CONNECTOR
33	PBUS SUPPLY,PMU SUPPLY,SUPERCAP ,BACKUP BATTERY
34	3.3V/5V SYSTEM POWER SUPPLY
35	CPU CORE VOLTAGE POWER SUPPLY
36	1.5V/1.8V/2.5V SYS. POWER SUPPLIES
37	SIGNAL CONSTRAINTS(PG1)-DDR MEM/CLK
38	SIGNAL CONSTRAINTS(PG2)-CPU
39	SIGNAL CONSTRAINTS(PG3)-DIGITAL/DIFF
40	SIGNAL CONSTRAINTS(PG4)-POWER NETS
41	FUNCTIONAL TESTPOINTS
42	REVISION HISTORY
43-46	SCHEMATIC CREF AND NETLIST REPORTS

SCHEM,MLB,PB15"
08/25/2005

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
NO_SSCG	SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
SOFT_MODEM	USB_MODEM
GPU_PWRMSR	EMI
GPU_SS	EXT_TMDS (BETTER/BEST)
VGA_BUFFER_RES	INT_TMDS (BEST128)
MMM	SUPERCAP
INT_TMDS (BETTER/BEST)	ADT7460
EXT_TMDS (BEST128)	
BACKUP_BATT	
ADT7467	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6680	1	SCHEM,MLB,PB15	SCH1	
820-1679	1	PCBF,MLB,PB15	PCB1	
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:U3Z	LABEL_BST128
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:U40	LABEL_BST64
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:U41	LABEL_BTR

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB15

DRAWING NUMBER 051-6680 REV. F

SHT 1 OF 46

U51 INTREPID

J23 Ethernet Connector P.28
4 DATA PAIRS
U43 Ethernet PHY P.28
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ

J24 FW - A Connector P.30
2 DATA PAIRS @ 200MHZ
J20 FW - B Connector P.30
2 DATA PAIRS @ 400MHZ
U36 FireWire PHY P.29
1394 OHCI
3.3V
8BIT TX/RX
50MHZ

J15 SW MODEM Connector P.27
J3 LIO/Audio Connector P.27
J2 RUX Board Connector P.24
J19 ALS BOARD Connector P.24
J16 BACKUP BATTERY CONNECTOR P.33
C692 SUPERCAP P.33
J26 Battery Connector P.32
Power Supply & Charger P.32-36
J27 DC-In Connector P.32
J13 ODD Connector P.26
J12 HDD Connector P.26
UIDE
EIDE
NOT USED
I2S
I2C
I2C
U53/J1/J18 Fan Circuit P.27
J8 SLEEP LED P.24
SMBUS
3.3V
U28 PMU P.31
SERIAL
5V
J5 CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V

U15/U20/U58 MMM P.25
U41 BATTERY CURRENT SENSOR P.25

ETHERNET 10/100/1000 P.13	FIREWIRE 400 MB/S P.13	UATA 100 P.13	EIDE P.13	CARDSLOT P.13	I2S P.14	I2C P.13 P.14

NOT USED USB PORT A P.14
NOT USED USB PORT B P.14
NOT USED USB PORT C P.14
NOT USED USB PORT D P.14
USB PORT E P.14
USB PORT F P.14
MAXBUS P.8

SCCA P.14
VIA/PMU P.14
BOOTROM P.12
PCI 64BITS 33MHZ P.12
4X AGP P.12

J28 Serial Debug Connector P.27
U11 BOOT ROM 1M X 8 P.9
J6 AIRPORT Connector P.26
U8 TI PCI1510 CardBus Controller P.18
PCI BUS
32BITS
33MHZ
3.3V

J3 BlueTooth (LIO) P.27
J10 SPIDEY P.24

AGP BUS
1.5V/3.3V
32BITS
66MHZ
U47 ATI M11 64MB P.19-22
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)
U17 NEC USB2.0 EHCI HC P.17
J3 LEFT USB (VIA LIO) P.27
J17 RIGHT USB (VIA STATLER) P.27

MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA
DDR MEMORY P.9
MEMORY BUS
2.5V
167MHZ
64BITS
U16/U18/U28/U27
2:1 DDR MUXES P.10
J4 Inverter Connector P.23
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS (VIA SIL1162)
RGB
DDC
J14 LCD Panel Connector P.23
J21 S-Video Connector P.23
J22 DVI-I Connector P.23

U56 APOLLO CPU (MPC7447) P.5-6
CPU PLL Config P.7
PMU
J25 DDR SDRAM DIMM 0
DDR SDRAM DIMM 1 SO-DIMM Connector P.11

SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6680 | REV. F
SCALE NONE | SHT 2 OF 46

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 32

INRUSH LIMITER PG 32

+24V_PBUS

1V20_REF - PG 33

>~13.44V TURNS-ON

<~13.44V SHUTS-OFF

RUN/SS

BUCK VCC REGULATOR (LTC1625) PG 33

AC: 12.8V

NO AC: BATTERY VOLTAGE 1625 NOT RUNNING

SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS

RC AT 1M*0.047UF @ 24V

STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

14V_PBUS

+3V_PMU LDO PG 33

+5V_MAIN

+3V_PMU

+4_6V_BU

+BATT

RUN/SS - 5V

TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 34

VCC STBYMD PGOOD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V

RUN/SS - 3V

+5V_MAIN

3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

RC AT 1M*0.1UF @ 24V

STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

BACKUP BATTERY

14V_PBUS

14V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 33

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

BATTERY CHARGER (MAX1772) PG 32

+BATT

3S 2P 18650 CELLS

DC/DC (LTC3411)

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

PG 36

+1.8V_MAIN

MAXBUS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 32

+PBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC MAIN 2.5V/1.5V DC/DC (MAX1715) PG 36

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

PGOOD

TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR CORE
MAP31 DDR I/O
DDR POWER

+2.5V_MAIN

1_5V_2_5V_OK

+1.5V_MAIN

INTREPID CORE
AGP I/O

DCDC_EN_L

AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+PBUS

+5V_MAIN

EXT_VCC

VCC DC/DC (LTC1778)

SHUTDOWN: STOPPED
SLEEP: D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V INTERNAL 1.2UA CURRENT SOURCE

RUN/SS PG 20

GPU_VCORE +1.2V

DCDC_EN

SLEEP

D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK

D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON

HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS

DCDC_EN

SLEEP

MAXBUS SEQUENCING

+5V_MAIN

VCC SHDN DC/DC (MAX1717)

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

PG 35

CPU_VCORE (+1.385V)

SHUT-DOWN RUN SLEEP RUN SHUT-DOWN

SLEEP
SLEEP_L_LS5
DCDC_EN
DCDC_EN_L
+5V_MAIN ~2.23MS
+5V_SLEEP
+3V_MAIN ~7.36MS
+3V_SLEEP
3V_5V_OK 2.4V - ??? MS
+2_5V_MAIN ??? MS
+2_5V_SLEEP
+1_5V_MAIN ??? MS
+1_5V_SLEEP
1_5V_2_5V_OK (MAX1715 OUTPUT)
1_5V_2_5V_OK (AT LTC1778 RUN/SS)
GPU_VCORE (D3HOT) ~8.2MS
GPU_VCORE (D3COLD)

POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F

SCALE	SHT	OF
NONE	3	46

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA

1		SIGNAL (1/2 OZ + COPPER PLATING)
2	PREPREG (3 MIL)	SIGNAL (1/2 OZ)
3	PREPREG (3 MIL)	GROUND (1/2 OZ)
4	CORE (3 MIL)	SIGNAL (1/2 OZ)
5	PREPREG (5 MIL)	CUT POWER PLANE (1 OZ)
6	CORE (5 MIL)	CUT POWER PLANE (1 OZ)
7	PREPREG (5 MIL)	SIGNAL (1/2 OZ)
8	CORE (3 MIL)	GROUND (1/2 OZ)
9	PREPREG (3 MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3 MIL)	SIGNAL (1/2 OZ + COPPER PLATING)

BOARD HOLES

CHASSIS MOUNTS

ASICS HEATSINK MOUNTS
ZT7 HOLE-VIA-20R10 LEFT CPU
ZT21 HOLE-VIA-20R10 UPPER RT GPU
ZT58 HOLE-VIA-20R10 LWR CPU
ZT59 HOLE-VIA-20R10 LWR RT GPU

I/O AREA
ZT85 HOLE-VIA-20R10 DVI (CHGND2)
ZT86 HOLE-VIA-20R10 DVI 1394 (CHGND1)
ZT16 HOLE-VIA-20R10 BATT. CHRGR (CHGND5)

INVERTER
SH1 QG-583040 SHLD-SM (CHGND3)

MECH. HOLES
ZT74 HOLE-VIA-20R10
ZT36 HOLE-VIA-20R10 ZT301 SPN NO_TEST=TRUE
ZT23 HOLE-VIA-20R10 ZT302 SPN NO_TEST=TRUE
ZT42 HOLE-VIA-20R10 ZT10 SPN NO_TEST=TRUE

GROUND VIAS

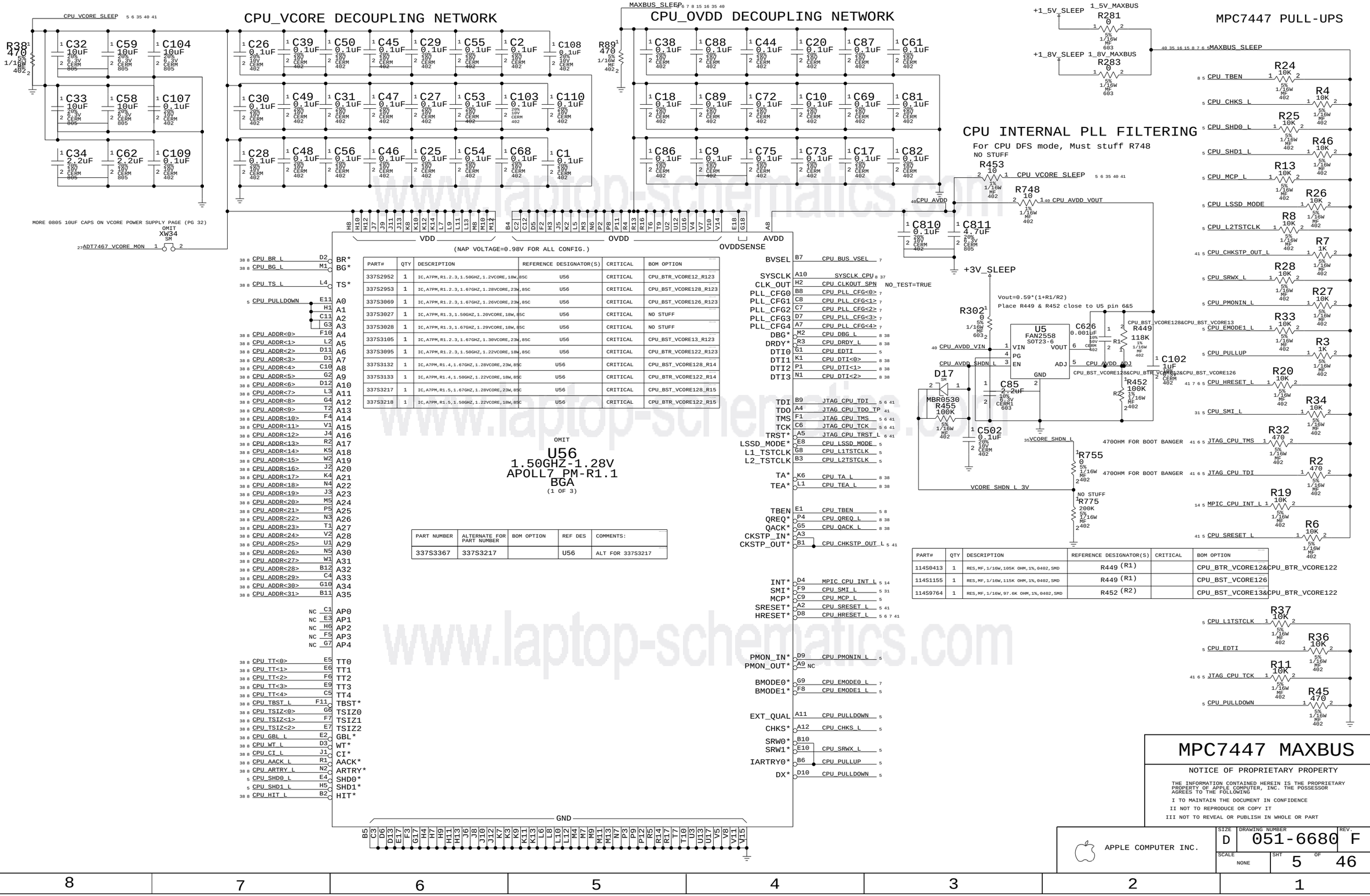
ZT76 ZT28 ZT72 ZT69 ZT68 ZT64 ZT61 ZT38 ZT39 ZT40 ZT41 ZT46 ZT71 ZT78 ZT80
ZT50 ZT51 ZT52 ZT53 ZT57 ZT60 ZT82 ZT22 ZT17 ZT35 ZT45 ZT79 ZT81 ZT83 ZT49
ZT48 ZT47 ZT54 ZT55 ZT56 ZT84 ZT5 ZT15 ZT44 ZT4 ZT8 ZT6 ZT32 ZT3 ZT10
ZT11 ZT34 ZT20 ZT43 ZT70 ZT2 ZT9 ZT75 ZT73 ZT63 ZT77 ZT66 ZT62 ZT65 ZT13
ZT25 ZT19 ZT24 ZT67 ZT37 ZT29 ZT31 ZT1 ZT14 ZT12 ZT27 ZT26 ZT30 ZT33 ZT18

All: HOLE-VIA-20R10

BOARD INFORMATION

APPLE COMPUTER INC.

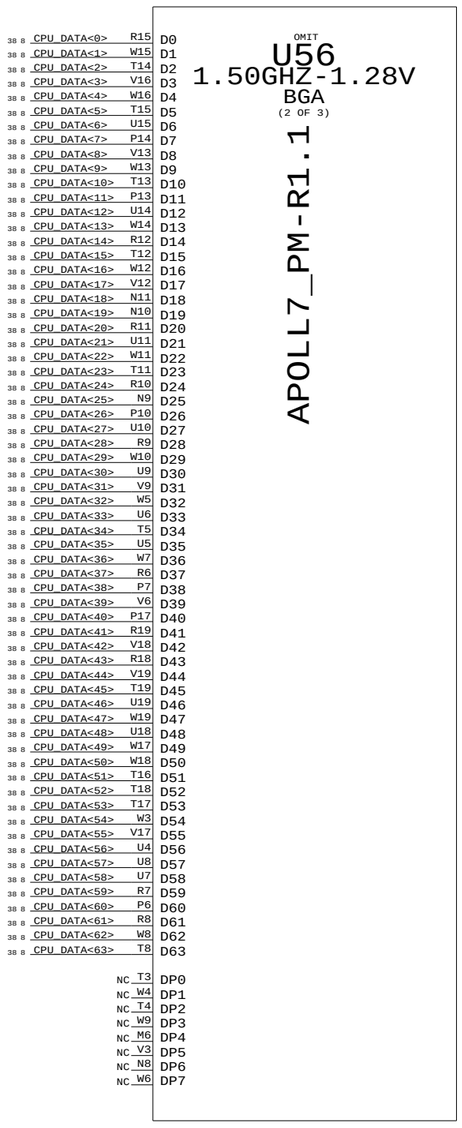
SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 4 OF 46	

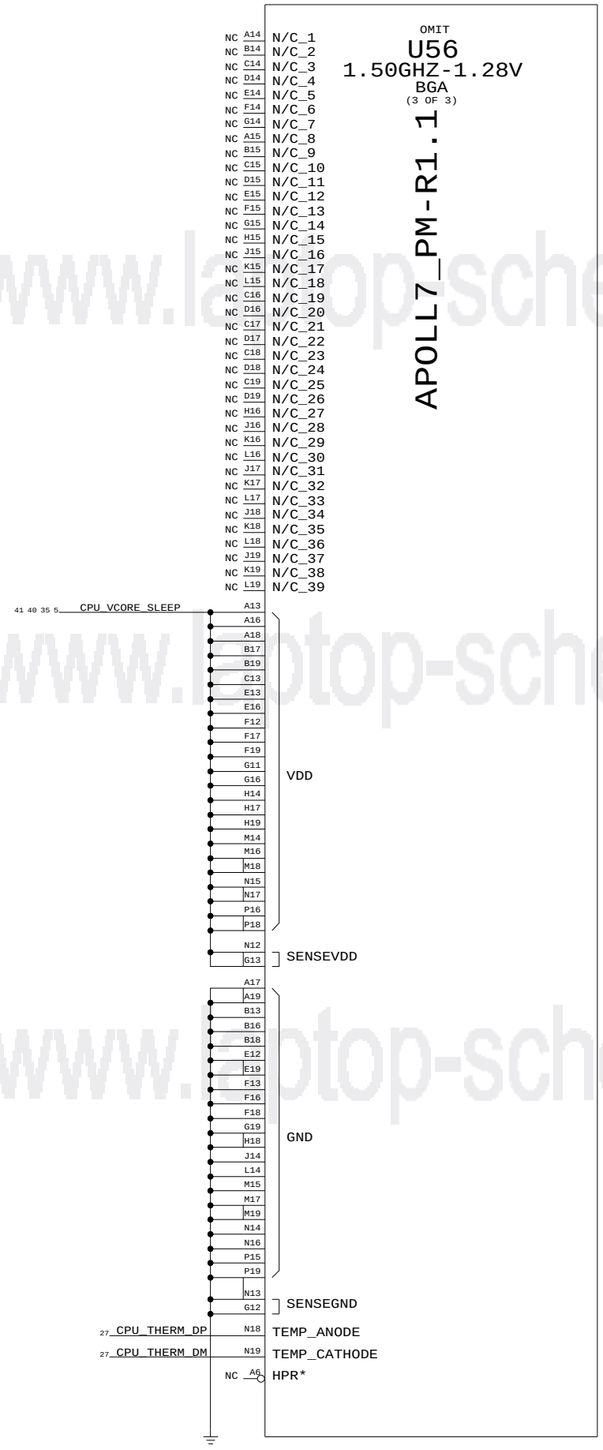


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2952	1	IC,A7PM,R1.2.3,1.50GHZ,1.2VCORE,18W,85C	U56	CRITICAL	CPU_BTR_VCORE12_R123
337S2953	1	IC,A7PM,R1.2.3,1.67GHZ,1.28VCORE,23W,85C	U56	CRITICAL	CPU_BST_VCORE128_R123
337S3069	1	IC,A7PM,R1.2.3,1.67GHZ,1.26VCORE,23W,85C	U56	CRITICAL	CPU_BST_VCORE126_R123
337S3027	1	IC,A7PM,R1.3,1.50GHZ,1.20VCORE,18W,85C	U56	CRITICAL	NO STUFF
337S3028	1	IC,A7PM,R1.3,1.67GHZ,1.29VCORE,18W,85C	U56	CRITICAL	NO STUFF
337S3105	1	IC,A7PM,R1.2.3,1.67GHZ,1.30VCORE,23W,85C	U56	CRITICAL	CPU_BST_VCORE13_R123
337S3095	1	IC,A7PM,R1.2.3,1.50GHZ,1.22VCORE,18W,85C	U56	CRITICAL	CPU_BTR_VCORE122_R123
337S3132	1	IC,A7PM,R1.4,1.67GHZ,1.28VCORE,23W,85C	U56	CRITICAL	CPU_BST_VCORE128_R14
337S3133	1	IC,A7PM,R1.4,1.50GHZ,1.22VCORE,18W,85C	U56	CRITICAL	CPU_BTR_VCORE122_R14
337S3217	1	IC,A7PM,R1.5,1.67GHZ,1.28VCORE,23W,85C	U56	CRITICAL	CPU_BST_VCORE128_R15
337S3218	1	IC,A7PM,R1.5,1.50GHZ,1.22VCORE,18W,85C	U56	CRITICAL	CPU_BTR_VCORE122_R15

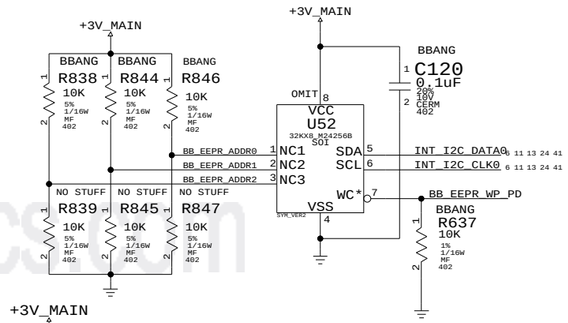
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3367	337S3217		U56	ALT FOR 337S3217

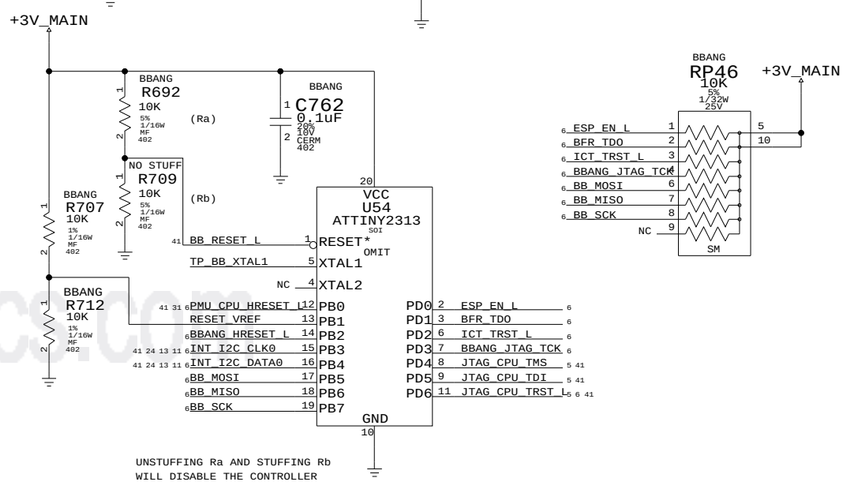
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0413	1	RES,MF,1/16W,105K OHM,1%,0402,SMD	R449 (R1)		CPU_BTR_VCORE128&CPU_BTR_VCORE122
114S1155	1	RES,MF,1/16W,115K OHM,1%,0402,SMD	R449 (R1)		CPU_BST_VCORE126
114S9764	1	RES,MF,1/16W,97.6K OHM,1%,0402,SMD	R452 (R2)		CPU_BST_VCORE13&CPU_BTR_VCORE122



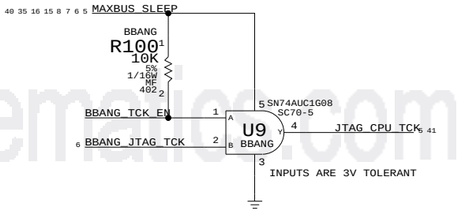


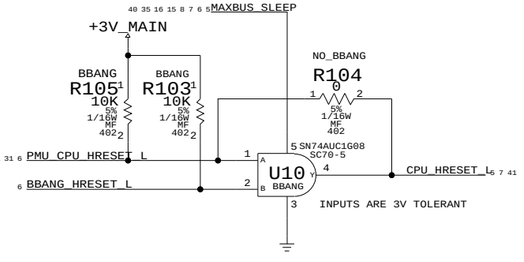
BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON

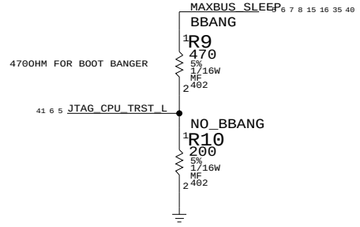




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1660	1	MCU,PROGRAMMED W/ BBANGER	U54	BBANG
341S1661	1	I2C EEPROM,PROGRAMMED W/ BBANGER	U52	BBANG







MPC7447/BBANG

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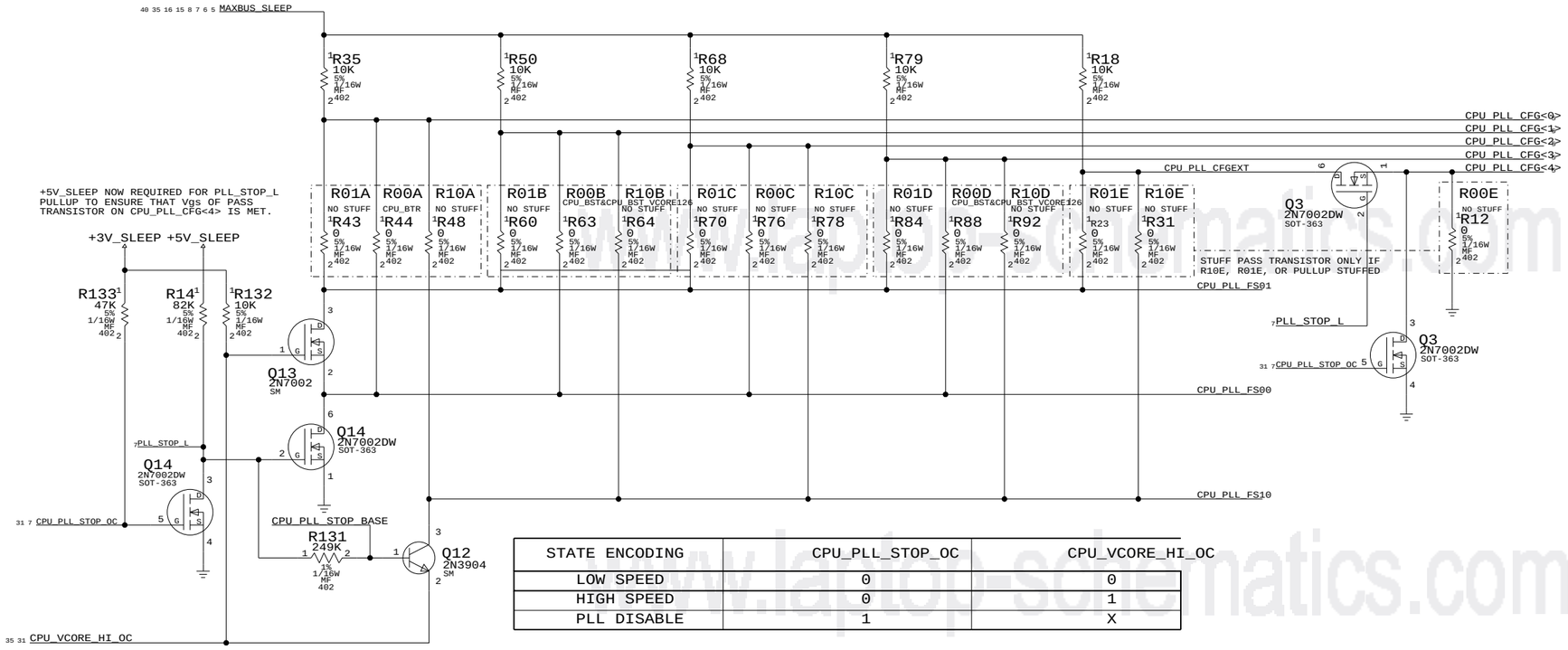
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 6 OF 46	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

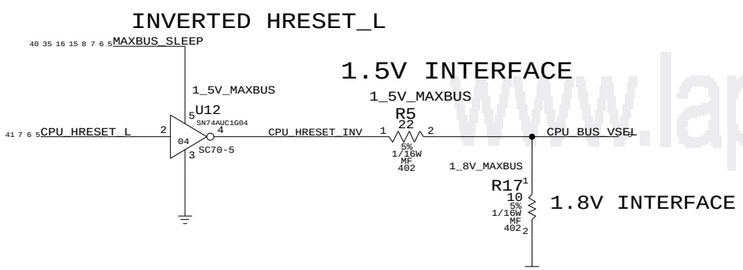
CPU FREQUENCY CONFIGURATION

APOLLO 7PM

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

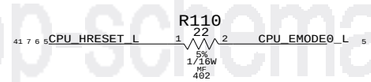
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 7 OF 46	

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

R640 10K NO STUFF — CPU_DATA<32>
R639 10K NO STUFF — CPU_DATA<33>
R638 10K NO STUFF — CPU_DATA<34>
R666 10K — CPU_DATA<35>
R622 10K — CPU_DATA<36>
R619 10K — CPU_DATA<37>
R618 10K — CPU_DATA<38>
R653 10K NO STUFF — CPU_DATA<39>
R621 10K — Spare
R620 10K — Spare
R652 10K — Spare
R650 10K — Spare

1: DDR_TRDMODE_Enable
0: HDI output

DDR_IPGEN Pol
1: Active High
0: Active low

AnalyzerClk_En_h
1: Active

Ext PLL Spread Pol
1: Active low
0: Active high

BIT 40 TO 47

MAXBUS_SLEEP

R641 10K NO STUFF — CPU_DATA<40>
R665 10K SSCG — CPU_DATA<41>
R664 10K NO STUFF — CPU_DATA<42>
R693 10K NO_SSCG — CPU_DATA<43>
R694 10K NO STUFF — CPU_DATA<44>
R699 10K NO STUFF — CPU_DATA<45>
R648 10K — CPU_DATA<46>
R677 10K — CPU_DATA<47>
R623 10K — Spare
R651 10K NO_SSCG — Spare
R649 10K — BIT2
R678 10K SSCG — BIT1
R679 10K — BIT0
R684 10K — Spare

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

1: Enable Alternate PLL4 (SW CNTL ONLY)
0: Disable Alternate PLL4

PLL4 Source (Clock Spread)
1: PLL4
0: PLL4 Source (no spread)

PLL4 Source (Clock Spread)
1: PLL4
0: PLL4 Source (no spread)

BIT 48 TO 55

MAXBUS_SLEEP

R696 10K SSCG — CPU_DATA<48>
R695 10K SSCG — CPU_DATA<49>
R667 10K — CPU_DATA<50>
R668 10K NO STUFF — CPU_DATA<51>
R643 10K NO STUFF — CPU_DATA<52>
R642 10K NO STUFF — CPU_DATA<53>
R698 10K — CPU_DATA<54>
R681 10K NO_SSCG — CPU_DATA<55>
R680 10K NO_SSCG — Spare
R654 10K NO STUFF — Spare
R655 10K — Spare
R625 10K — Spare
R624 10K — Spare
R683 10K NO STUFF — Spare
R626 10K — Spare

BUF_REF CLK OUTEnable_h
1: Enable
0: Disable

PLL4ExtSrc
0: PLL4
1: external source

OBSOLETE (Should remain high)
0: BootROM on IDE/CardSlot
1: BootROM on PCI1

1: 100ohm workaround
0: 50ohm
HI PHY workaround

BIT2 BIT1 BIT0

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R159 4.7 5% 1/16W MF 402 — +1_5V_INTREPID_PLL → +1_5V_INTREPID_PLL7

C187 0.22uF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6)

OMIT
U51
INTREPID-REV2.1
BGA

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER
CPU_ADDR<0>	D24	A_0	
CPU_ADDR<1>	D25	A_1	
CPU_ADDR<2>	A27	A_2	
CPU_ADDR<3>	E24	A_3	
CPU_ADDR<4>	G23	A_4	
CPU_ADDR<5>	B26	A_5	
CPU_ADDR<6>	A26	A_6	
CPU_ADDR<7>	D23	A_7	
CPU_ADDR<8>	A25	A_8	
CPU_ADDR<9>	E23	A_9	
CPU_ADDR<10>	J22	A_10	
CPU_ADDR<11>	B25	A_11	
CPU_ADDR<12>	H22	A_12	
CPU_ADDR<13>	G22	A_13	
CPU_ADDR<14>	D22	A_14	
CPU_ADDR<15>	B24	A_15	
CPU_ADDR<16>	B23	A_16	
CPU_ADDR<17>	E22	A_17	
CPU_ADDR<18>	J21	A_18	
CPU_ADDR<19>	G21	A_19	
CPU_ADDR<20>	E21	A_20	
CPU_ADDR<21>	A24	A_21	
CPU_ADDR<22>	D21	A_22	
CPU_ADDR<23>	A23	A_23	
CPU_ADDR<24>	H20	A_24	
CPU_ADDR<25>	B22	A_25	
CPU_ADDR<26>	H21	A_26	
CPU_ADDR<27>	A22	A_27	
CPU_ADDR<28>	E20	A_28	
CPU_ADDR<29>	B21	A_29	
CPU_ADDR<30>	D20	A_30	
CPU_ADDR<31>	A21	A_31	
CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	

(1 OF 9) CRITCAL

MAXBUS INTERFACE

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - PU
SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - PU
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU

R169 511 1% 1/16W MF 402
R168 0 5% 1/16W MF 402 — SYSCLK_CPU → SYSCLK_CPU_UF
R161 1K 1% 1/16W MF 402

INTREPID OUTPUTS HIGH BY DEFAULT

VSSA_7 (PLL6) H25

DRDY	G28	CPU_DRDY_L	5 38
DTI_0	K25	CPU_DTI<0>	5 38
DTI_1	D29	CPU_DTI<1>	5 38
DTI_2	B30	CPU_DTI<2>	5 38
TA	E27	CPU_TA_L	5 38
TEA	E28	CPU_TEA_L	5 38
DBG	A30	CPU_DBG_L	5 38

D_0	D10	CPU_DATA<0>	6 38
D_1	G12	CPU_DATA<1>	6 38
D_2	E11	CPU_DATA<2>	6 38
D_3	H11	CPU_DATA<3>	6 38
D_4	B9	CPU_DATA<4>	6 38
D_5	B8	CPU_DATA<5>	6 38
D_6	A9	CPU_DATA<6>	6 38
D_7	A8	CPU_DATA<7>	6 38
D_8	E12	CPU_DATA<8>	6 38
D_9	D11	CPU_DATA<9>	6 38
D_10	B10	CPU_DATA<10>	6 38
D_11	J13	CPU_DATA<11>	6 38
D_12	A10	CPU_DATA<12>	6 38
D_13	D12	CPU_DATA<13>	6 38
D_14	E13	CPU_DATA<14>	6 38
D_15	G13	CPU_DATA<15>	6 38
D_16	B11	CPU_DATA<16>	6 38
D_17	D13	CPU_DATA<17>	6 38
D_18	A11	CPU_DATA<18>	6 38
D_19	G14	CPU_DATA<19>	6 38
D_20	H14	CPU_DATA<20>	6 38
D_21	E14	CPU_DATA<21>	6 38
D_22	B12	CPU_DATA<22>	6 38
D_23	G15	CPU_DATA<23>	6 38
D_24	B13	CPU_DATA<24>	6 38
D_25	H15	CPU_DATA<25>	6 38
D_26	D14	CPU_DATA<26>	6 38
D_27	B14	CPU_DATA<27>	6 38
D_28	A12	CPU_DATA<28>	6 38
D_29	G16	CPU_DATA<29>	6 38
D_30	E15	CPU_DATA<30>	6 38
D_31	J16	CPU_DATA<31>	6 38
D_32	D15	CPU_DATA<32>	6 8 38
D_33	A14	CPU_DATA<33>	6 8 38
D_34	A13	CPU_DATA<34>	6 8 38
D_35	D16	CPU_DATA<35>	6 8 38
D_36	E16	CPU_DATA<36>	6 8 38
D_37	G17	CPU_DATA<37>	6 8 38
D_38	B15	CPU_DATA<38>	6 8 38
D_39	H17	CPU_DATA<39>	6 8 38
D_40	A15	CPU_DATA<40>	6 8 38
D_41	B16	CPU_DATA<41>	6 8 38
D_42	E17	CPU_DATA<42>	6 8 38
D_43	A16	CPU_DATA<43>	6 8 38
D_44	J18	CPU_DATA<44>	6 8 38
D_45	H18	CPU_DATA<45>	6 8 38
D_46	D17	CPU_DATA<46>	6 8 38
D_47	G18	CPU_DATA<47>	6 8 38
D_48	A17	CPU_DATA<48>	6 8 38
D_49	B17	CPU_DATA<49>	6 8 38
D_50	E18	CPU_DATA<50>	6 8 38
D_51	B18	CPU_DATA<51>	6 8 38
D_52	D18	CPU_DATA<52>	6 8 38
D_53	A18	CPU_DATA<53>	6 8 38
D_54	A19	CPU_DATA<54>	6 8 38
D_55	H19	CPU_DATA<55>	6 8 38
D_56	B19	CPU_DATA<56>	6 8 38
D_57	J19	CPU_DATA<57>	6 8 38
D_58	A20	CPU_DATA<58>	6 8 38
D_59	D19	CPU_DATA<59>	6 8 38
D_60	E19	CPU_DATA<60>	6 8 38
D_61	G19	CPU_DATA<61>	6 8 38
D_62	B20	CPU_DATA<62>	6 8 38
D_63	G20	CPU_DATA<63>	6 8 38

SHORT = 1" SHORTER THAN MATCHED LENGTH

R155 0 5% 1/16W MF 402 — INT_CPUFB_OUT → INT_CPUFB_OUT_SHORT
R140 0 5% 1/16W MF 402 — INT_CPUFB_OUT_NORM → INT_CPUFB_LONG
R146 0 5% 1/16W MF 402 — NO STUFF
R147 0 5% 1/16W MF 402 — INT_CPUFB_IN → INT_CPUFB_IN_NORM
R141 0 5% 1/16W MF 402 — NO STUFF
R128 0 5% 1/16W MF 402 — NO STUFF
R136 0 5% 1/16W MF 402

LONG = 1" LONGER THAN MATCHED LENGTH

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

MAXBUS PULL-UPS

MAXBUS_SLEEP

RP3 10K — CPU_TS_L (2, 7)
RP3 10K — CPU_TA_L (1, 8)
RP3 10K — CPU_ARTRY_L (4, 5)
RP2 10K — CPU_BR_L (1, 8)
R152 10K — CPU_HIT_L (1, 2)
RP2 10K — CPU_DRDY_L (3, 6)
RP2 10K — CPU_TEA_L (4, 5)
RP2 10K — CPU_AACK_L (2, 7)
R150 10K — CPU_DBG_L (1, 2)
RP3 10K — CPU_BG_L (3, 6)
R151 10K — CPU_QREQ_L (1, 2)

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

R669 10K NO STUFF — CPU_DATA<56>
R645 10K NO STUFF — CPU_DATA<57>
R697 10K NO STUFF — CPU_DATA<58>
R670 10K NO STUFF — CPU_DATA<59>
R644 10K NO STUFF — CPU_DATA<60>
R646 10K NO STUFF — CPU_DATA<61>
R656 10K — CPU_DATA<62>
R685 10K — CPU_DATA<63>
R657 10K — Spare
R628 10K — Spare
R682 10K — Spare
R658 10K — Spare
R627 10K NO STUFF — Spare
R629 10K — Spare

OBSOLETE
ROM Overlay R90
1: 0-1 IDE / 2-3 PCI1

PCI1_REQ2_L / PCI1_GNT2_L
1: REQ/GNT
0: GPIOs

PCI1_REQ1_L / PCI1_GNT1_L
1: REQ/GNT
0: GPIOs

PCI1_REQ0_L / PCI1_GNT0_L
1: REQ/GNT
0: GPIOs

Firewire PHY interface
1: B-mode interface

Processor Bus Mode
1: 64x bus (G4)
0: 60x bus (G3)

Intrepid MaxBus

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 8 OF 46	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

1MB BOOT ROM

U51 — OMIT — INTREPID-REV2.1 BGA (2 OF 9) CRITICAL

DDR_DATA_0	AK32	MEM_DATA<0>	H35	DDR_A_0
DDR_DATA_1	AK33	MEM_DATA<1>	G35	DDR_A_1
DDR_DATA_2	AK31	MEM_DATA<2>	G36	DDR_A_2
DDR_DATA_3	AK35	MEM_DATA<3>	F36	DDR_A_3
DDR_DATA_4	AK36	MEM_DATA<4>	F35	DDR_A_4
DDR_DATA_5	AJ32	MEM_DATA<5>	E35	DDR_A_5
DDR_DATA_6	AJ35	MEM_DATA<6>	E36	DDR_A_6
DDR_DATA_7	AJ36	MEM_DATA<7>	G32	DDR_A_7
DDR_DATA_8	AG33	MEM_DATA<8>	D36	DDR_A_8
DDR_DATA_9	AG35	MEM_DATA<9>	H36	DDR_A_9
DDR_DATA_10	AH35	MEM_DATA<10>	G33	DDR_A_10
DDR_DATA_11	AG36	MEM_DATA<11>	H33	DDR_A_11
DDR_DATA_12	AH36	MEM_DATA<12>	D35	DDR_A_12
DDR_DATA_13	AH32	MEM_DATA<13>	L30	DDR_BA_0
DDR_DATA_14	AG32	MEM_DATA<14>	M29	DDR_BA_1
DDR_DATA_15	AG31	MEM_DATA<15>		
DDR_DATA_16	AE32	MEM_DATA<16>	AN34	DDRCS_0
DDR_DATA_17	AF35	MEM_DATA<17>	AN36	DDRCS_1
DDR_DATA_18	AF36	MEM_DATA<18>	AL35	DDRCS_2
DDR_DATA_19	AE36	MEM_DATA<19>	AL33	DDRCS_3
DDR_DATA_20	AE35	MEM_DATA<20>		
DDR_DATA_21	AE33	MEM_DATA<21>	AJ31	DDR_DQS_0
DDR_DATA_22	AD36	MEM_DATA<22>	AH31	DDR_DQS_1
DDR_DATA_23	AD35	MEM_DATA<23>	AD32	DDR_DQS_2
DDR_DATA_24	AA36	MEM_DATA<24>	AB30	DDR_DQS_3
DDR_DATA_25	AA35	MEM_DATA<25>	V30	DDR_DQS_4
DDR_DATA_26	AA33	MEM_DATA<26>	P32	DDR_DQS_5
DDR_DATA_27	AB36	MEM_DATA<27>	N29	DDR_DQS_6
DDR_DATA_28	AB35	MEM_DATA<28>	L32	DDR_DQS_7
DDR_DATA_29	AC36	MEM_DATA<29>		
DDR_DATA_30	AA32	MEM_DATA<30>	AJ33	DDR_DM_0
DDR_DATA_31	AB33	MEM_DATA<31>	AH33	DDR_DM_1
DDR_DATA_32	V36	MEM_DATA<32>	AD33	DDR_DM_2
DDR_DATA_33	U33	MEM_DATA<33>	AC35	DDR_DM_3
DDR_DATA_34	U32	MEM_DATA<34>	T35	DDR_DM_4
DDR_DATA_35	V35	MEM_DATA<35>	T33	DDR_DM_5
DDR_DATA_36	T36	MEM_DATA<36>	N32	DDR_DM_6
DDR_DATA_37	U36	MEM_DATA<37>	L33	DDR_DM_7
DDR_DATA_38	U35	MEM_DATA<38>		
DDR_DATA_39	T36	MEM_DATA<39>	L29	DDRRAS
DDR_DATA_40	P33	MEM_DATA<40>	H32	DDRCAS
DDR_DATA_41	R36	MEM_DATA<41>	K30	DDRWE
DDR_DATA_42	P35	MEM_DATA<42>	AN35	DDRCKE0
DDR_DATA_43	P36	MEM_DATA<43>	AM35	DDRCKE1
DDR_DATA_44	R36	MEM_DATA<44>	AM36	DDRCKE2
DDR_DATA_45	R35	MEM_DATA<45>	AL36	DDRCKE3
DDR_DATA_46	R33	MEM_DATA<46>		
DDR_DATA_47	R32	MEM_DATA<47>	AB32	DDR_SELHI_0
DDR_DATA_48	N35	MEM_DATA<48>	AE29	DDR_SELHI_1
DDR_DATA_49	M36	MEM_DATA<49>	N30	DDR_SELLO_0
DDR_DATA_50	L35	MEM_DATA<50>	T32	DDR_SELLO_1
DDR_DATA_51	M35	MEM_DATA<51>		
DDR_DATA_52	M33	MEM_DATA<52>	Y32	DDR_MCLK_0_P
DDR_DATA_53	L36	MEM_DATA<53>	Y33	DDR_MCLK_0_N
DDR_DATA_54	N33	MEM_DATA<54>	Y35	DDR_MCLK_1_P
DDR_DATA_55	M30	MEM_DATA<55>	Y36	DDR_MCLK_1_N
DDR_DATA_56	J32	MEM_DATA<56>	Y30	DDR_MCLK_2_P
DDR_DATA_57	J33	MEM_DATA<57>	W30	DDR_MCLK_2_N
DDR_DATA_58	J35	MEM_DATA<58>	W32	DDR_MCLK_3_P
DDR_DATA_59	K32	MEM_DATA<59>	W33	DDR_MCLK_3_N
DDR_DATA_60	K33	MEM_DATA<60>	V33	DDR_MCLK_4_P
DDR_DATA_61	J36	MEM_DATA<61>	V32	DDR_MCLK_4_N
DDR_DATA_62	K36	MEM_DATA<62>	W35	DDR_MCLK_5_P
DDR_DATA_63	K35	MEM_DATA<63>	W36	DDR_MCLK_5_N
			AA22	DDR_REF
			Y22	DDR_VREF_0
			T22	DDR_VREF_1

DDR MEMORY INTERFACE

’0’ & ’1’ GO TO SLOT A
’2’ & ’3’ GO TO SLOT B

’0’ & ’1’ GO TO SLOT A
’2’ & ’3’ GO TO SLOT B

MEM_MUXSEL_MSB_L_TP
MEM_MUXSEL_MSB
MEM_MUXSEL_LSB_L_TP
MEM_MUXSEL_LSB

’0’S ARE SAME POLARITY (ACTIVE-LO)
’1’S ARE SAME POLARITY (ACTIVE-HI)

SYSCLK_DDRCLK_A0_UF
SYSCLK_DDRCLK_A0_L_UF
SYSCLK_DDRCLK_A1_UF
SYSCLK_DDRCLK_A1_L_UF
INT_DDRCLK2_P_TP
INT_DDRCLK2_N_TP
SYSCLK_DDRCLK_B0_UF
SYSCLK_DDRCLK_B0_L_UF
SYSCLK_DDRCLK_B1_UF
SYSCLK_DDRCLK_B1_L_UF
INT_DDRCLK5_P_TP
INT_DDRCLK5_N_TP

INT_MEM_REF_H
INT_MEM_VREF

R209 1K 1% 1/16W MF 402

MEM_VREF

+2.5V_INTREPID

R208 10K 1% 1/16W MF 402
R202 10K 1% 1/16W MF 402
C249 0.1uF 10% 10V CERM 402

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP20	4	5
SYSCLK_DDRCLK_A1_L_UF	RP20	6	7
SYSCLK_DDRCLK_A0_UF	RP22	1	8
SYSCLK_DDRCLK_A0_L_UF	RP22	7	6
SYSCLK_DDRCLK_B1_UF	RP20	2	7
SYSCLK_DDRCLK_B1_L_UF	RP20	8	1
SYSCLK_DDRCLK_B0_UF	RP22	3	6
SYSCLK_DDRCLK_B0_L_UF	RP22	5	4

CS

MEM_CS_L<0>	RP31	3	6
MEM_CS_L<1>	RP31	2	7
MEM_CS_L<2>	RP29	3	6
MEM_CS_L<3>	RP29	4	5

CKE

MEM_CKE<0>	RP31	1	8
MEM_CKE<1>	RP31	4	5
MEM_CKE<2>	RP29	1	8
MEM_CKE<3>	RP29	2	7

ADDR

MEM_ADDR<0>	RP14	3	6
MEM_ADDR<1>	RP12	2	7
MEM_ADDR<2>	RP12	1	8
MEM_ADDR<3>	RP12	4	5
MEM_ADDR<4>	RP12	3	6
MEM_ADDR<5>	RP9	2	7
MEM_ADDR<6>	RP9	1	8
MEM_ADDR<7>	RP14	2	7
MEM_ADDR<8>	RP9	4	5
MEM_ADDR<9>	RP14	4	5
MEM_ADDR<10>	RP14	1	8
MEM_ADDR<11>	RP17	4	5
MEM_ADDR<12>	RP9	3	6

BA

MEM_BA<0>	RP17	2	7
MEM_BA<1>	RP17	1	8

CNTL

MEM_WE_L	RP17	3	6
MEM_CAS_L	R162	1	2
MEM_RAS_L	R176	1	2

RAM_CS_L<0>	RP31	3	6
RAM_CS_L<1>	RP31	2	7
RAM_CS_L<2>	RP29	3	6
RAM_CS_L<3>	RP29	4	5
RAM_CKE<0>	RP31	1	8
RAM_CKE<1>	RP31	4	5
RAM_CKE<2>	RP29	1	8
RAM_CKE<3>	RP29	2	7
RAM_ADDR<0>	RP14	3	6
RAM_ADDR<1>	RP12	2	7
RAM_ADDR<2>	RP12	1	8
RAM_ADDR<3>	RP12	4	5
RAM_ADDR<4>	RP12	3	6
RAM_ADDR<5>	RP9	2	7
RAM_ADDR<6>	RP9	1	8
RAM_ADDR<7>	RP14	2	7
RAM_ADDR<8>	RP9	4	5
RAM_ADDR<9>	RP14	4	5
RAM_ADDR<10>	RP14	1	8
RAM_ADDR<11>	RP17	4	5
RAM_ADDR<12>	RP9	3	6
RAM_BA<0>	RP17	2	7
RAM_BA<1>	RP17	1	8
RAM_WE_L	RP17	3	6
RAM_CAS_L	R162	1	2
RAM_RAS_L	R176	1	2

+3V_MAIN

C125 2.2uF 10% 10V CERM 805
C773 0.1uF 10% 10V CERM 402
C122 0.1uF 10% 10V CERM 402

U11 — VPP OMIT VCC — 1MX8-3.3V TSOP

A0	21	DQ0	25
A1	20	DQ1	26
A2	19	DQ2	27
A3	18	DQ3	28
A4	17	DQ4	32
A5	16	DQ5	33
A6	15	DQ6	34
A7	14	DQ7	35
A8	8		
A9	7		
A10	36		
A11	6		
A12	5		
A13	4		
A14	3		
A15	2		
A16	1		
A17	40		
A18	13		
A19	37		
A20	38		
CE	22		
OE	24		
WE	9		
WP	12		
PWD	10		
GND	23, 39		

PCI_AD<0> … PCI_AD<31>

ROM_CS_TP_L
NO STUFF R236 0 5% 1/16W MF 402
R691 10K 5% 1/16W MF 402
R112 10K 5% 1/16W MF 402
ROM_CS_L
R674 1K 5% 1/16W MF 402
R1 0 NO STUFF
ROM_ONBOARD_CS_TP_L
R271 0 NO STUFF
ROM_OE_TP_L
R194 0 NO STUFF
ROM_RW_TP_L

ROM_ONBOARD_CS_L
ROM_OE_L
ROM_RW_L
ROM_WP_L
INT_RESET_L

OVERRIDE ROM MODULE INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1792	1	IC,BOOTROM,4.9.1F3,Q16B	U11	CRITICAL	?

Weak pulldowns ensure CKEs stay low after 2.5V I/O to Intrepid shuts off.

RAM_CKE<0>
RAM_CKE<1>
RAM_CKE<2>
RAM_CKE<3>

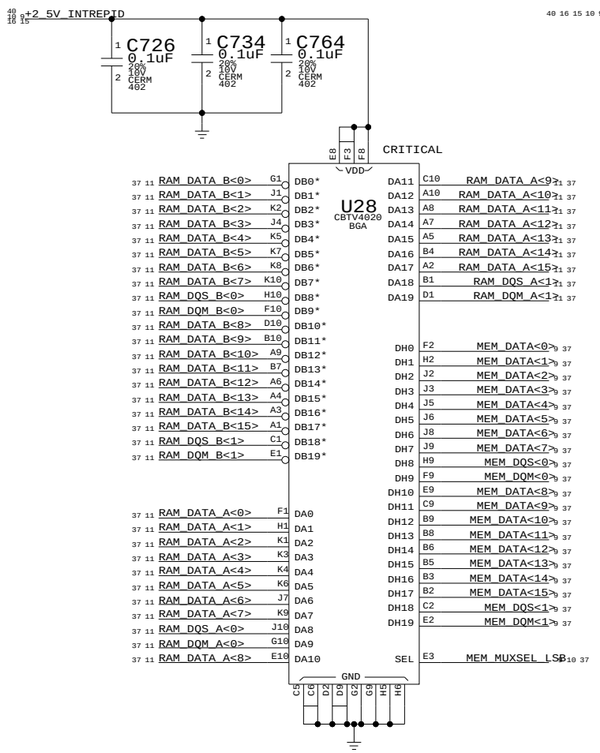
R247 10K 5% 1/16W MF 402 — INT_2_5V_COLD
R257 10K 5% 1/16W MF 402 — INT_2_5V_COLD
R260 10K 5% 1/16W MF 402 — INT_2_5V_COLD
R265 10K 5% 1/16W MF 402 — INT_2_5V_COLD

INT - DDR/BOOTROM

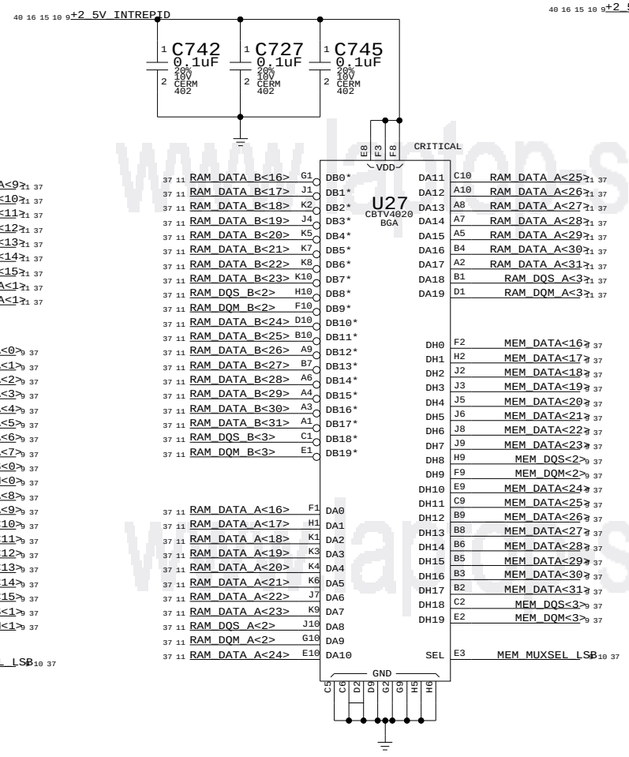
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 9 OF 46	

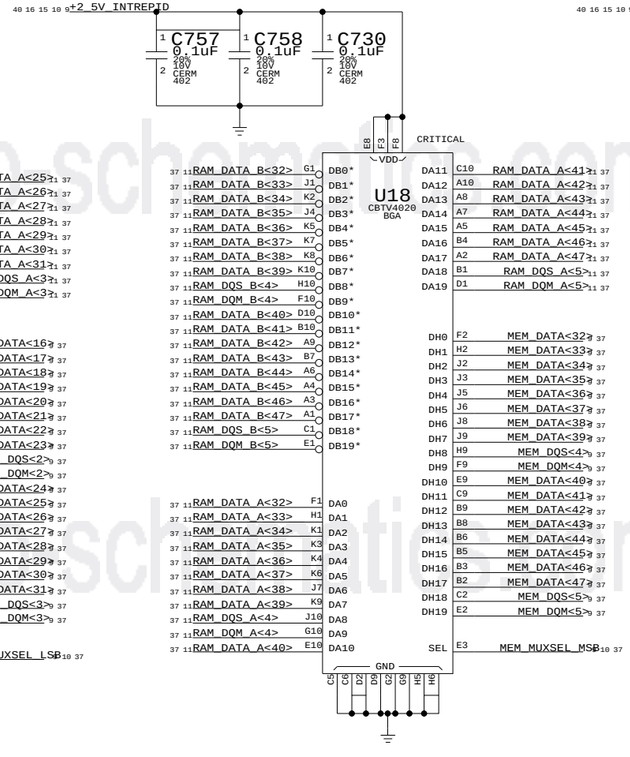
BIT 0..15



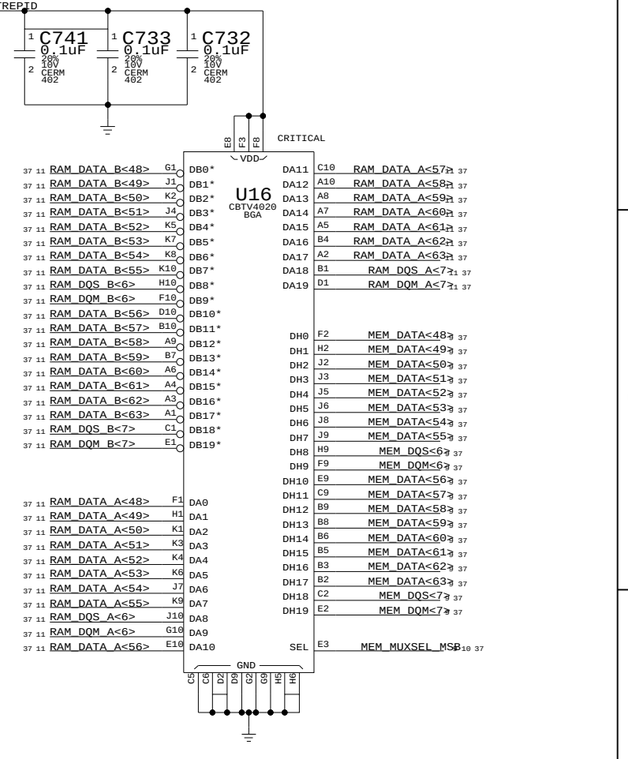
BIT 16..31



BIT 32..47



BIT 48..63



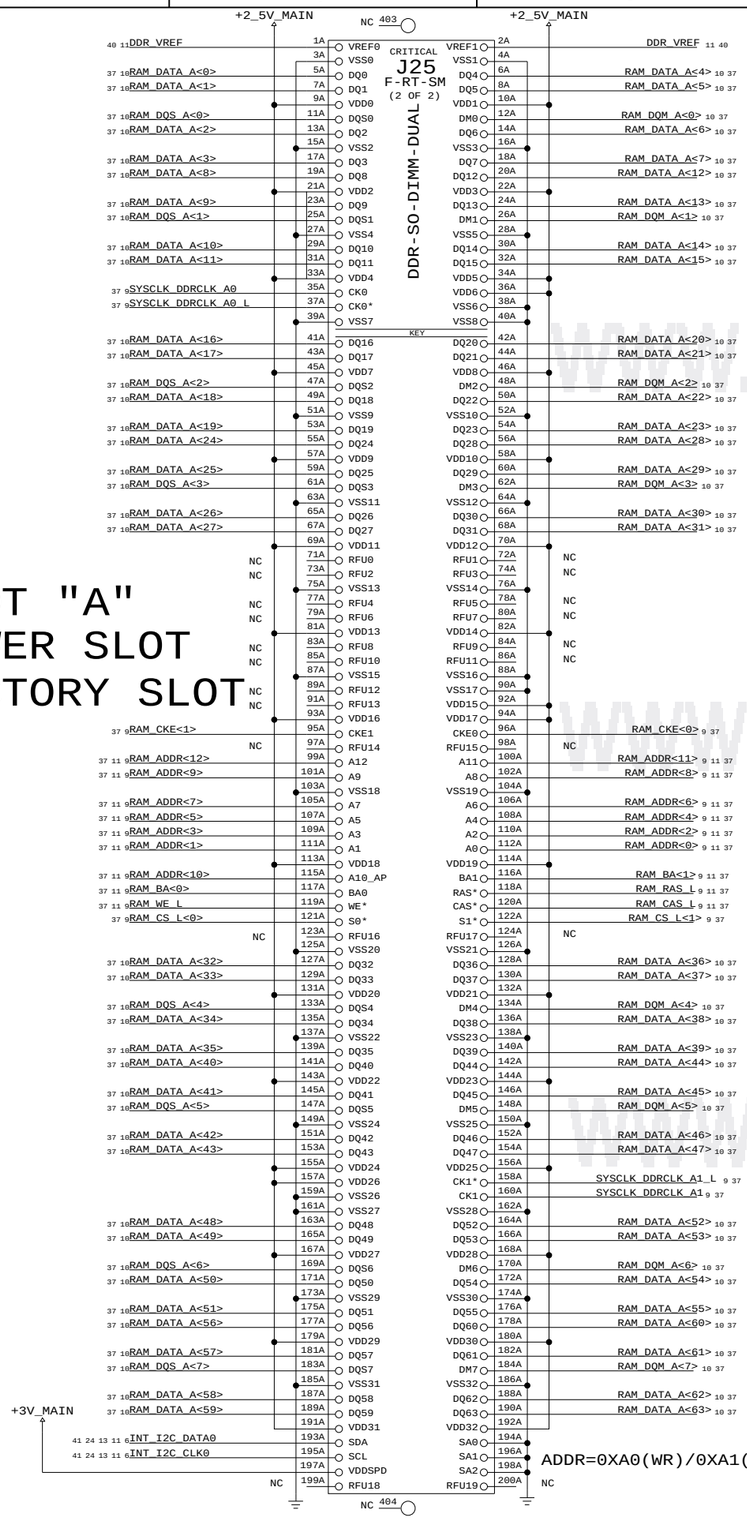
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F

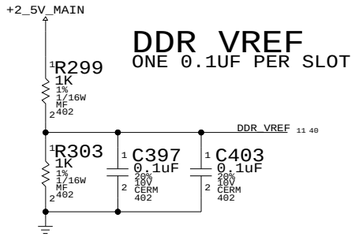
SCALE	SHT OF
NONE	10 46

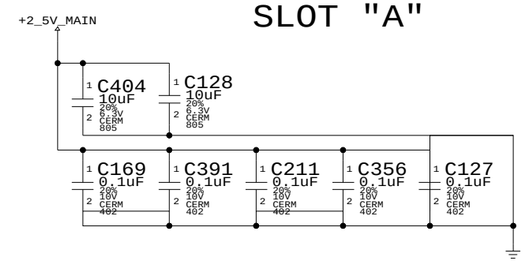


SLOT "A"
LOWER SLOT
FACTORY SLOT

SLOT "B"
UPPER SLOT
CUSTOMER SLOT

NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting

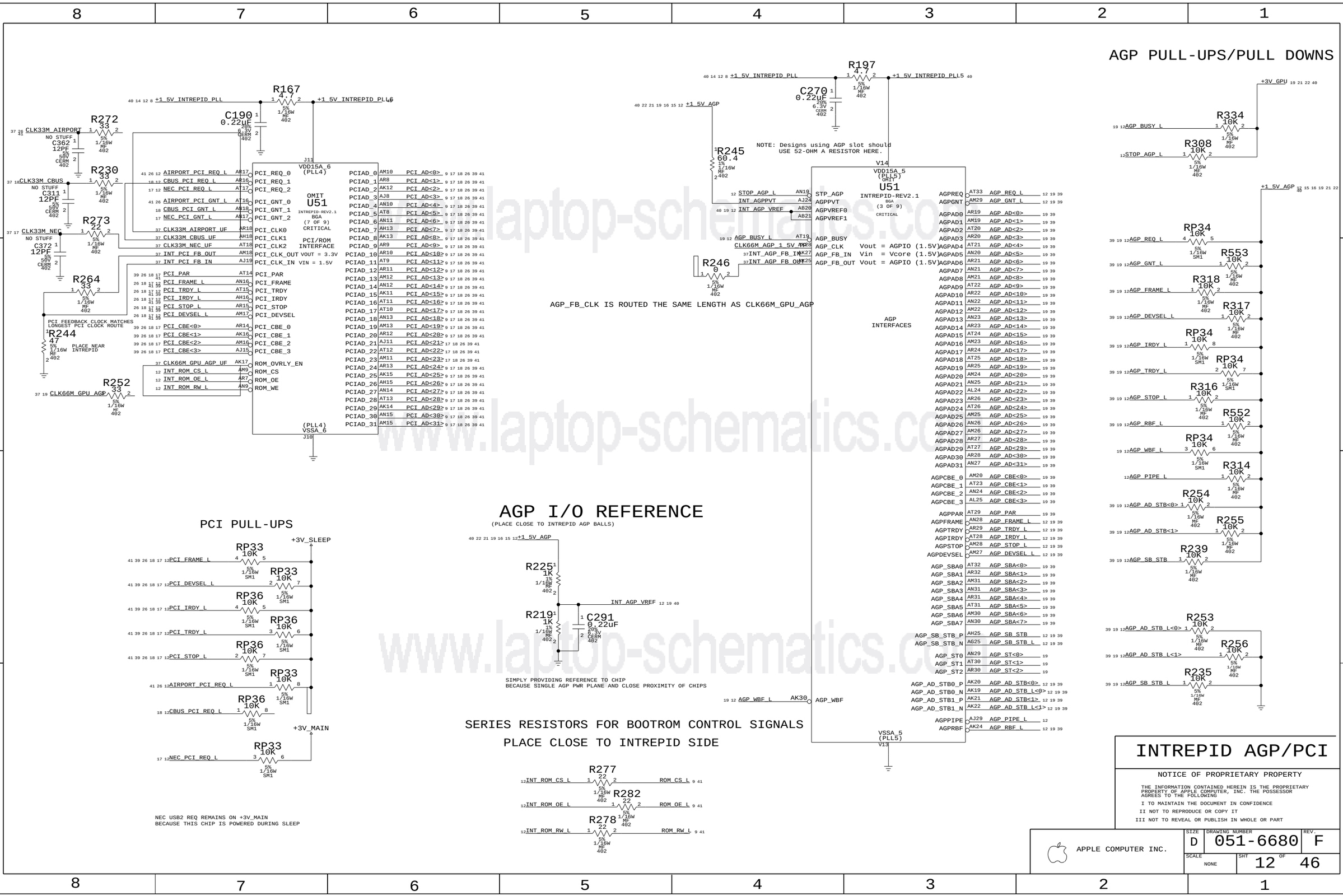




DDR SODIMM CONNS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 11 OF 46	


AGP PULL-UPS/PULL DOWNS
PCI PULL-UPS
AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)
SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS
PLACE CLOSE TO INTREPID SIDE
AGP_FB_CLK IS ROUTED THE SAME LENGTH AS CLK66M_GPU_AGP
NOTE: Designs using AGP slot should USE 52-OHM A RESISTOR HERE.
SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS
NEC USB2 REQ REMAINS ON +3V_MAIN
BECAUSE THIS CHIP IS POWERED DURING SLEEP
PCI_FEEDBACK_CLOCK_MATCHES LONGEST PCI CLOCK ROUTE
PLACE NEAR INTREPID
AGP INTERFACES
U51
INTREPID-REV2.1
BGA
(7 OF 9)
CRITICAL
PCI/ROM INTERFACE
VOUT = 3.3V
VIN = 1.5V
VDD15A_6 (PLL4)
OMIT
(PLL4) VSSA_6
VDD15A_5 (PLL5)
OMIT
VSSA_5 (PLL5)
AGP_BUSY
AGP_CLK
AGP_FB_IN
AGP_FB_OUT
Vout = AGPIO (1.5V)
Vin = Vcore (1.5V)
INTREPID AGP/PCI
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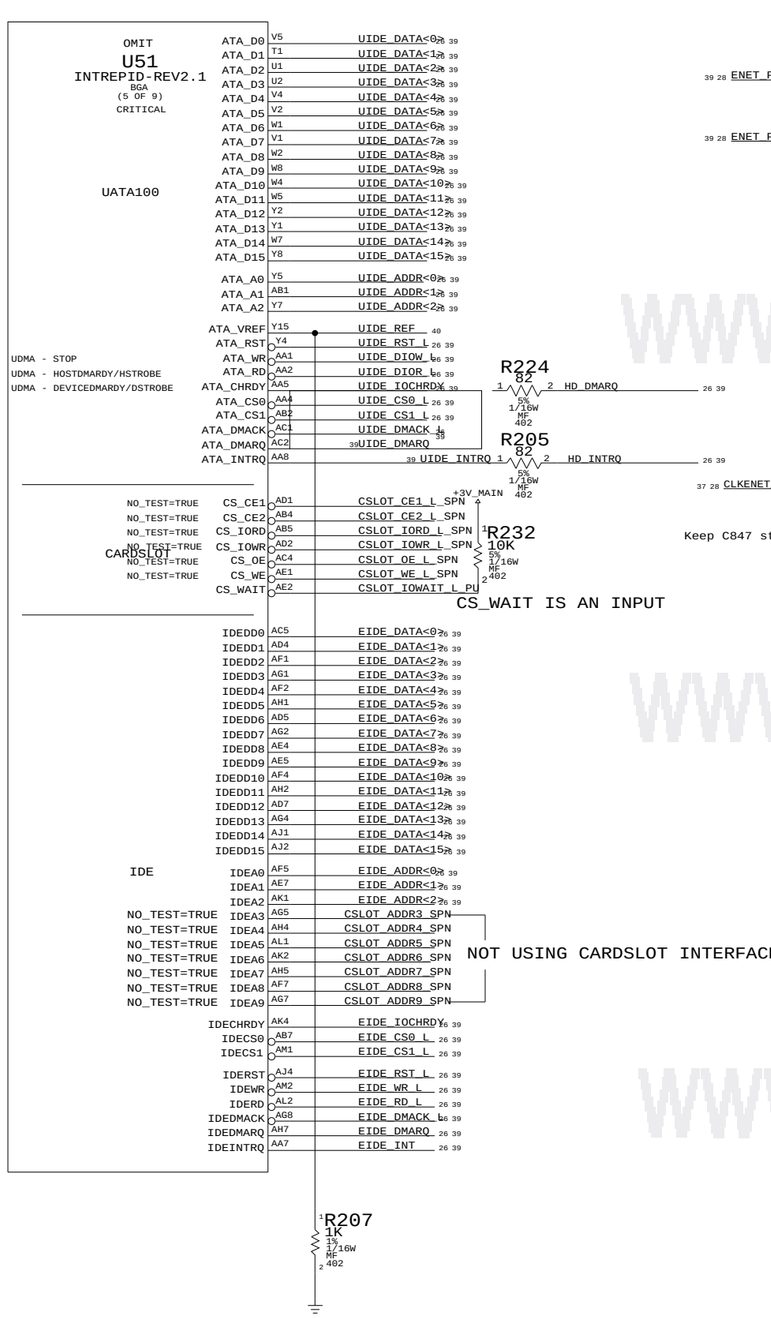
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6680
REV. F
SCALE NONE
SHT 12 OF 46



BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - LOWER J25 - PG 11	N/A	N/A	N/A
A2-WR A3-RD	RAM - UPPER J25 - PG 11	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	SOFT MODEM J14 - PG 26	N/A
AE-WR AF-RD	BOOTBANG EEPROM U51 - PG 6	N/A	N/A	N/A
84-WR 85-RD	LMU J3000 - PG 24 (LMU on RUX Brd.)	N/A	N/A	N/A
5C-WR 5D-RD	N/A	FAN CONTROLLER U52 - PG 26	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J2 - PG 26	N/A
D2-WR D3-RD	N/A	CLOCK SLEW SSCG U30 - PG 14	N/A	N/A
B0-WR B1-RD	N/A	MMM U15 - PG 42	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F

SCALE: NONE

SHT 13 OF 46

USB PORT ASSIGNMENTS

PORT A B C D/UNUSED

R181 10K — USB_DAM
R183 10K — USB_DAP
R123 10K — USB_DBP
R121 10K — USB_DBM
R164 10K — USB_DCM
R165 10K — USB_DCP
R182 10K — USB_DDM
R180 10K — USB_DDP

PORT E/BLUETOOTH

R174 22 — USB_DEP → BT_USB_DP
R179 22 — USB_DEM → BT_USB_DM
R178 15K, R175 15K

PORT F/TRACKPAD

R635 22 — USB_DFP → USB_TPAD_P
R603 22 — USB_DFM → USB_TPAD_N
R129 15K, R125 15K

PCI INTERRUPTS

+3V_SLEEP
R148 10K — CBUS_INT_L
+3V_MAIN
R746 10K — AIRPORT_PCI_INT_L
R158 10K — NEC_PCI_INT_L

GPIO/EXTINT PULLUPS

+3V_MAIN
R187 10K — USB_PWREN_EF_L
R191 10K — USB_OC_EF_L
RP11 10K — USB_OC_AB_L
RP11 10K — USB_PWREN_CD_L
RP8 10K — USB_PWREN_AB_L
RP11 10K — USB_OC_CD_L
RP8 10K — INT_EXTINT14_PU
RP5 10K — INT_EXTINT8_PU
RP6 10K — COMM_RING_DET_L
RP11 10K — INT_GPIO15_PU
RP6 10K — PMU_INT_NMI
RP6 10K — PMU_INT_L
R250 10K — PMU_REQ_L
RP7 10K — INT_GPIO12_PU
RP7 10K — INT_EXTINT13_PU
RP4 10K — INT_EXTINT16_PU
RP6 10K — INT_EXTINT10_PU
RP8 10K — INT_GPIO9_PU
RP8 10K — INT_GPIO1_PU
R153 10K — INT_EXTINT3_PU
RP15 10K — INT_MOD_DTO_UF
RP15 10K — INT_MOD_CLKOUT_UF
RP5 10K — NC EXTINT11
RP4 10K — NC EXTINT12
RP15 10K — INT_MOD_DTI
RP15 10K — INT_MOD_SYNC_UF
R206 10K — INT_MOD_BITCLK_UF
R166 100K — SND_HW_RESET_L

+2_5V_MAIN / +1_8V_MAIN

R568 0 (NO STUFF)
R565 0
→ LTC1962_INT_VIN

U49 LT1962-ADJ MSOP

IN, NC, NC, SHDN, OUT, ADJ, BYP, GND
LTC1962_INT_ADJ, LTC1962_INT_BYP
C721 1uF X5R 10V CERM 603
C392 0.01uF 20% 16V CERM 402
R574 18.7K 1% 1/16W MF 402
R567 68.1K 1% 1/16W MF 402
C723 10uF 20% 6.3V CERM 805
+1_5V_INTREPID_PLL → 1.55V OUTPUT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0086	1	IC,CY28512-2	U31	CRITICAL	SSCG

U31 CY28512D TSSOP (OMIT)

CRITICAL
INTERNAL 250K PULL-UP
OUTPUT IMPEDANCE ~18-20 OHMS
CLKIN, FSEL, SCLK, SDATA, ADDRSEL, RESET*, PD*, LOCK, ODSEL
VDD0, VDD1, VDDA, VDDC, VDDP
VSS0, VSS1, VSSA, VSSC, VSSQ
CG_FSEL, INT_I2C_CLK1, INT_I2C_DATA1, CG_ADDRSEL, CG_RESET_L, CG_SYSCLK_EN, CG_LOCK
INT_REF_CLK_OUT, CG_CLKOUT, INT_REF_CLK_IN

R287 10K, R288 10K, R295 10K, R284 0, R296 10K, R292 75, R293 33
PLACE NEAR INTREPID TO MINIMIZE OVERSHOOT
R142 0 — VCORE_VGATE

+3V_MAIN / +2_5V_MAIN

SSCG L15 400-OHM-EMI SM-1
SSCG L14 400-OHM-EMI SM-1
+3V_CG_PLL_MAIN
C400 0.1uF, C402 1uF, C399 0.1uF, C394 0.1uF
MAIN_RESET_L
R286 0 (NO STUFF)

R240 / C337 / R280 / C389 / R279 / C388 / R243 / C386 / R201 / C387

4.7 1/16W MF 402; 0.22uF 20% 6.3V CERM 402
→ +1_5V_INTREPID_PLL

+3V_MAIN

L13 FERR-EMI-100-OHM SM
+3V_INTREPID_USB
C235 0.01uF, C246 0.1uF, C256 10uF 20% 6.3V CERM 805

U51 INTREPID-REV2.1 BGA CRITICAL (6 OF 9) — OMIT

PCI VDD15A_1 (PLL1), PCI VDD15A_2 (PLL2), PCI VDD15A_3 (PLL3), PCI VDD15A_4 (PLL7), PCI VDD15A_8 (PLL9)
VDDU33_1, VDDU33_2

GENERAL PURPOSE I/O'S

GPIO0 (VCORE A/B SEL), GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO9, GPIO11, GPIO12, GPIO15, GPIO16

INTERRUPTS

EXTINT0, EXTINT1, EXTINT2, EXTINT3, EXTINT4, EXTINT5, EXTINT6, EXTINT7, EXTINT8, EXTINT9, EXTINT10, EXTINT11, EXTINT12, EXTINT13, EXTINT14, EXTINT15, EXTINT16, EXTINT17, CPU_INT
POWERBOOK SPARE: CBUS_REG_L, CBUS_IREQ_L
PCIPME, PROCSLEEPREQ, PENDPROCINT

CLOCKS

XTAL_IN, XTAL_OUT, STOPXTAL, WATCHDOG, BUF_REF_CLK_OUT, SS_REF_CLK_IN

IIC

IICCLK_2, IICDATA_2

USB

SCCTXDA, SCCRTSA, SCCDTRA, SCCRXDA, SCCGPIOA, SCCTRXCA
SCCTXDB, SCCRTSB, SCCRXDB, SCCGPIOB, SCCTRXCB
USB_VD0_P/N, USB_VD1_P/N, USB_VD2_P/N, USB_VD3_P/N, USB_PRTPWR0, USB_PWRFLT0, USB_PRTPWR1, USB_PWRFLT1, USB_VD4_P/N, USB_VD5_P/N, USB_PRTPWR2, USB_PWRFLT2

AUDIO/I2S

AUD_DTO, AUD_DTI, AUD_SYNC, AUD_BITCLK, AUD_CLKOUT
MOD_DTO, MOD_DTI, MOD_SYNC, MOD_BITCLK, MOD_CLKOUT
(SIGNAL FROM MODEM)

VSSA1 (PLL1), VSSA2 (PLL2), VSSA3 (PLL3), VSSA4 (PLL7), VSSA_8 (PLL9), VSSU_1, VSSU_2

SOFT_MODEM

RP13 47 — INT_I2S0_SND_TO_DAC
RP13 47 — INT_I2S0_SND_LRCLK
RP13 47 — INT_I2S0_SND_SCLK
RP13 47 — INT_I2S0_SND_MCLK
RP47 0K — INT_MOD_DTO
RP47 0K — INT_MOD_SYNC
RP47 0K — INT_MOD_BITCLK
RP47 0K — INT_MOD_CLKOUT

+3V_SLEEP
R258 1K, R241 1K
→ INT_I2C_CLK2, INT_I2C_DATA2

R450 / R218 / R467 / R457 / R134 / R144 / R143 / R113 / J9 U.FL-R-SMT

CG_FSEL_INT, INT_GPIO1_PU, COMM_RESET_L, FW_PHY_PD, SND_HP_MUTE_L, SND_AMP_MUTE_L, INT_GPIO9_PU, SND_HW_RESET_L, INT_GPIO12_PU, INT_GPIO15_PU, INT_ENET_RST_L, COMM_RING_DET_L, PMU_INT_L, AGP_ATI_INT_L, INT_EXTINT3_PU, SND_LIN_SENSE_L, ENET_ENERGY_DET, AIRPORT_PCI_INT_L, CBUS_INT_L, INT_EXTINT8_PU, PMU_INT_NMI, INT_EXTINT10_PU, MMM_FFIRQ_L, MMM_SIRQ_L, INT_EXTINT13_PU, INT_EXTINT14_PU, SND_HP_SENSE_L, INT_EXTINT16_PU, NEC_PCI_INT_L, MPIC_CPU_INT_L, PMU_PME_L, INT_PROC_SLEEP_REQ, INT_PEND_PROC_INT, CLK18M_INT_XIN, SYSTEM_CLK_EN, INT_WATCHDOG_L, INT_REF_CLK_OUT_UF, INT_REF_CLK_IN
SYSTEM_CLK_EN, INT_TDO, CG_SYSCLK_EN, CLK18M_INT_EXT, CLK18M_INT_XOUT, INT_REF_CLK_OUT
CRITICAL Y2 OMIT 18.432M 8X4.5MM-SM
C152 22pF, C151 22pF
R802 10K MMM_SIRQ_L, R801 10K MMM_FFIRQ_L
CRYSTAL LOAD CAPACITANCE IS 16PF

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

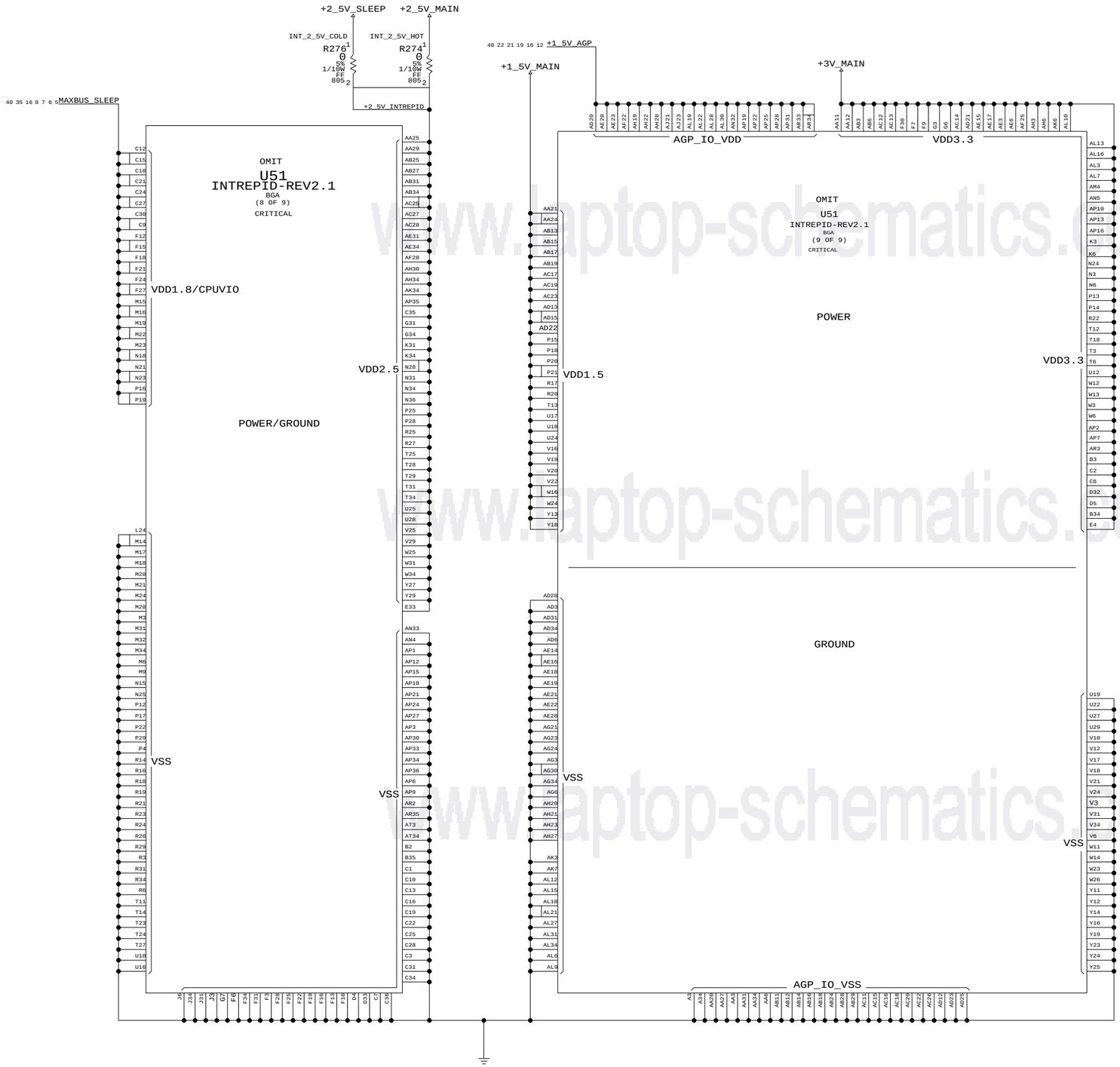
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0090	1	XTAL,CER,LOW PROF,18,432MHZ,8X4.5MM,SMD	Y2	CRITICAL	?

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

INT - USB/GPIOS/I2S

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 14 OF 46	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0305	1	IC,ASIC,INTREPID,REV2.1,974 BGA,FAST	U51	CRITICAL	?

Intrepid Power

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 15 OF 46	

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
28 X 0.22UF (0402)

35 15 8 7 6 5 MAXBUS_SLEEP 40

C148 10uF 20% 6.3V CERM 805 1 2
C142 10uF 20% 6.3V CERM 805 1 2
C144 10uF 20% 6.3V CERM 805 1 2
C146 10uF 20% 6.3V CERM 805 1 2

C182 0.22uF 20% 6.3V CERM 402 1 2
C178 0.22uF 20% 6.3V CERM 402 1 2
C141 0.22uF 20% 6.3V CERM 402 1 2
C145 0.22uF 20% 6.3V CERM 402 1 2
C214 0.22uF 20% 6.3V CERM 402 1 2
C163 0.22uF 20% 6.3V CERM 402 1 2
C164 0.22uF 20% 6.3V CERM 402 1 2
C225 0.22uF 20% 6.3V CERM 402 1 2
C160 0.22uF 20% 6.3V CERM 402 1 2
C159 0.22uF 20% 6.3V CERM 402 1 2
C204 0.22uF 20% 6.3V CERM 402 1 2
C166 0.22uF 20% 6.3V CERM 402 1 2
C205 0.22uF 20% 6.3V CERM 402 1 2
C223 0.22uF 20% 6.3V CERM 402 1 2
C229 0.22uF 20% 6.3V CERM 402 1 2
C181 0.22uF 20% 6.3V CERM 402 1 2
C207 0.22uF 20% 6.3V CERM 402 1 2
C208 0.22uF 20% 6.3V CERM 402 1 2
C183 0.22uF 20% 6.3V CERM 402 1 2
C180 0.22uF 20% 6.3V CERM 402 1 2
C165 0.22uF 20% 6.3V CERM 402 1 2
C206 0.22uF 20% 6.3V CERM 402 1 2
C147 0.22uF 20% 6.3V CERM 402 1 2
C149 0.22uF 20% 6.3V CERM 402 1 2
C179 0.22uF 20% 6.3V CERM 402 1 2
C162 0.22uF 20% 6.3V CERM 402 1 2
C161 0.22uF 20% 6.3V CERM 402 1 2
C213 0.22uF 20% 6.3V CERM 402 1 2

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C324 10uF 20% 6.3V CERM 805 1 2
C325 10uF 20% 6.3V CERM 805 1 2
C201 10uF 20% 6.3V CERM 805 1 2
C200 10uF 20% 6.3V CERM 805 1 2

C299 0.22uF 20% 6.3V CERM 402 1 2
C279 0.22uF 20% 6.3V CERM 402 1 2
C262 0.22uF 20% 6.3V CERM 402 1 2
C292 0.22uF 20% 6.3V CERM 402 1 2
C248 0.22uF 20% 6.3V CERM 402 1 2
C302 0.22uF 20% 6.3V CERM 402 1 2
C300 0.22uF 20% 6.3V CERM 402 1 2
C290 0.22uF 20% 6.3V CERM 402 1 2
C272 0.22uF 20% 6.3V CERM 402 1 2
C259 0.22uF 20% 6.3V CERM 402 1 2
C301 0.22uF 20% 6.3V CERM 402 1 2
C278 0.22uF 20% 6.3V CERM 402 1 2
C226 0.22uF 20% 6.3V CERM 402 1 2
C238 0.22uF 20% 6.3V CERM 402 1 2
C250 0.22uF 20% 6.3V CERM 402 1 2
C263 0.22uF 20% 6.3V CERM 402 1 2
C224 0.22uF 20% 6.3V CERM 402 1 2
C222 0.22uF 20% 6.3V CERM 402 1 2
C261 0.22uF 20% 6.3V CERM 402 1 2
C227 0.22uF 20% 6.3V CERM 402 1 2
C271 0.22uF 20% 6.3V CERM 402 1 2
C310 0.22uF 20% 6.3V CERM 402 1 2
C288 0.22uF 20% 6.3V CERM 402 1 2
C260 0.22uF 20% 6.3V CERM 402 1 2
C303 0.22uF 20% 6.3V CERM 402 1 2
C287 0.22uF 20% 6.3V CERM 402 1 2
C258 0.22uF 20% 6.3V CERM 402 1 2
C236 0.22uF 20% 6.3V CERM 402 1 2
C289 0.22uF 20% 6.3V CERM 402 1 2

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
21 X 0.22UF (0402)

40 22 21 19 15 12 +1_5V_AGP

C381 10uF 20% 6.3V CERM 805 1 2
C380 10uF 20% 6.3V CERM 805 1 2
C382 10uF 20% 6.3V CERM 805 1 2
C379 10uF 20% 6.3V CERM 805 1 2

C367 0.22uF 20% 6.3V CERM 402 1 2
C319 0.22uF 20% 6.3V CERM 402 1 2
C330 0.22uF 20% 6.3V CERM 402 1 2
C363 0.22uF 20% 6.3V CERM 402 1 2
C366 0.22uF 20% 6.3V CERM 402 1 2
C332 0.22uF 20% 6.3V CERM 402 1 2
C361 0.22uF 20% 6.3V CERM 402 1 2
C320 0.22uF 20% 6.3V CERM 402 1 2
C328 0.22uF 20% 6.3V CERM 402 1 2
C364 0.22uF 20% 6.3V CERM 402 1 2
C365 0.22uF 20% 6.3V CERM 402 1 2
C329 0.22uF 20% 6.3V CERM 402 1 2
C345 0.22uF 20% 6.3V CERM 402 1 2
C346 0.22uF 20% 6.3V CERM 402 1 2
C373 0.22uF 20% 6.3V CERM 402 1 2
C344 0.22uF 20% 6.3V CERM 402 1 2
C331 0.22uF 20% 6.3V CERM 402 1 2
C312 0.22uF 20% 6.3V CERM 402 1 2
C354 0.22uF 20% 6.3V CERM 402 1 2
C347 0.22uF 20% 6.3V CERM 402 1 2
C321 0.22uF 20% 6.3V CERM 402 1 2

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
40 X 0.22UF (0402)

+3V_MAIN

C378 10uF 20% 6.3V CERM 805 1 2
C376 10uF 20% 6.3V CERM 805 1 2
C377 10uF 20% 6.3V CERM 805 1 2
C375 10uF 20% 6.3V CERM 805 1 2

C170 0.22uF 20% 6.3V CERM 402 1 2
C358 0.22uF 20% 6.3V CERM 402 1 2
C268 0.22uF 20% 6.3V CERM 402 1 2
C327 0.22uF 20% 6.3V CERM 402 1 2
C342 0.22uF 20% 6.3V CERM 402 1 2
C215 0.22uF 20% 6.3V CERM 402 1 2
C352 0.22uF 20% 6.3V CERM 402 1 2
C171 0.22uF 20% 6.3V CERM 402 1 2
C158 0.22uF 20% 6.3V CERM 402 1 2
C309 0.22uF 20% 6.3V CERM 402 1 2
C175 0.22uF 20% 6.3V CERM 402 1 2
C357 0.22uF 20% 6.3V CERM 402 1 2
C351 0.22uF 20% 6.3V CERM 402 1 2
C350 0.22uF 20% 6.3V CERM 402 1 2
C286 0.22uF 20% 6.3V CERM 402 1 2
C176 0.22uF 20% 6.3V CERM 402 1 2
C189 0.22uF 20% 6.3V CERM 402 1 2
C167 0.22uF 20% 6.3V CERM 402 1 2
C371 0.22uF 20% 6.3V CERM 402 1 2
C359 0.22uF 20% 6.3V CERM 402 1 2
C285 0.22uF 20% 6.3V CERM 402 1 2
C283 0.22uF 20% 6.3V CERM 402 1 2
C269 0.22uF 20% 6.3V CERM 402 1 2
C221 0.22uF 20% 6.3V CERM 402 1 2
C234 0.22uF 20% 6.3V CERM 402 1 2
C247 0.22uF 20% 6.3V CERM 402 1 2
C257 0.22uF 20% 6.3V CERM 402 1 2
C343 0.22uF 20% 6.3V CERM 402 1 2
C313 0.22uF 20% 6.3V CERM 402 1 2
C228 0.22uF 20% 6.3V CERM 402 1 2
C360 0.22uF 20% 6.3V CERM 402 1 2
C308 0.22uF 20% 6.3V CERM 402 1 2
C318 0.22uF 20% 6.3V CERM 402 1 2
C237 0.22uF 20% 6.3V CERM 402 1 2
C317 0.22uF 20% 6.3V CERM 402 1 2
C341 0.22uF 20% 6.3V CERM 402 1 2
C177 0.22uF 20% 6.3V CERM 402 1 2
C212 0.22uF 20% 6.3V CERM 402 1 2
C349 0.22uF 20% 6.3V CERM 402 1 2
C184 0.22uF 20% 6.3V CERM 402 1 2

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
46 X 0.22UF (0402)

40 15 10 9 +2_5V_INTREPID

C314 10uF 20% 6.3V CERM 805 1 2
C322 10uF 20% 6.3V CERM 805 1 2
C191 10uF 20% 6.3V CERM 805 1 2
C202 10uF 20% 6.3V CERM 805 1 2

C304 0.22uF 20% 6.3V CERM 402 1 2
C266 0.22uF 20% 6.3V CERM 402 1 2
C172 0.22uF 20% 6.3V CERM 402 1 2
C281 0.22uF 20% 6.3V CERM 402 1 2
C243 0.22uF 20% 6.3V CERM 402 1 2
C253 0.22uF 20% 6.3V CERM 402 1 2
C334 0.22uF 20% 6.3V CERM 402 1 2
C241 0.22uF 20% 6.3V CERM 402 1 2
C348 0.22uF 20% 6.3V CERM 402 1 2
C192 0.22uF 20% 6.3V CERM 402 1 2
C306 0.22uF 20% 6.3V CERM 402 1 2
C252 0.22uF 20% 6.3V CERM 402 1 2
C275 0.22uF 20% 6.3V CERM 402 1 2
C297 0.22uF 20% 6.3V CERM 402 1 2
C240 0.22uF 20% 6.3V CERM 402 1 2
C218 0.22uF 20% 6.3V CERM 402 1 2
C274 0.22uF 20% 6.3V CERM 402 1 2
C369 0.22uF 20% 6.3V CERM 402 1 2
C368 0.22uF 20% 6.3V CERM 402 1 2
C168 0.22uF 20% 6.3V CERM 402 1 2
C265 0.22uF 20% 6.3V CERM 402 1 2
C251 0.22uF 20% 6.3V CERM 402 1 2
C216 0.22uF 20% 6.3V CERM 402 1 2
C254 0.22uF 20% 6.3V CERM 402 1 2
C305 0.22uF 20% 6.3V CERM 402 1 2
C186 0.22uF 20% 6.3V CERM 402 1 2
C219 0.22uF 20% 6.3V CERM 402 1 2
C315 0.22uF 20% 6.3V CERM 402 1 2
C264 0.22uF 20% 6.3V CERM 402 1 2
C294 0.22uF 20% 6.3V CERM 402 1 2
C323 0.22uF 20% 6.3V CERM 402 1 2
C273 0.22uF 20% 6.3V CERM 402 1 2
C242 0.22uF 20% 6.3V CERM 402 1 2
C203 0.22uF 20% 6.3V CERM 402 1 2
C333 0.22uF 20% 6.3V CERM 402 1 2
C217 0.22uF 20% 6.3V CERM 402 1 2
C230 0.22uF 20% 6.3V CERM 402 1 2
C293 0.22uF 20% 6.3V CERM 402 1 2
C231 0.22uF 20% 6.3V CERM 402 1 2
C296 0.22uF 20% 6.3V CERM 402 1 2
C239 0.22uF 20% 6.3V CERM 402 1 2
C316 0.22uF 20% 6.3V CERM 402 1 2
C185 0.22uF 20% 6.3V CERM 402 1 2
C282 0.22uF 20% 6.3V CERM 402 1 2
C295 0.22uF 20% 6.3V CERM 402 1 2
C280 0.22uF 20% 6.3V CERM 402 1 2

INTREPID/MAIN 2.5V DECOUPLING

10 X 0.22UF (0402)

+2_5V_MAIN

C770 0.22uF 20% 6.3V CERM 402 1 2
C139 0.22uF 20% 6.3V CERM 402 1 2
C335 0.22uF 20% 6.3V CERM 402 1 2
C735 0.22uF 20% 6.3V CERM 402 1 2
C245 0.22uF 20% 6.3V CERM 402 1 2
C736 0.22uF 20% 6.3V CERM 402 1 2
C739 0.22uF 20% 6.3V CERM 402 1 2
C395 0.22uF 20% 6.3V CERM 402 1 2
C374 0.22uF 20% 6.3V CERM 402 1 2
C385 0.22uF 20% 6.3V CERM 402 1 2

Place these 2.5V Decoupling Caps near the Edge of +2.5V_MAIN and +2.5V_INTREPID split

Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 16 OF 46	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,LW PROF,30.0000MHZ,8X4.5MM,SMD	Y1	CRITICAL	?

+3V_NEC_VDD 17 40

C749 0.1uF 20% 10V CERM 402
C746 0.1uF 20% 10V CERM 402
C761 0.1uF 20% 10V CERM 402
C750 0.1uF 20% 10V CERM 402
C756 0.1uF 20% 10V CERM 402
C748 0.1uF 20% 10V CERM 402
C769 0.1uF 20% 10V CERM 402
C752 0.1uF 20% 10V CERM 402
C747 0.1uF 20% 10V CERM 402
C197 10uF 20% 6.3V CERM 805
C765 0.1uF 20% 10V CERM 402
C768 0.1uF 20% 10V CERM 402

+3V_MAIN
L7 FERR-EMI-100-OHM SM
R172 0 5% 1/16W MF 603
C760 0.1uF 20% 10V CERM 402
C751 0.1uF 20% 10V CERM 402
C173 10uF 20% 6.3V CERM 805
40 NEC_AVDD
40 17 +3V_NEC_VDD

Y1's LOAD CAPACITANCE = 16 pF
OMIT
CRITICAL
Y1 30.0000M 8X4.5MM-SM
NEC_XT2_R
C759 27pF 5% 50V CERM 402
C136 27pF 5% 50V CERM 402
R124 100 5% 1/16W MF 402

R613 43.2 1% 1/16W MF 402 — NEC_USB_DAM 27 39 41
Low/Full/High Speed (External)
R612 43.2 1% 1/16W MF 402 — NEC_USB_DAP 27 39 41
R609 43.2 1% 1/16W MF 402 — NEC_USB_DBM 27 39 41
Low/Full/High Speed (External)
R610 43.2 1% 1/16W MF 402 — NEC_USB_DBP 27 39 41

CRITICAL
U17
NEC_uPD720101_USB2
FBGA

H3 M4 C8 P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 — VDD_PCI
VDD
N10 N12 — AVDD

41 39 26 18 12 9 PCI_AD<0>	M5	AD0
41 39 26 18 12 9 PCI_AD<1>	P5	AD1
41 39 26 18 12 9 PCI_AD<2>	N5	AD2
41 39 26 18 12 9 PCI_AD<3>	P4	AD3
41 39 26 18 12 9 PCI_AD<4>	N4	AD4
41 39 26 18 12 9 PCI_AD<5>	M3	AD5
41 39 26 18 12 9 PCI_AD<6>	N3	AD6
41 39 26 18 12 9 PCI_AD<7>	M1	AD7
41 39 26 18 12 9 PCI_AD<8>	L2	AD8
41 39 26 18 12 9 PCI_AD<9>	L1	AD9
41 39 26 18 12 9 PCI_AD<10>	K2	AD10
41 39 26 18 12 9 PCI_AD<11>	L3	AD11
41 39 26 18 12 9 PCI_AD<12>	K1	AD12
41 39 26 18 12 9 PCI_AD<13>	K3	AD13
41 39 26 18 12 9 PCI_AD<14>	J2	AD14
41 39 26 18 12 9 PCI_AD<15>	J1	AD15
41 39 26 18 12 9 PCI_AD<16>	F2	AD16
41 39 26 18 12 9 PCI_AD<17>	E3	AD17
41 39 26 18 12 9 PCI_AD<18>	E1	AD18
41 39 26 18 12 9 PCI_AD<19>	D3	AD19
41 39 26 18 12 9 PCI_AD<20>	D1	AD20
41 39 26 18 12 PCI_AD<21>	D2	AD21
41 39 26 18 12 PCI_AD<22>	C2	AD22
41 39 26 18 12 PCI_AD<23>	C1	AD23
41 39 26 18 12 9 PCI_AD<24>	B4	AD24
41 39 26 18 12 9 PCI_AD<25>	A4	AD25
41 39 26 18 12 9 PCI_AD<26>	B5	AD26
(PCI_AD<27>)	C4	AD27
41 39 26 18 12 9 PCI_AD<28>	A5	AD28
41 39 26 18 12 9 PCI_AD<29>	C5	AD29
41 39 26 18 12 9 PCI_AD<30>	B6	AD30
41 39 26 18 12 9 PCI_AD<31>	A6	AD31
39 26 18 12 PCI_CBE<0>	M2	CBE0
39 26 18 12 PCI_CBE<1>	J3	CBE1
39 26 18 12 PCI_CBE<2>	F1	CBE2
39 26 18 12 PCI_CBE<3>	C3	CBE3
41 39 26 18 12 PCI_PAR	J4	PAR
41 39 26 18 12 PCI_FRAME_L	F3	FRAME
41 39 26 18 12 PCI_IRDY_L	F4	IRDY
41 39 26 18 12 PCI_TRDY_L	G1	TRDY
41 39 26 18 12 PCI_STOP_L	G3	STOP
NEC_IDSEL	B3	IDSEL
41 39 26 18 12 PCI_DEVSEL_L	G2	DEVSEL
12 NEC_PCI_REQ_L	C6	REQ
12 NEC_PCI_GNT_L	D6	GNT
18 PCI_PERR_L	H2	PERR
18 PCI_SERR_L	H1	SERR
NEC_PCI_INTA_L	C7	INTA
NEC_PCI_INTB_L	B7	INTB
NEC_PCI_INTC_L	A7	INTC
37 12 CLK33M_NEC	A8	PCLK
17 NEC_IO_RESET_L	B8	VBRRST
NEC_CRUN_L	N6	CRUN
17 NEC_PME_L	D8	PME
17 NEC_MAIN_RESET_L	C8	VCCRST
NEC_SMI_L_TP	L6	SMI
17 NEC_LEGC	L7	LEGC

R636 22 5% 1/16W MF 402
Series Rpaks required to facilitate NAND-tree testing
RP45 47 5% 1/16W SM1
14 NEC_PCI_INT
R617 4.7k 5% 1/16W MF 402
RP44 47 5% 1/16W SM1
31 28 25 24 IO_RESET_L — NEC_IO_RESET_L 17
41 31 26 14 PMU_PME_L — NEC_PME_L 17
41 31 26 20 19 18 14 MAIN_RESET_L — NEC_MAIN_RESET_L 17
17 NEC_LEGC

VSS
B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8

XT1/SCLK L9 NEC_XT1
XT2 P8 NEC_XT2
RSDM1 M14 NEC_USB_RSDM1
DM1 M13 (NEC_USB_DAM)
DP1 L14 (NEC_USB_DAP)
RSDP1 K13 NEC_USB_RSDP1
RSDM2 K14 NEC_USB_RSDM2
DM2 K12 (NEC_USB_DBM)
DP2 J14 (NEC_USB_DBP)
RSDP2 J12 NEC_USB_RSDP2
RSDM3 H11 NC
DM3 G11
DP3 G13
RSDP3 G14 NC
RSDM4 F12 NC
DM4 F14
DP4 E12
RSDP4 E14 NC
RSDM5 E13 NC
DM5 D14
DP5 C13
RSDP5 C14 NC
RREF P11 NEC_RREF
R614 9.09K 1% 1/16W MF 402 — Tie to GND (NEC_AVSS_F) at ball N11
NEC_AVSS_F 17

OCI1 B12 NEC_LUSB_OCI
OCI2 B11 NEC_RUSB_OCI
OCI3 B10 NEC_OCI<3>
OCI4 A10 NEC_OCI<4>
OCI5 B9 NEC_OCI<5>
RP43 10K 5% 1/16W SM1
R606 10K 5% 1/16W MF 402
R615 1K 5% 1/16W MF 402
R632 1K 5% 1/16W MF 402
+3V_NEC_VDD 17 40

PPON1 C12 OUT NEC_LUSB_PPON 41
PPON2 A11 OUT NEC_RUSB_PPON 41
PPON3 C11 OUT NEC_PPON3_TP
PPON4 C10 OUT NEC_PPON4_TP
PPON5 A9 OUT NEC_PPON5_TP
NC1 P6 NEC_NC<1>
NC2 M6 NEC_NC<2>

NEC documentation indicates that NCs must be tied high.

NTEST1 M8 IPD NC
SMC M7 IPD NC
TEB N7 IPD NC
AMC P7 IPD NEC_AMC_TP
TEST L8 IPD NC
NANDTEST M10 NEC_NANDTESTEN_TP
SRCLK M9 NC
SRDTA N9 NEC_NANDTESTOUT_TP
SRMOD P9 IPD NC
AVSS N11 P13 M12
R798 0 5% 1/16W MF 603 — NEC_AVSS_F

+3V_MAIN
RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
R607 0 5% 1/16W MF 402 — 17 NEC_LUSB_OCI — NEC_LUSB_OCI_UF 27 41
R608 0 5% 1/16W MF 402 — 17 NEC_RUSB_OCI — NEC_RUSB_OCI_UF 27 41
NO STUFF C743 0.1uF 20% 10V CERM 402
NO STUFF C744 0.1uF 20% 10V CERM 402

USB 2.0

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 17 OF 46	

PCI1510 PULL-UPS

+3V_SLEEP_PCCARD

R718 10K 5% 1/16W MF 402 — PCI_PERR_L (17 18)

R714 10K 5% 1/16W MF 402 — PCI_SERR_L (17 18)

R722 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU (18)

+2_5V_SLEEP

C787 4.7uF 20% 6.3V CERM 805

C786 0.22uF 20% 6.3V CERM 402

+3V_SLEEP

R756 0 5% 1/16W MF 603 — (40) +3V_SLEEP_PCCARD

C60 10uF 20% 6.3V CERM 805

C776 10uF 20% 6.3V CERM 805

C789 0.22uF 20% 6.3V CERM 402

C791 0.22uF 20% 6.3V CERM 402

C784 0.22uF 20% 6.3V CERM 402

C782 0.22uF 20% 6.3V CERM 402

C783 0.22uF 20% 6.3V CERM 402

C778 0.22uF 20% 6.3V CERM 402

C775 0.22uF 20% 6.3V CERM 402

R721 10K 5% 1/16W MF 402

A7 C13 D5 E1 M1 N7 N11 — VCC

(36 38 44) SLEEP_L_LS5

R726 0 5% 1/16W MF 402

+3V_MAIN

+5V_MAIN

U4 TPS2211 SSOI

NC	9		
V_12	5	AVPP	10
V_5_1	6		
V_5_2	3	AVCC0	11
V_3_1	4	AVCC1	12
V_3_2		AVCC2	13
VCCD0	1		
VCCD1	2		
VPPD0	15		
VPPD1	14		
SHTDWN	16		
GND	7	OC	8 NC

TPS2211_SHTDWN_L

+VPP_CBUS_SW (18 40)

+VCC_CBUS_SW (18 40)

C40 0.1uF 20% 16V CERM 402

C37 0.1uF 20% 16V CERM 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

U8 PCI1510GGU BGA

CRITICAL CLAMP FOR PC-CARD
CLAMP FOR PCI

NC	H10	CLK_48_RSVD/NC
PCI1510_VR_EN_L	D4	VR_EN*
	L8	VR_PORT
PCI_AD<0>	N8	AD0
PCI_AD<1>	M7	AD1
PCI_AD<2>	L7	AD2
PCI_AD<3>	N6	AD3
PCI_AD<4>	K4	AD4
PCI_AD<5>	M6	AD5
PCI_AD<6>	L6	AD6
PCI_AD<7>	N5	AD7
PCI_AD<8>	N4	AD8
PCI_AD<9>	M2	AD9
PCI_AD<10>	M5	AD10
PCI_AD<11>	L4	AD11
PCI_AD<12>	N3	AD12
PCI_AD<13>	K5	AD13
PCI_AD<14>	L5	AD14
PCI_AD<15>	M4	AD15
PCI_AD<16>	J4	AD16
PCI_AD<17>	H1	AD17
PCI_AD<18>	H3	AD18
(PCI_AD<19>)	H2	AD19
PCI_AD<20>	G2	AD20
PCI_AD<21>	G4	AD21
PCI_AD<22>	F1	AD22
PCI_AD<23>	C3	AD23
PCI_AD<24>	F3	AD24
PCI_AD<25>	E2	AD25
PCI_AD<26>	F4	AD26
PCI_AD<27>	B1	AD27
PCI_AD<28>	D2	AD28
PCI_AD<29>	E4	AD29
PCI_AD<30>	D3	AD30
PCI_AD<31>	E3	AD31
PCI_CBE<0>	K6	C/BE0*
PCI_CBE<1>	M3	C/BE1*
PCI_CBE<2>	J2	C/BE2*
PCI_CBE<3>	A1	C/BE3*
PCI_PAR	N1	PAR
PCI_IRDY_L	K1	IRDY
PCI_SERR_L	L2	SERR
CBUS_PCI_IDSEL	F2	IDSEL
PCI_PERR_L	K3	PERR
PCI_FRAME_L	J1	FRAME
PCI_STOP_L	L1	STOP
PCI_TRDY_L	J3	TRDY
PCI_DEVSEL_L	K2	DEVSEL
CBUS_PCI_RESET_L	G3	PRST
CBUS_PCI_REQ_L	C2	REQ
CBUS_PCI_GNT_L	C1	GNT
CLK33M_CBUS	G1	PCLK
	M9	SPKROUT
	M8	RI_OUT/PME
CBUS_SUSPEND_PD	L10	SUSPEND
CBUS_INT_L	K7	MFUNC0
CBUS_MFUNC1_PD	N9	MFUNC1
CBUS_MFUNC2_PD	L9	MFUNC2
CBUS_MFUNC3_PD	K10	MFUNC3
CBUS_MFUNC4_PD	M10	MFUNC4
CBUS_MFUNC5_PD	N12	MFUNC5
CBUS_MFUNC6_PD	L10	MFUNC6
	L11	GRST

	N13	VCCB
	L3	VCCP
VCCD0*	N13	CBUS_VCCD0_L
VCCD1*	L12	CBUS_VCCD1_L
VPPD0	K9	CBUS_VPPD0
VPPD1	M11	CBUS_VPPD1
CD1*/CCD1*	L13	CBUS_DET_1_L (18 41)
CD2*/CCD2*	B5	CBUS_DET_2_L (18 41)
IORD*/CAD13	F12	CBUS_IORD_L (18)
IOWR*/CAD15	C11	CBUS_IOWR_L (18)
OE*/CAD11	G10	CBUS_OE_L (18)
CE1*/CC/BE0*	H13	CBUS_CE1_L (18)
VS1*/CVS1	B2	CBUS_VS1 (18)
VS2*/CVS2	A9	CBUS_VS2 (18)
WE*/CGNT*	D13	CBUS_WE_L (18)
RDY/IREQ*/CINT*	A6	CBUS_READY (18)
RESET/CRST*	D8	CBUS_RESET_L (18)
REG*/CC/BE3*	A8	CBUS_REG_L (18)
BVD1/CSTSCHG/STSCHG*/RI*	C6	CBUS_BVD1_L (18)
BVD2/SPKR*/CAUDIO	D6	CBUS_BVD2_L (18)
INTEGRATED PULL-UP WP/IOIS16*/CCLKRUN*	A5	CBUS_WP_L (18)
CE2/CAD10*	G13	CBUS_CE2_L (18)
INPACK/CREQ*	B8	CBUS_INPACK_L (18)
WAIT/CSERR*	B6	CBUS_WAIT_L (18)
A0/CAD26	C7	CBUS_ADDR<0> (18)
A1/CAD25	D7	CBUS_ADDR<1> (18)
A2/CAD24	B7	CBUS_ADDR<2> (18)
A3/CAD23	D10	CBUS_ADDR<3> (18)
A4/CAD22	B12	CBUS_ADDR<4> (18)
A5/CAD21	C8	CBUS_ADDR<5> (18)
A6/CAD20	C9	CBUS_ADDR<6> (18)
A7/CAD18	A12	CBUS_ADDR<7> (18)
A8/CC/BE1*	E11	CBUS_ADDR<8> (18)
A9/CAD14	F11	CBUS_ADDR<9> (18)
A10/CAD9	G11	CBUS_ADDR<10> (18)
A11/CAD12	G12	CBUS_ADDR<11> (18)
A12/CC/BE2*	D9	CBUS_ADDR<12> (18)
A13/CPAR	E12	CBUS_ADDR<13> (18)
A14/CPERR*	D12	CBUS_ADDR<14> (18)
A15/CIRDY*	C10	CBUS_ADDR<15> (18)
A16/CCLK	B13	CBUS_ADDR_16_UF
A17/CAD16	F10	CBUS_ADDR<17> (18)
A18/RSVD	E13	CBUS_ADDR<18> (18)
A19/CBLOCK*	A13	CBUS_ADDR<19> (18)
A20/CSTOP*	E10	CBUS_ADDR<20> (18)
A21/CDEVSEL*	D11	CBUS_ADDR<21> (18)
A22/CTRDY*	C12	CBUS_ADDR<22> (18)
A23/CFRAME*	A10	CBUS_ADDR<23> (18)
A24/CAD17	B10	CBUS_ADDR<24> (18)
A25/CAD19	B9	CBUS_ADDR<25> (18)
D0/CAD27	A4	CBUS_DATA<0> (18)
D1/CAD29	C4	CBUS_DATA<1> (18)
D2/RSVD	A3	CBUS_DATA<2> (18)
D3/CAD0	K11	CBUS_DATA<3> (18)
D4/CAD1	K12	CBUS_DATA<4> (18)
D5/CAD3	J13	CBUS_DATA<5> (18)
D6/CAD5	J10	CBUS_DATA<6> (18)
D7/CAD7	H12	CBUS_DATA<7> (18)
D8/CAD28	C5	CBUS_DATA<8> (18)
D9/CAD30	B4	CBUS_DATA<9> (18)
D10/CAD31	B3	CBUS_DATA<10> (18)
D11/CAD2	M12	CBUS_DATA<11> (18)
D12/CAD4	J11	CBUS_DATA<12> (18)
D13/CAD6	K13	CBUS_DATA<13> (18)
D14/RSVD	J12	CBUS_DATA<14> (18)
D15/CAD8	H11	CBUS_DATA<15> (18)

R724 47 5% 1/16W MF 402 — CBUS_ADDR<16> (18)

R719 22 5% 1/16W MF 402

R723 47 5% 1/16W MF 402 — MAIN_RESET_L (31 26 20 19 17 14)

RP1 10K 5% 1/32W 25V SM

5	6	CBUS_MFUNC1_PD (18)
10	4	CBUS_MFUNC2_PD (18)
	7	CBUS_MFUNC3_PD (18)
	3	CBUS_MFUNC4_PD (18)
	9	CBUS_MFUNC5_PD (18)
	8	CBUS_MFUNC6_PD (18)
	2	NC
	1	NC

GND: A2 A11 D1 F13 H4 K8 M13 N2

PC CARD/CARDBUS CONNECTOR

CRITICAL
J5
QT500806-L111
M-ST-SM1

	84	81	
	2	1	CBUS_DATA<3> (18)
CBUS_DET_1_L (18 41)	4	3	CBUS_DATA<4> (18)
CBUS_DATA<11> (18)	6	5	CBUS_DATA<5> (18)
CBUS_DATA<12> (18)	8	7	CBUS_DATA<6> (18)
CBUS_DATA<13> (18)	10	9	
	12	11	CBUS_DATA<7> (18)
CBUS_DATA<14> (18)	14	13	CBUS_CE1_L (18)
CBUS_DATA<15> (18)	16	15	CBUS_ADDR<10> (18)
CBUS_CE2_L (18)	18	17	CBUS_OE_L (18)
CBUS_VS1 (18)	20	19	
	22	21	CBUS_ADDR<11> (18)
CBUS_IORD_L (18)	24	23	CBUS_ADDR<9> (18)
CBUS_IOWR_L (18)	26	25	CBUS_ADDR<8> (18)
CBUS_ADDR<17> (18)	28	27	CBUS_ADDR<13> (18)
CBUS_ADDR<18> (18)	30	29	
	32	31	CBUS_ADDR<14> (18)
CBUS_ADDR<19> (18)	34	33	CBUS_WE_L (18)
CBUS_ADDR<20> (18)	36	35	CBUS_READY (18)
CBUS_ADDR<21> (18)	38	37	+VCC_CBUS_SW (18 40)
+VCC_CBUS_SW (18 40)	40	39	
	42	41	+VPP_CBUS_SW (18 40)
+VPP_CBUS_SW (18 40)	44	43	CBUS_ADDR<16> (18)
CBUS_ADDR<22> (18)	46	45	CBUS_ADDR<15> (18)
CBUS_ADDR<23> (18)	48	47	CBUS_ADDR<12> (18)
CBUS_ADDR<24> (18)	50	49	
	52	51	CBUS_ADDR<7> (18)
CBUS_ADDR<25> (18)	54	53	CBUS_ADDR<6> (18)
CBUS_VS2 (18)	56	55	CBUS_ADDR<5> (18)
CBUS_RESET_L (18)	58	57	CBUS_ADDR<4> (18)
CBUS_WAIT_L (18)	60	59	
	62	61	CBUS_ADDR<3> (18)
CBUS_INPACK_L (18)	64	63	CBUS_ADDR<2> (18)
CBUS_REG_L (18)	66	65	CBUS_ADDR<1> (18)
CBUS_BVD2_L (18)	68	67	CBUS_ADDR<0> (18)
CBUS_BVD1_L (18)	70	69	
	72	71	CBUS_DATA<0> (18)
CBUS_DATA<8> (18)	74	73	CBUS_DATA<1> (18)
CBUS_DATA<9> (18)	76	75	CBUS_DATA<2> (18)
CBUS_DATA<10> (18)	78	77	CBUS_WP_L (18)
CBUS_DET_2_L (41 18)	80	79	
	83	82	

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C796 2.2uF 20% 16V CERM 805

C800 2.2uF 20% 16V CERM 805

CARDBUS

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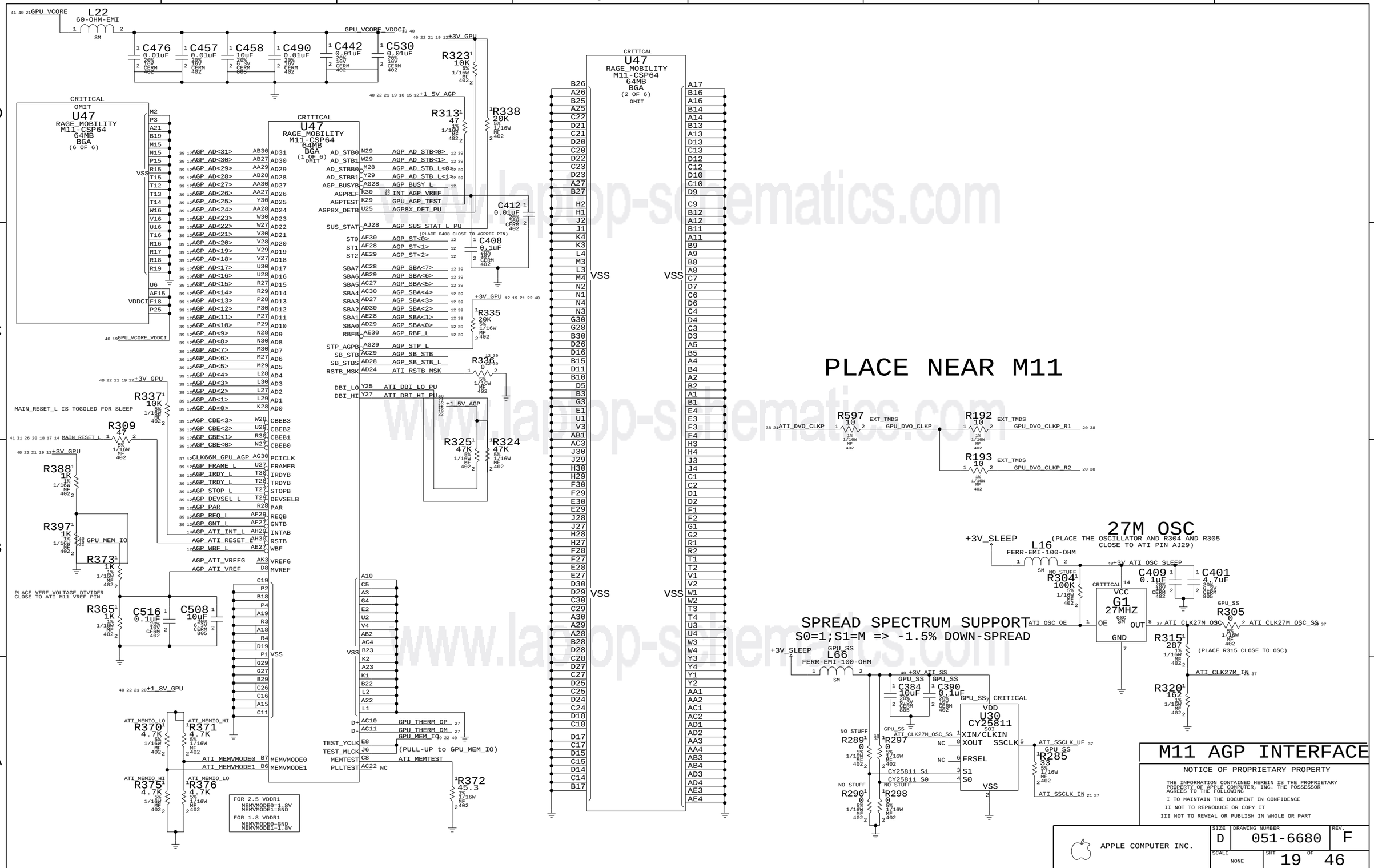
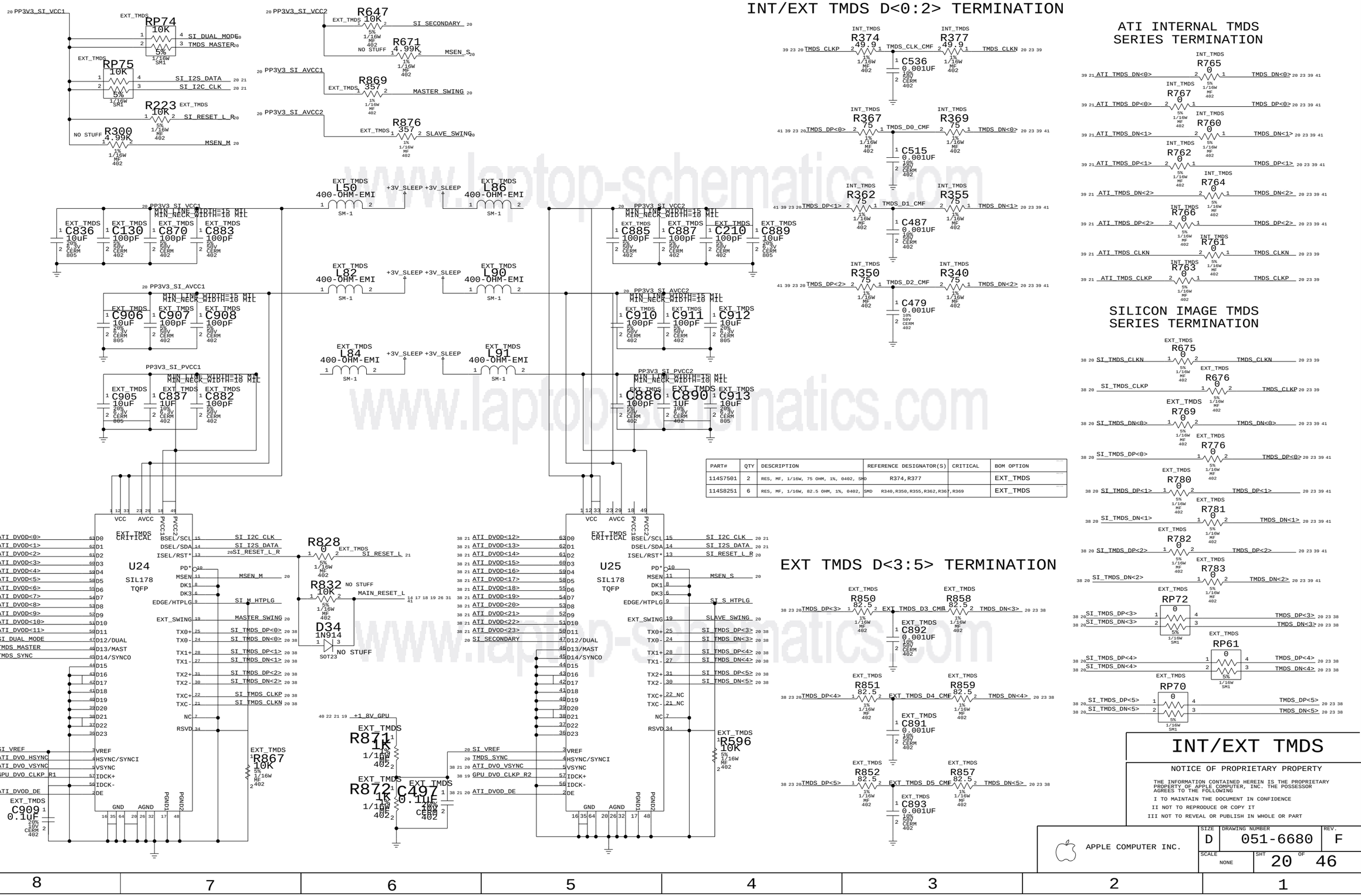
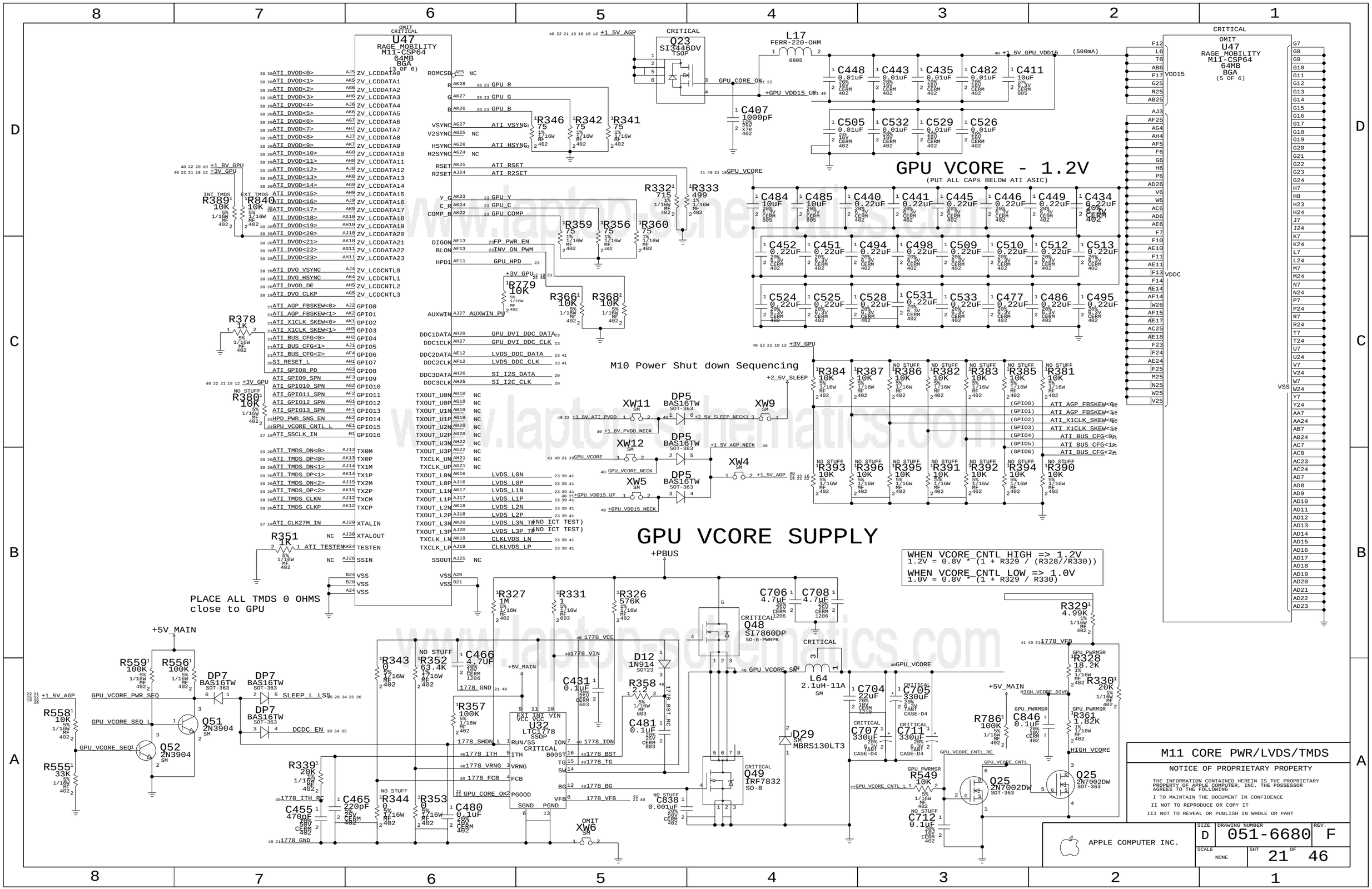
SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 18 OF 46	





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S7501	2	RES, MF, 1/16W, 75 OHM, 1%, 0402, SMD	R374,R377		EXT_TMDS
114S8251	6	RES, MF, 1/16W, 82.5 OHM, 1%, 0402, SMD	R340,R350,R355,R362,R367,R369		EXT_TMDS


U47
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(3 OF 6)
(5 OF 6)
Q23
SI3446DV
TSOP
L17
FERR-220-OHM
0805
GPU VCORE - 1.2V
(PUT ALL CAPS BELOW ATI ASIC)
M10 Power Shut down Sequencing
GPU VCORE SUPPLY
PLACE ALL TMDS 0 OHMS
close to GPU
WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)
U32
LTC1778
SSOP
Q48
SI7860DP
SO-8-PWRPK
Q49
IRF7832
SO-8
D29
MBRS130LT3
L64
2.1uH-11A
Q51
2N3904
Q52
2N3904
Q25
2N7002DW
SOT-363
M11 CORE PWR/LVDS/TMDS
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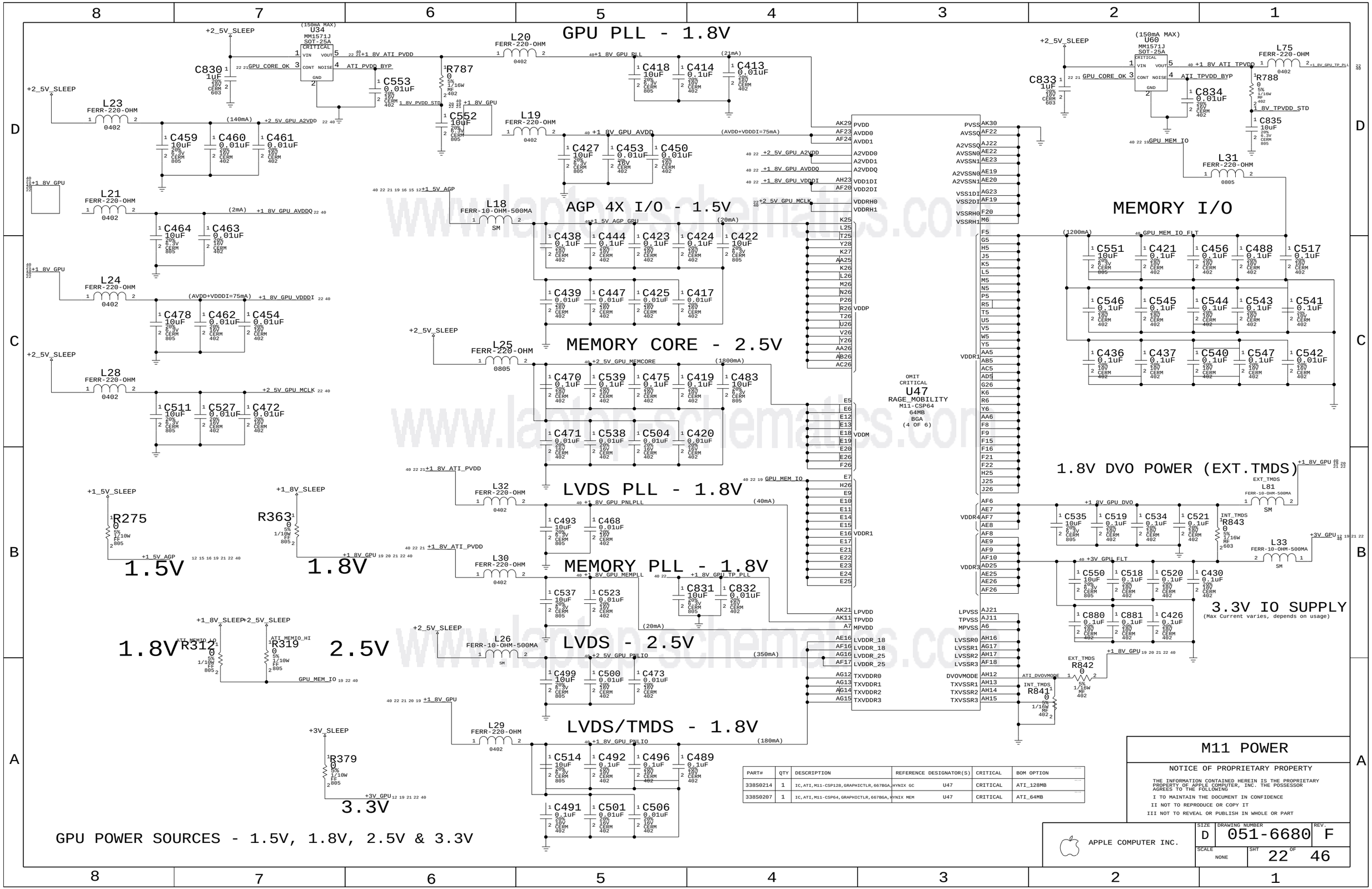
DRAWING NUMBER 051-6680
REV. F
SCALE NONE
SHT 21 OF 46



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0214	1	IC,ATI,M11-CSP128,GRAPHICTLR,667BGA,HYNIX GC	U47	CRITICAL	ATI_128MB
338S0207	1	IC,ATI,M11-CSP64,GRAPHICTLR,667BGA,HYNIX MEM	U47	CRITICAL	ATI_64MB

EXTERNAL VIDEO (DVI) INTERFACE

VGA SYNC BUFFERS

+3V_MAIN

74AHC1G32 U40 — OMIT L38 FERR-60-OHM-0.1A — ATI_VSYNC → ATI_VSYNC_BUF → VGA_VSYNC

74AHC1G32 U39 — OMIT L36 FERR-60-OHM-0.1A — ATI_HSYNC → ATI_HSYNC_BUF → VGA_HSYNC

PLACE L1002 & L1003 CLOSE TO DVI CONNECTOR

TMDS FILTERING

PLACE CLOSE TO CONNECTOR

L37 370-OHM — TMDS_CLKP, TMDS_CLKN → TMDS CONN CLKP, CLKN

ANALOG FILTERING

PLACE CLOSE TO CONNECTOR

FL1, FL2, FL3 LCFILTER SM-220MHZ CRITICAL — GPU_B, GPU_G, GPU_R → VGA_B, VGA_G, VGA_R

C641, C634, C631 3.3pF 0.25pF 50V CERM 402

R462, R458, R456 75 1% 1/16W MF 402 NO STUFF

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

+5V_SLEEP → F2 0.5AMP-13.2V CRITICAL → +5V_DDC_SLEEP_UF → L42 400-OHM-EMI → +5V_DDC_SLEEP

Isolation required for DVI power switch

D19 MBR0530 — DDC_CLK_ISO

R476 4.7K, R478 4.7K 5% 1/16W MF 402

R479 100 5% 1/16W MF 402

C654 100pF 5% 25V CERM 201

C655 100pF 5% 25V CERM 201

R465 100 5% 1/16W MF 402

C667 0.01UF 20% 50V CERM 603

C653 100pF 5% 25V CERM 201

PLACE NEAR C5A & C5B

R464 0 5% 1/16W MF 402

R463 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19 → CHGND1

3V LEVEL SHIFTERS

+3V_SLEEP

Q39 2N7002DW SOT-363 — DVI_DDC_CLK → GPU_DVI_DDC_CLK

Q39 2N7002DW SOT-363 — DVI_DDC_DATA → GPU_DVI_DDC_DATA

Q40 2N7002DW SOT-363 — DVI_HPD → GPU_HPD

R480 10K, R474 10K, R481 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

L47 CRITICAL 90-OHM-300mA 2012H — TMDS_CONN_DN<2>, TMDS_CONN_DP<2>

L46 CRITICAL 90-OHM-300mA 2012H — TMDS_CONN_DN<1>, TMDS_CONN_DP<1>

L44 CRITICAL 90-OHM-300mA 2012H EXT_TMDS — TMDS_DN<3>, TMDS_DP<3>

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from NVI7M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC CLK. since most rails will be low, TP0610 will turn on, driving SOFT_PWR_ON low. As most rails rise, TP0610 will turn off, and DDC CLK remote device path will be disabled as well.

Q38 TP0610 SM — DVI_DDC_CLK_DF, +5V_DDC_SLEEP

R473 680 5% 1/16W MF 402 — DVI_TURN_ON

R460 10K 5% 1/16W MF 402 — DVI_TURN_ON_TLM

Q35 MMDT3904 SOT-363 — DVI_TURN_ON_BASE → SOFT_PWR_ON_L

R459 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

+3V_SLEEP

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NVI7MAP

R485 68.1K 1% 1/16W MF 402, C668 0.1UF 20% 10V CERM 402

HPD_4V_REF

U42 LMC7211 SM — HPD_PWR_SW_BASE

R475 10K 5% 1/16W MF 402

Q35 MMDT3904 SOT-363

R472 10K 1% 1/16W MF 402 — DVI_HPD_UF → DVI_HPD_DIV

R484 100K 1% 1/16W MF 402

R482 10K 1% 1/16W MF 402

HPD_PWR_SW

R470 330 5% 1/16W MF 402

HPD_REF_EN_L

Q40 2N7002DW SOT-363 — HPD_PWR_SNS_EN

R483 470K 5% 1/16W MF 402

L49 CRITICAL 90-OHM-300mA 2012H EXT_TMDS — TMDS_DN<4>, TMDS_DP<4>

L85 CRITICAL 90-OHM-300mA 2012H EXT_TMDS — TMDS_DN<5>, TMDS_DP<5>

LCD INTERFACE

LVDS INTERFACE

J22 QHI112 F-RT-TH CRITICAL — CHGND1, CHGND2

TMDS_CONN_DN<2>, DN<1>, DP<2>, DP<1>, DN<4>, DN<3>, DP<4>, DP<3>, DN<5>, DP<5>

TMDS_DN<0>, TMDS_DP<0> → L45 90-OHM-300mA 2012H CRITICAL → TMDS_CONN_DN<0>, TMDS_CONN_DP<0>

TMDS_CLKP, TMDS_CLKN → TMDS_CONN_CLKP, CLKN

DVI_DDC_CLK_UF, DVI_DDC_DATA_UF, DVI_HPD_UF, VGA_VSYNC, VGA_R, VGA_G, VGA_B

(+5V_DDC_SLEEP)

LCD POWER SWITCH

+3V_MAIN

R347 100K 5% 1/16W MF 402, C474 2200pF 10% 50V CERM 603

R354 100K 5% 1/16W MF 402 — LCD_PWREN_L, LCD_DIGON_L

Q28 2N7002 SM — FP_PWR_EN

Q29 SI3443DV TSOP — +3V_LCD_SW → +3V_LCD

+3V_SLEEP

L27 FERR-250-OHM — +3V_LCD (LVDS DDC POWER)

C548 0.001UF 10% 50V CERM 402 → CHGND4

C503 0.001UF 10% 50V CERM 402 → CHGND4

J14 CRITICAL G-501973 F-RT-SM

LVDS_DDC_CLK, LVDS_DDC_DATA, LVDS_L0N, LVDS_L0P, LVDS_L1N, LVDS_L1P, LVDS_L2N, LVDS_L2P, CLKLVDS_LN, CLKLVDS_LP

R543 100K, R544 100K 1% 1/16W MF 402

C701 0.001UF 10% 50V CERM 402

LVDS_DDC_CLK, LVDS_DDC_DATA

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

NO STUFF C702 0.001UF 10% 50V CERM 402

C549 0.001UF 10% 50V CERM 402 → CHGND4

R753 0 5% 1/16W MF 402

C819 0.01UF 20% 50V CERM 603 → CHGND3

INVERTER INTERFACE

+PBUS

L73 FERR-1K-OHM-EMI — +14V_INV

+5V_MAIN

Q76 FDG6324L SC70-6 — FP_PWR_EN_L, +5V_INV_UF_SW

R750 100K 5% 1/16W MF 402

L74 400-OHM-EMI — +5V_INV_SW

C813 10UF 20% 6.3V CERM 805

C812 0.001UF 10% 50V CERM 402

J4 CRITICAL SM-2MT

C815 0.001UF 10% 50V CERM 402

Q76 FDG6324L SC70-6 — FP_PWR_EN

L72 400-OHM-EMI — BRIGHT_PWM

+3V_MAIN

C816 0.001UF 10% 50V CERM 402

C19 0.001UF 10% 50V CERM 402

L1 FERR-250-OHM — INV_GND → CHGND3

C22 0.1UF 10% 16V CERM 402

U2 NC7S32 SC70 — INV_ON_PWM → BRIGHT_PWM_UF

INVERTER EXPECTS ACTIVE HIGH SIGNAL

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW15 — GPU_TV_GND1 → L54 FERR-10-OHM-500MA → TV_GND1

XW14 — GPU_TV_GND2 → L56 FERR-10-OHM-500MA → TV_GND2

GPU_Y → L53 3.3UH 0603 → TV_Y

GPU_C → L57 3.3UH 0603 → TV_C

GPU_COMP → L55 3.3UH 0603 → TV_COMP

C663, C661, C664 560PF 10% 50V CERM 402

C657, C656, C660, C658, C659 0.01UF 20% 50V CERM 603

J21 CRITICAL MINIDIN RT-TH MH11773-WMR8A → CHGND1

Place GND shorts at graphics controller

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

VIDEO CONNECTORS

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D	051-6680	F
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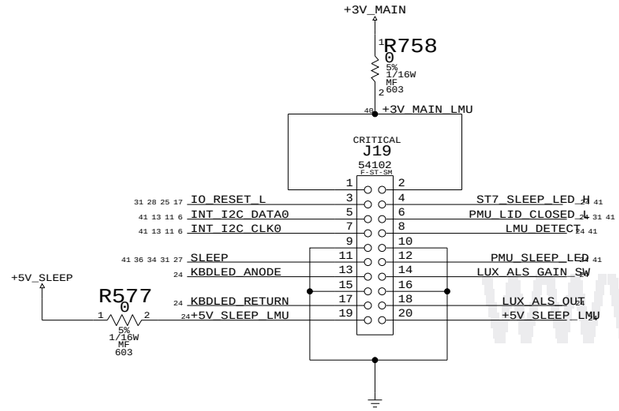
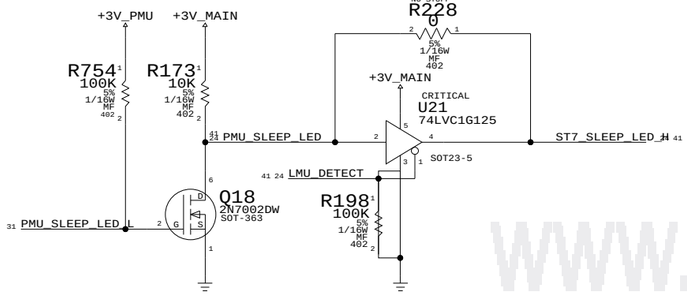
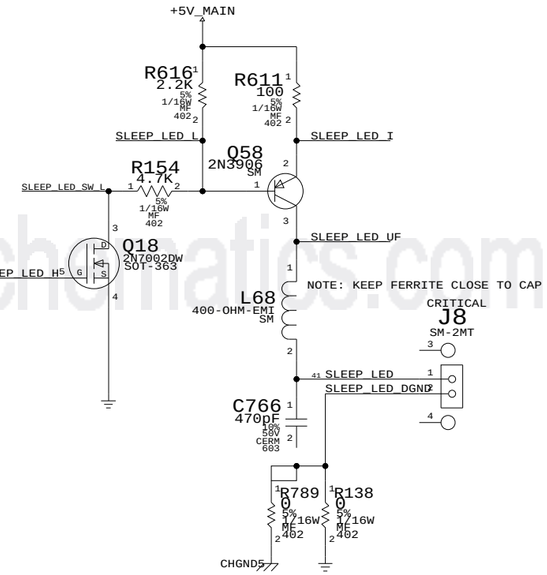
LMU/RIGHT SENSOR CONNECTOR

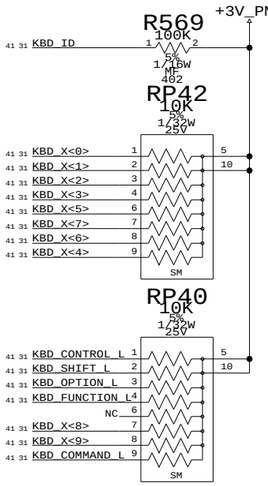




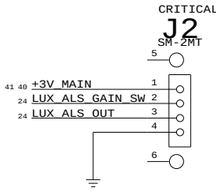
SLEEP LED



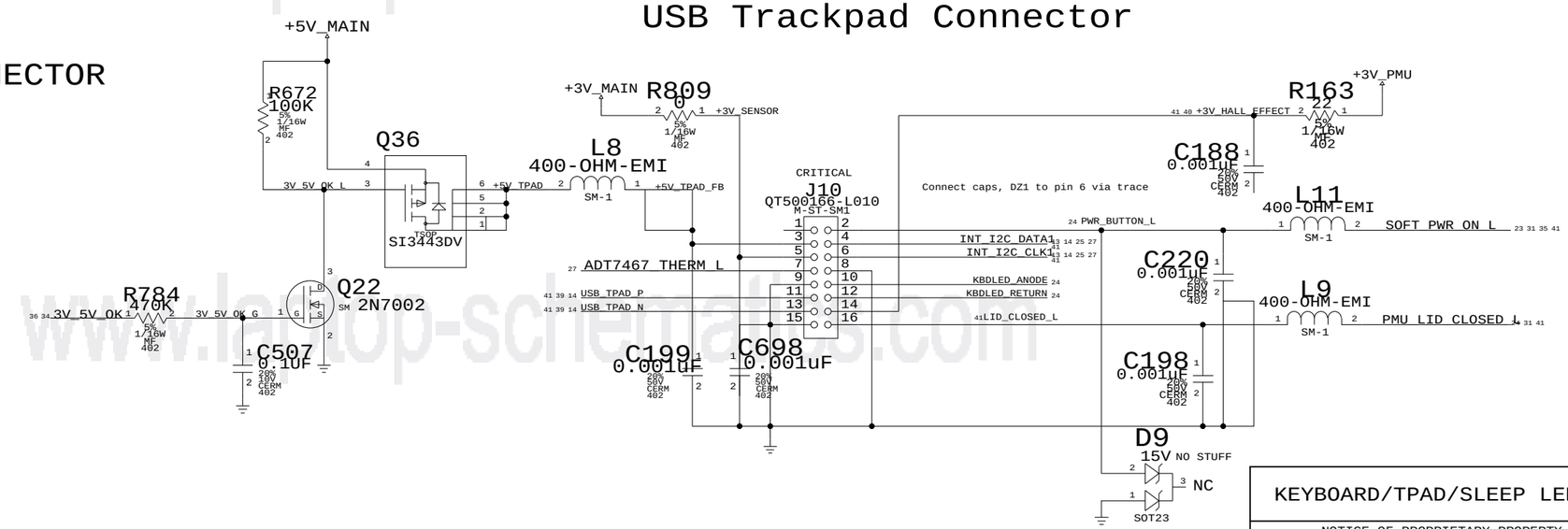
KEYBOARD PULLUPS



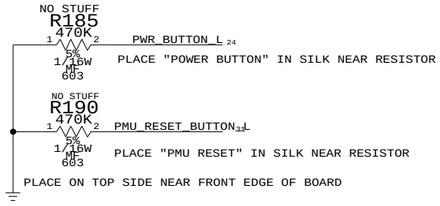
LEFT LIGHT SENSOR CONNECTOR



USB Trackpad Connector



DEBUG HELPERS



KEYBOARD/TPAD/SLEEP LED

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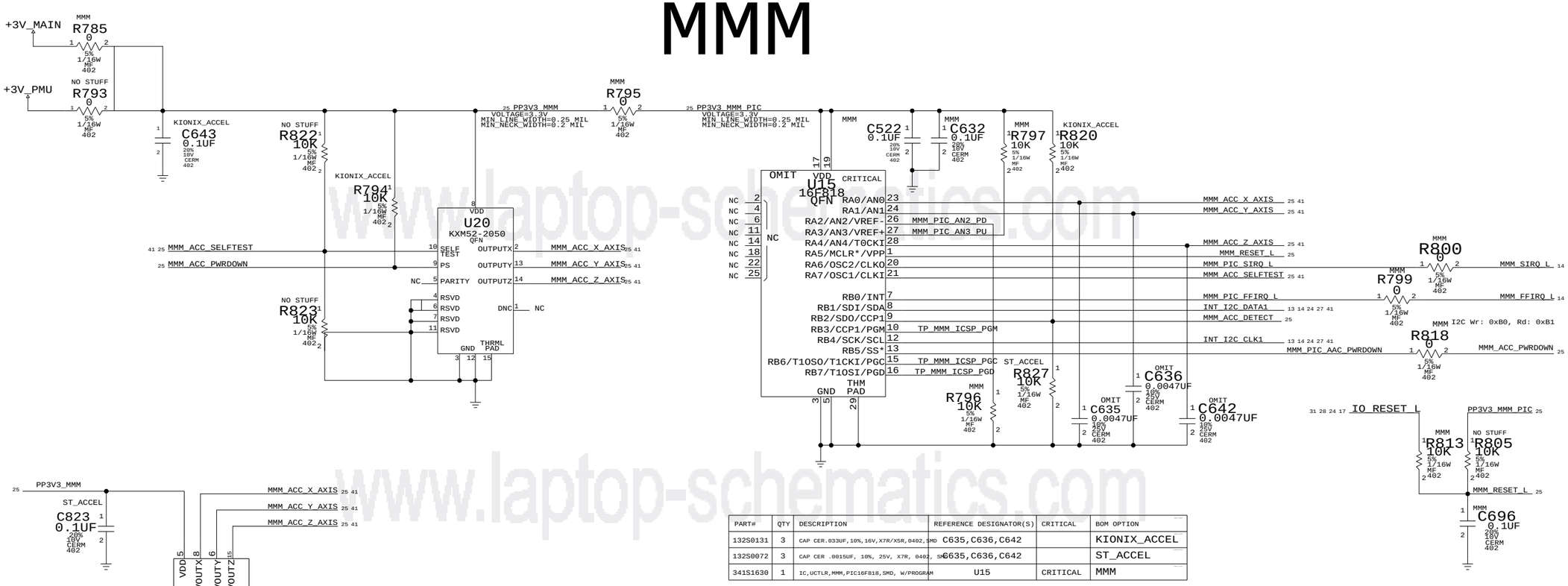
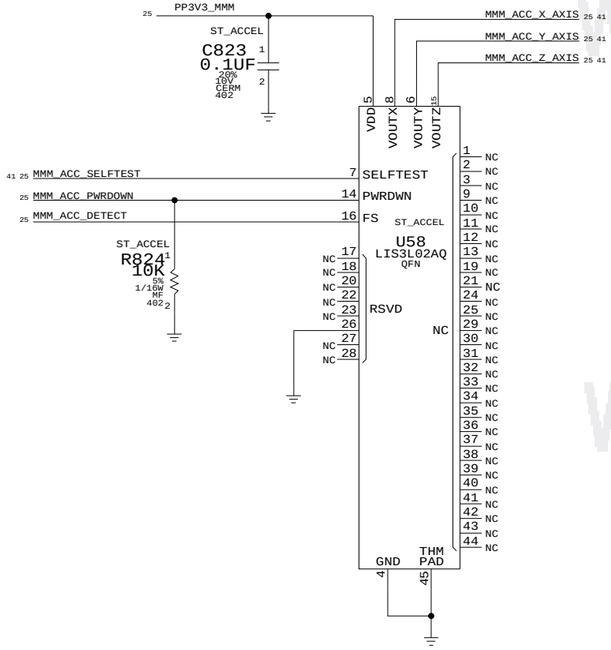
D	051-6680	F
SCALE: NONE	SHT 24 OF 46	

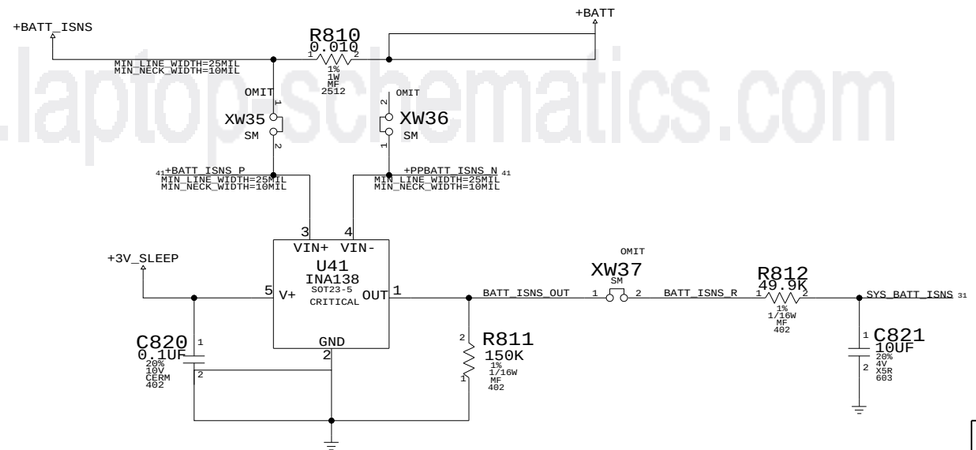
MMM





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	CAP CER.033UF,10%,16V,X7R/X5R,0402,SMD	C635,C636,C642		KIONIX_ACCEL
132S0072	3	CAP CER .0015UF, 10%, 25V, X7R, 0402, SM	C635,C636,C642		ST_ACCEL
341S1630	1	IC,UCTLR,MMM,PIC16F818,SMD, W/PROGRAM	U15	CRITICAL	MMM

BATTERY CURRENT SENSE



MMM & BATTERY CURRENT SENSOR

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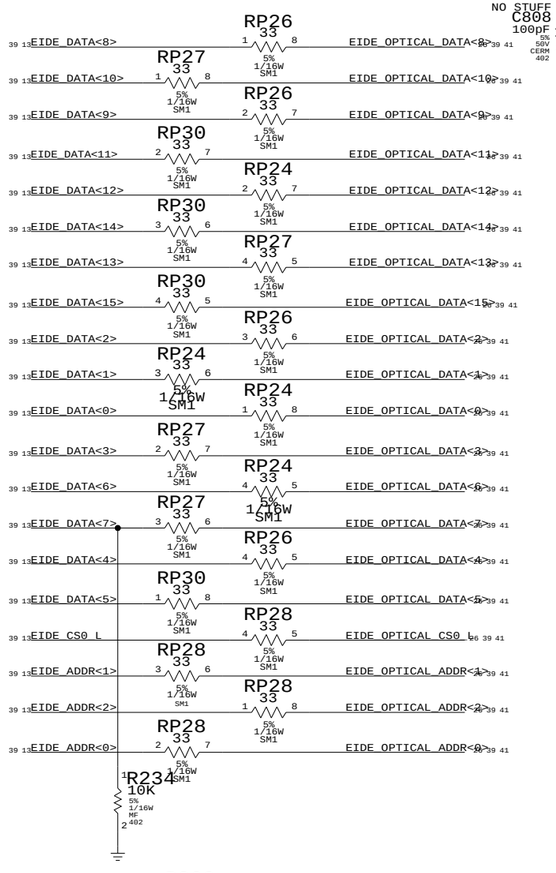
APPLE COMPUTER INC.

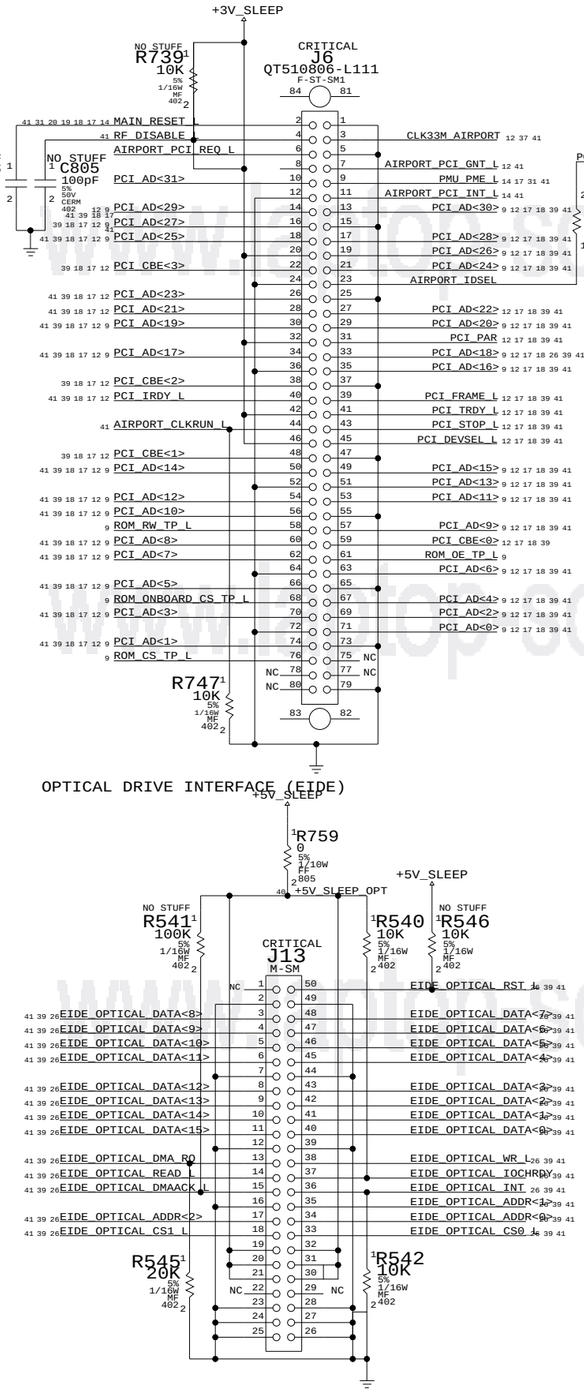
SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 25 OF 46	

WIRELESS INTERFACE

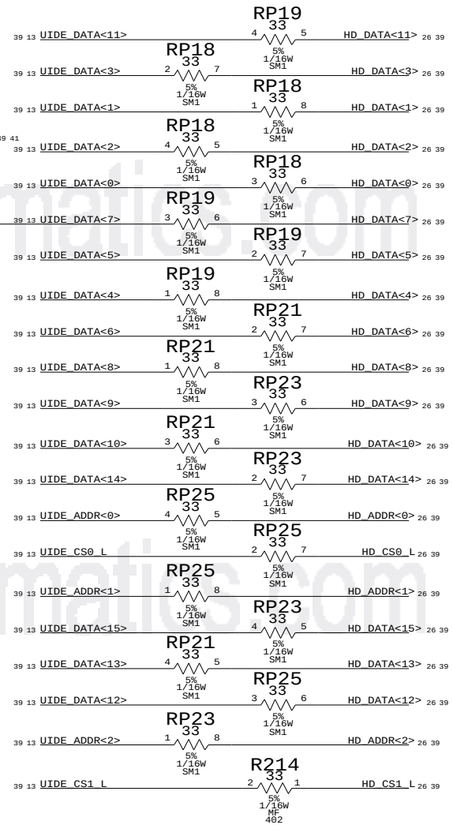
EIDE SERIES TERMINATION
PLACE TERMINATORS NEAR INTREPID



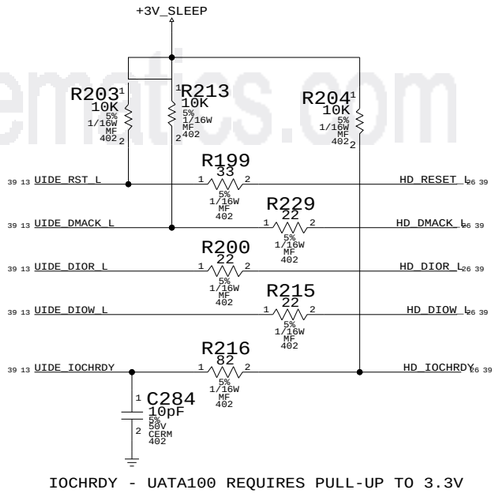
OPTICAL DRIVE INTERFACE (EIDE)



PLACE SERIES R CLOSE TO INTERPID

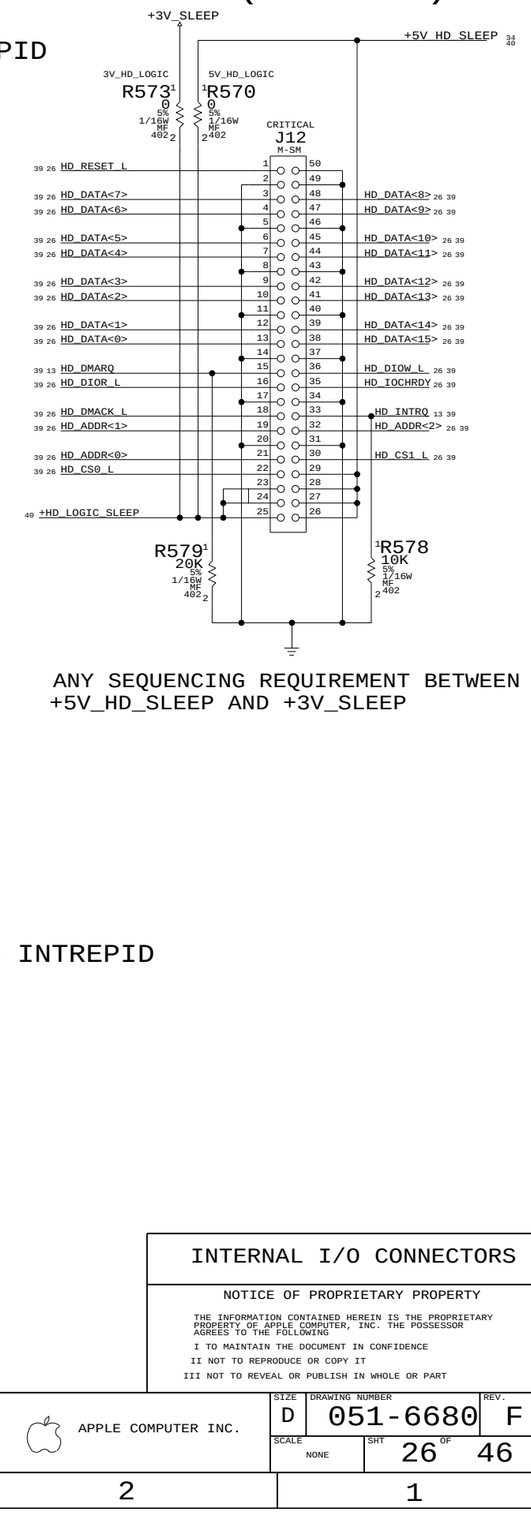


PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

HARD DRIVE INTERFACE (UATA100)



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

+5V_SLEEP

INTERNAL I/O CONNECTORS

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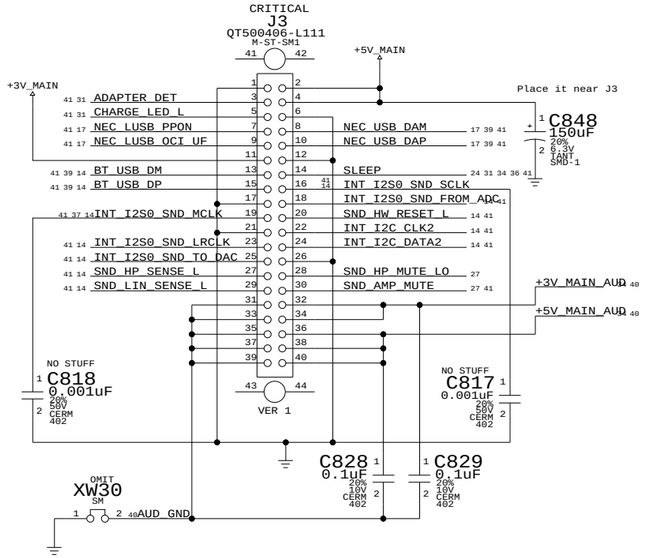
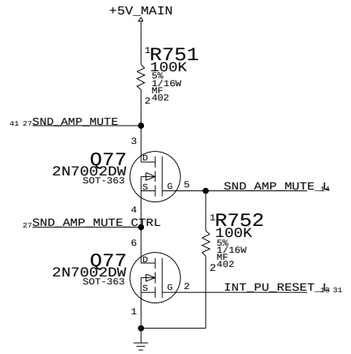
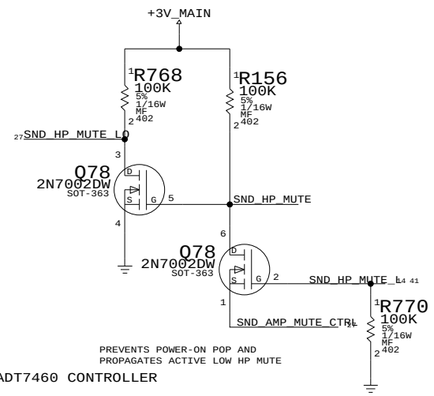
SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 26 OF 46	

LEFT I/O & AUDIO BOARD (LIO)



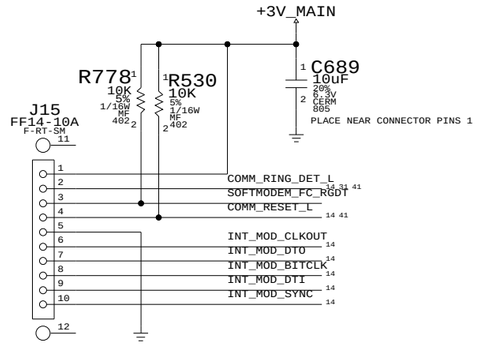


PREVENTS POWER-ON POP AND
GENERATES ACTIVE HIGH SPKR MUTE



PREVENTS POWER-ON POP AND
PROPAGATES ACTIVE LOW HP MUTE

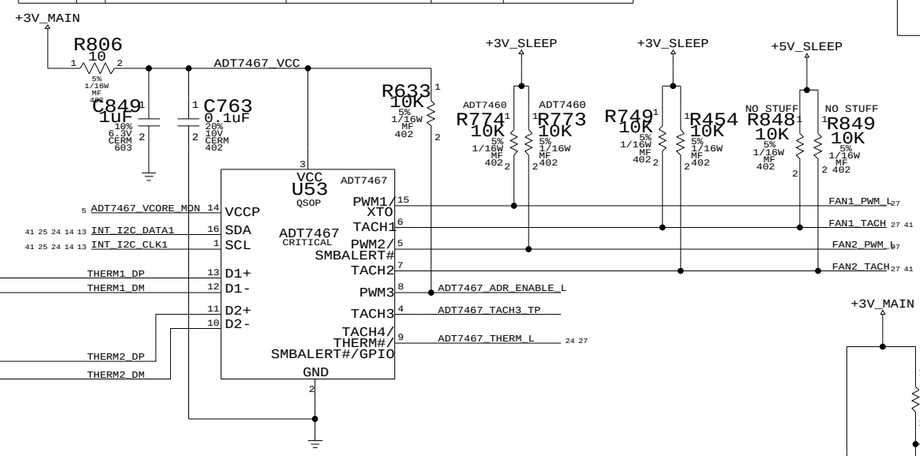
SOFT MODEM CONN



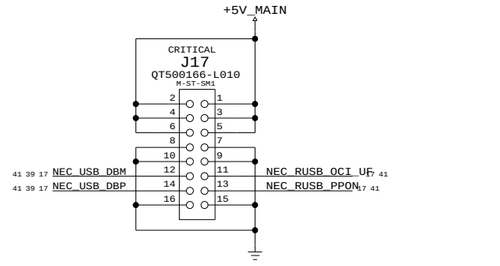
FAN INTERFACE

FAN CONTROLLER

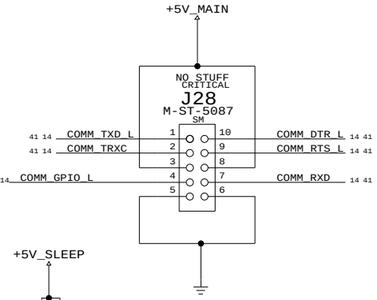
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S0608	1	IC,ADT7460,FAN CTLR,16P QSOP	U53	CRITICAL	ADT7460



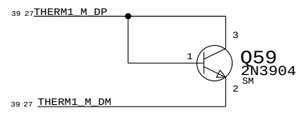
RIGHT USB BOARD



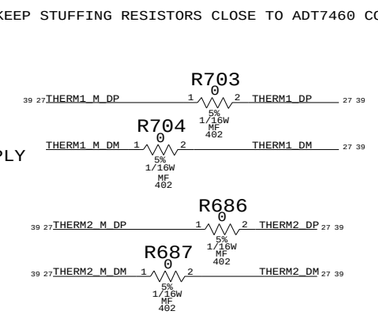
SERIAL DEBUG INTERFACE



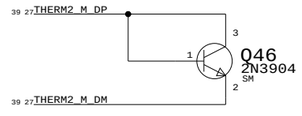
PLACE CLOSE TO CPU
MAIN1



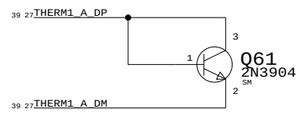
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



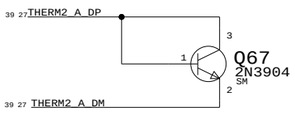
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



PLACE UNDERNEATH UPPER RAM
ALTERNATE1

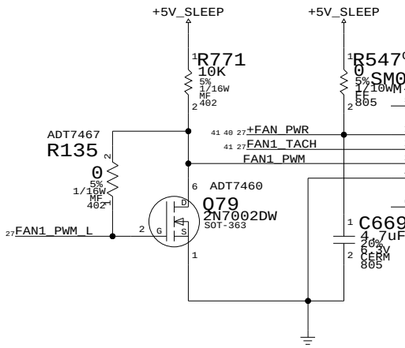


PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2

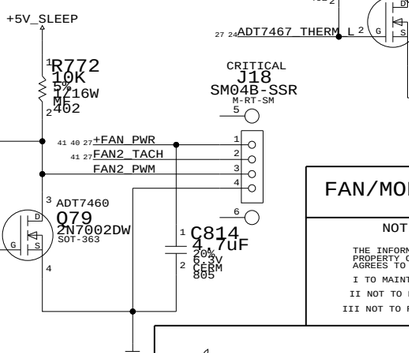


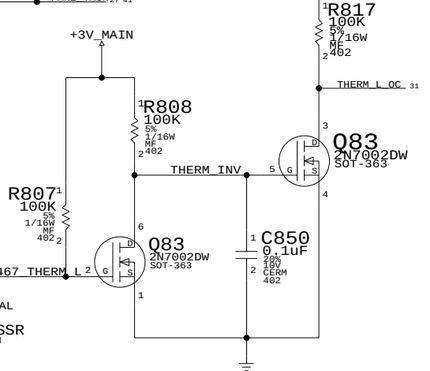
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

CPU FAN



GPU FAN





FAN/MODEM/SOUND/BACKUP BATT.

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 27 OF 46	

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0079	338S0223		U43	ALT FOR 88E1111 B1

+3V_MAIN

C680 10uF 20% 6.3V CERM 805

NO STUFF R513 0 5% 1/16W MF 402

3405_MODE

R507 0 5% 1/16W MF 402

U45 LTC3405 SOT23-6 CRITICAL
VIN, RUN, MODE, GND, SW, VFB

LTC3405_SW

CRITICAL L60 3.3uH SM1

R506 665K 1% 1/16W MF 402 R2A

C675 22pF 5% 50V CERM 402

R504 49.9K 1% 1/16W MF 402 R2B

3405_VFB

C674 10uF 20% 6.3V CERM 805

R503 182K 1% 1/16W MF 402 R1

+1_0V_MARVELL

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R423 0 5% 1/16W MF 402 — 37 13 CLKENET_LINK_TX — 37 CLKENET_PHY_TX
R421 0 5% 1/16W MF 402 — 37 13 CLKENET_LINK_RX — 37 CLKENET_PHY_RX
R445 0 5% 1/16W MF 402 — 37 13 CLKENET_LINK_GBE_REF — 37 CLKENET_PHY_GBE_REF

NO STUFF C851 10pF 5% 50V CERM 402
C852 10pF 5% 50V CERM 402
Keep C851 & C852 Stubs short

U43 88E1111-BDIE BCC

TX_CLK	4		
RX_CLK	2		
125CLK	22		
TXD0	11	39 13 ENET_PHY_TXD<0>	
TXD1	12	39 13 ENET_PHY_TXD<1>	
TXD2	14	39 13 ENET_PHY_TXD<2>	
TXD3	16	39 13 ENET_PHY_TXD<3>	
TXD4	17	39 13 ENET_PHY_TXD<4>	
TXD5	18	39 13 ENET_PHY_TXD<5>	
TXD6	19	39 13 ENET_PHY_TXD<6>	
TXD7	20	39 13 ENET_PHY_TXD<7>	
TX_EN	9	39 13 ENET_PHY_TX_EN	
TX_ER	7	39 13 ENET_PHY_TX_ER	
GTX_CLK	8	37 13 CLKENET_PHY_GTX	
RXD0	95	39 13 ENET_LINK_RXD<0>	
RXD1	92	39 13 ENET_LINK_RXD<1>	
RXD2	93	39 13 ENET_LINK_RXD<2>	
RXD3	91	39 13 ENET_LINK_RXD<3>	
RXD4	90	39 13 ENET_LINK_RXD<4>	
RXD5	89	39 13 ENET_LINK_RXD<5>	
RXD6	87	39 13 ENET_LINK_RXD<6>	
RXD7	86	39 13 ENET_LINK_RXD<7>	
RX_DV	94	39 13 ENET_RX_DV	
RX_ER	3	39 13 ENET_RX_ER	
CRS	84	39 13 ENET_CRS	
COL	83	39 13 ENET_COL	
MDC	25	39 13 ENET_MDC	
MDIO	24	39 13 ENET_MDIO	
INT-/INT+	23	14 ENET_ENERGY_DET	
RESET	28	ENET_RST_L	
COMA	27	ENET_COMA	
S_IN+	82	NC	
S_IN-	81	NC	
S_OUT+	77	NC	
S_OUT-	75	NC	
S_CLK+	79	NC	
S_CLK-	80	NC	
HSDAC+	37	ENET_HSDACP	
HSDAC-	38	ENET_HSDACM	
XTAL1	55	CLK25M_ENET_XIN	
XTAL2	54	CLK25M_ENET_XOUT	
VSSC	53	ENET_VSSC	
GND	97		
CTRL10	51	NC	
DVDD	1, 6, 10, 15, 57, 62, 67, 71, 85		
VDDO	5, 21, 88, 96		
VDDOH	52, 66, 72		
VDDOX	26, 48		
AVDD	32, 35, 36, 40, 45, 78		
MDI0+	29	41 39 MDI_P<0>	
MDI0-	31	41 39 MDI_M<0>	
MDI1+	33	41 39 MDI_P<1>	
MDI1-	34	41 39 MDI_M<1>	
MDI2+	39	41 39 MDI_P<2>	
MDI2-	41	41 39 MDI_M<2>	
MDI3+	42	41 39 MDI_P<3>	
MDI3-	43	41 39 MDI_M<3>	
LED_LINK10	76	LED_LINK10	
LED_LINK100	74	LED_LINK100	
LED_LINK1000	73 NC		
LED_DUPLEX	70 NC		
LED_RX	69	LED_RX_SPN	
LED_TX	68 NC		
CONFIG0	65	(000)	
CONFIG1	64	(000)	
CONFIG2	63	(111)	
CONFIG3	61	(110)	
CONFIG4	60	(111)	
CONFIG5	59	(101)	
CONFIG6	58	(000)	
TDI	44		
TDO	50	JTAG_ASIC_TDO	41
TCK	49	JTAG_ASIC_TCK	13 41
TMS	46	JTAG_ASIC_TMS	13 41
TRST	47	JTAG_ASIC_TRST_L	41
RSET	30	ENET_RSET	
SEL_OSC	56 NC		
SEL_2.5V	13		

SEE CONFIG TABLES (BELOW)

C611 2.2uF 10% 10V CERM 805

D15 1N914 SOT23

Q32 2N7002DW SOT-363
Q32 2N7002DW SOT-363

32 31 30 AC_IN
36 35 34 21 18 SLEEP_L_LS5

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

14 INT_ENET_RST_L — R422 1K 5% 1/16W MF 402
31 25 24 17 IO_RESET_L

40 28 +2_5V_MARVELL

R431 10K 5% 1/16W MF 402
R430 10K 5% 1/16W MF 402
R432 1.5K 5% 1/16W MF 402

PUT CRYSTAL CIRCUIT CLOSE TO PHY

NO STUFF R425 20K 5% 1/16W MF 402

R441 0 5% 1/16W MF 402

CRITICAL Y5 SM-3 25.0000M
CLK25M_XTAL_IN

C604 27pF 5% 50V CERM 402
C624 27pF 5% 50V CERM 402

Y6 LOAD CAPACITANCE IS 16PF

NO STUFF R424 49.9 1% 1/16W MF 402
R429 49.9 1% 1/16W MF 402
R428 10K 5% 1/16W MF 402
R427 4.99K 1% 1/16W MF 402

C594 0.1uF 20% 10V CERM 402
C601 0.01uF 20% 10V CERM 402
C608 0.1uF 20% 10V CERM 402
C619 0.01uF 20% 10V CERM 402
C603 0.1uF 20% 10V CERM 402
C599 0.01uF 20% 10V CERM 402

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

C597 0.1uF 20% 10V CERM 402
C612 0.01uF 20% 10V CERM 402
C623 0.1uF 20% 10V CERM 402
C600 0.01uF 20% 10V CERM 402
C598 0.1uF 20% 10V CERM 402
C595 10uF 20% 6.3V CERM 805

40 28 +2_5V_MARVELL

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

C614 0.1uF 20% 10V CERM 402
C616 0.1uF 20% 10V CERM 402
C618 0.1uF 20% 10V CERM 402
C602 0.01uF 20% 10V CERM 402
C592 10uF 20% 6.3V CERM 805

40 +2_5V_MARVELL_AVDD — L35 FERR-EMI-600-OHM SM

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

R433 49.9 1% 1/16W MF 402
R435 49.9 1% 1/16W MF 402
R437 49.9 1% 1/16W MF 402
R439 49.9 1% 1/16W MF 402

R434 49.9 1% 1/16W MF 402
R436 49.9 1% 1/16W MF 402
R438 49.9 1% 1/16W MF 402
R440 49.9 1% 1/16W MF 402

MDI0_PD MDI1_PD MDI2_PD MDI3_PD

C622 0.01uF 20% 10V CERM 402
C613 0.01uF 20% 10V CERM 402
C615 0.01uF 20% 10V CERM 402
C617 0.01uF 20% 10V CERM 402

PLACE RESISTORS CLOSE TO PHY

+2_5V_MAIN

R442 0 5% 1/10W FF 805

C646 0.1uF 20% 10V CERM 402
C648 0.1uF 20% 10V CERM 402
C645 0.1uF 20% 10V CERM 402
C647 0.1uF 20% 10V CERM 402

PLACE CAPS AT CONNECTOR PINS 5 & 6

R814 0 5% 1/10W FF 805

+2_5V_MARVELL_CONN

J23 MJ-R0076 F-RT-TH

PRIMARY
13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12
14
RJ45 CHIP SIDE

1CT:1CT — 75 OHM
1CT:1CT — 75 OHM
1CT:1CT — 75 OHM
1CT:1CT — 75 OHM

SECONDARY
J1
J2
J3
J4
J5
J6
J7
J8
RJ45 CABLE SIDE

CHGND1

SHIELD 1000PF, 2000V

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6680 | REV. F
SCALE NONE | SHT 28 OF 46

165MA MAX LOAD

D25 SC-59 SDM20E40C

U37 LM2594 SM — CRITICAL — VIN, FB, VOUT, GND ON/OFF

L59 220uH SM-3

C665 10uF 20% 50V CERM 2320

C670 100uF 20% 6.3V POLY CASE-B-3528

D16 SM MBR0540

L34 400-OHM-EMI SM-1

R414 10 5% 1/16W MF 603

C587 0.1uF 20% 10V CERM 402

C684 0.1uF 20% 10V CERM 402

C585 2.2uF 20% 10V CERM 805

PHY PINS 72,76

C588 2.2uF 20% 10V CERM 805

C589 0.1uF 20% 10V CERM 402

PHY PIN 64

U44 LTC1761ES5-BYP SOT-23-1 SYM_VER2 — CRITICAL — IN, OUT, BYP, ADJ, GND

VOUT = 1.22*(1+R2/R1)+ IADJ*R2
IADJ = 30NA AT 25C

R418 1 5% 1/16W MF 603

R426 1 5% 1/16W MF 603

R420 1 5% 1/16W MF 603

R413 1 5% 1/16W MF 603

C593 1uF 20% 10V CERM 603

C606 1uF 20% 10V CERM 603

C596 1uF 20% 10V CERM 603

C584 1uF 20% 10V CERM 603

PHY PIN 61 · PHY PIN 59 · PHY PIN 40 · PHY PIN 21

R415 3.3 5% 1/16W MF 603

R416 3.3 5% 1/16W MF 603

C586 1uF 20% 10V CERM 603

C678 1uF 20% 10V CERM 603

PHY PIN 25 · PHY PIN 28

R419 1 5% 1/16W MF 603

R417 1 5% 1/16W MF 603

C591 0.1uF 20% 10V CERM 402

C590 0.1uF 20% 10V CERM 402

PHY PIN 38

R519 22 5% 1/16W MF 402 — FW_PHY_CNTL<0> — FW_LINK_CNTL<0>

R520 22 5% 1/16W MF 402 — FW_PHY_CNTL<1> — FW_LINK_CNTL<1>

R518 22 5% 1/16W MF 402 — CLKFW_PHY_PCLK — CLKFW_LINK_PCLK

C681 10uF 20% 6.3V CERM 805

C683 0.1uF 20% 10V CERM 402

C677 0.1uF 20% 10V CERM 402

C676 0.1uF 20% 10V CERM 402

C682 0.1uF 20% 10V CERM 402

PHY PINS 4,14

U38 LT1962-ADJ MSOP — CRITICAL — IN, NC, NC, SHDN, OUT, ADJ, BYP, GND

C621 0.01uF 10% 16V CERM 402

R443 16.2K 1% 1/16W MF 402 R2

C620 10uF 20% 6.3V CERM 805

R444 27.4K 1% 1/16W MF 402 R1

C625 2.2uF 20% 10V CERM 805

R505 1K 5% 1/16W MF 402

R509 1K 5% 1/16W MF 402

R497 1K 5% 1/16W MF 402

R508 0 5% 1/16W MF 402

R515 1K 5% 1/16W MF 402

R516 10K 5% 1/16W MF 402

U36 TSB81BA3A PQFP (SYM_VER1) — CRITICAL — SN0201029PFP

AVDD 3.3 · DVDD 1.8 · DVDD 3.3 · PLL VDD 1.8 · PLL VDD 3.3 · AGND · DGND · PLLGND · PAD

DS0, DS1, LCLK, LPS, LREQ, PC0, PC1, PC2, PD, BMODE, CPS, D0–D7, RESETZ, SE, SM, TESTM, VREG_PD, THRML, PCLK, PINT, CNA, CTL0, CTL1, C/LKON, TPA0+/-, TPA1+/-, TPA2+/-, TPB0+/-, TPB1+/-, TPB2+/-, TPBIAS0, TPBIAS1, TPBIAS2, XI, XO, R0, R1, TX0, RX0

1MA (MAX) BUS HOLDERS

PWR CLASS = 100
(MAY PROVIDE POWER, OR MAY REQUIRE UP TO 5W)
(PC0 IS MSB, PC2 IS LSB)

R502 402K 1% 1/16W MF 402

RP38 22 5% 1/16W SM1 — RP37 22 5% 1/16W SM1

R510 47 5% 1/16W MF 402

R511 100 5% 1/16W MF 402

R512 6.34K 1% 1/16W MF 402

C583 0.22uF 20% 6.3V CERM 402

CRITICAL — VCC, G2, 98.304MHZ OSC SM-A, OUT, OE, GND

NO STUFF R412 100K 5% 1/16W MF 402

R488 56.2 1% 1/16W MF 402 · R487 56.2 1% 1/16W MF 402 · C605C607 1uF 20% 10V CERM 603 · 1uF 20% 10V CERM 603 · R492 56.2 1% 1/16W MF 402 · R491 56.2 1% 1/16W MF 402

R494 56.2 1% 1/16W MF 402 · R493 56.2 1% 1/16W MF 402 · R490 56.2 1% 1/16W MF 402 · R489 56.2 1% 1/16W MF 402

C673 220pF 5% 25V CERM 402 · R499 4.99K 1% 1/16W MF 402 · C672 220pF 5% 25V CERM 402 · R498 4.99K 1% 1/16W MF 402

FW_TPB0 · FW_TPB1

C679 0.22uF 20% 6.3V CERM 402

R514 1K 5% 1/16W MF 402

R517 1K 5% 1/16W MF 402

R500 470 5% 1/16W MF 402

R501 0 5% 1/16W MF 402

R486 1K 5% 1/16W MF 402

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

DSx Strap Options
0 = Bilingual port
1 = A-only port

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052		G2	Alt. for Siward Part

APPLE COMPUTER INC.

SIZE D · DRAWING NUMBER 051-6680 · REV. F · SCALE NONE · SHT 29 OF 46

PORT POWER SWITCH

+PBUS
F3 1.5A-24V MINISMDC
+FW_PBUS
CRITICAL Q34 NDS9407 SOI
+FW_SW
CRITICAL D24 SMB B340B
+FW_PWR_OR
R448 470K 5% 1/16W MF 402
C639 0.01UF 20% 16V CERM 402
FW_GATE_EN
+3V_PMU
R447 100K 5% 1/16W MF 402
DP6 BAS16TW SOT-363
POWER_UP
Q33 2N7002DW SOT-363
PMU_POWER_UP_L
R461 330K 5% 1/16W MF 402
FW_GATE_EN_RC
Q33 2N7002DW SOT-363
FW_POWER_UP
R803 0 5% 1/16W MF 402
DCDC_EN
DCDC_EN_CTRL
DP6 BAS16TW SOT-363
R446 10K 5% 1/16W MF 402
AC_IN
AC_IN_FW_CNTL
DP6 BAS16TW SOT-363
R777 470K 5% 1/16W MF 402

ENABLES PORT POWER WHEN
MACHINE IS RUNNING OR WHEN ASLEEP ON AC

+3V_FW
NO STUFF C822 0.1UF 20% 10V CERM 402
R451 10K 5% 1/16W MF 402
+3V_FW_ESD_ITM
L39 400-OHM-EMI SM-1
C630 0.1UF 20% 10V CERM 402
C637 0.001UF 20% 50V CERM 402
D21 1N5227B SOT23
C638 0.01UF 20% 16V CERM 402
+3V_FW_ESD
D20 BAV99DW SOT-363
D23 BAV99DW SOT-363
D20 BAV99DW SOT-363
D23 BAV99DW SOT-363
C633 0.01UF 20% 16V CERM 402

PORT 0
1394a/b
(BILINGUAL)
514S0058

L76 CRITICAL 90-OHM-300mA 2012H SYM_VER-1
L77 CRITICAL 90-OHM-300mA 2012H SYM_VER-1
FW_TPO0P
FW_TPO0N
FW_TPI0P
FW_TPI0N
(AREF)
(BREF)
(TPI0R)
FW_VGND0
FW_VP0
CRITICAL J20 1394B F-RT-SM
INT-SHIELD
TPA
TPA(R)
TPA*
VG
SC
NC
VP
TPB
TPB(R)
TPB*
INT-SHIELD
C650 0.01UF 20% 16V CERM 402
CHGND1

L51 FERR-250-OHM SM

R465 1M 5% 1/16W MF 402
C649 0.1uF 20% 50V CERM 805
NO STUFF C652 0.01UF 20% 16V CERM 402
R466 0 5% 1/10W MF 805
NO STUFF C651 0.01UF 20% 16V CERM 402
CHGND1

AREF NEEDS TO BE ISOLATED FROM
ALL LOCAL GROUNDS PER 1394B SPEC
SO WHEN A BILINGUAL DEVICE IS
PLUGGED TO A BETA-ONLY DEVICE,
THERE'S NO DC PATH BETWEEN THEM
(TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO
LOGIC GROUND FOR SPEED SIGNALING
AND CONNECTION DETECTION CURRENTS
PER 1394b V1.33

R837 0 5% 1/16W MF 603
+FW_PWR_OR_F
PLACE NEAR D24
Q37 NO STUFF SI2319DS SOT23
NO STUFF R829 470K 5% 1/16W MF 402
+FW_PWR_OR_GATE
NO STUFF R830 470K 5% 1/16W MF 402
+FW_PWR_OR_GATE_L
NO STUFF R831 649K 1% 1/16W MF 402
NO STUFF Q73 2N7002 SM
+FW_PWR_CTRL
NO STUFF C824 1UF 20% 10V CERM 603
NO STUFF D35 SM MBR0540
+2_5V_REG_F
NO STUFF C825 0.1UF 20% 10V CERM 402
NO STUFF U59 LMC7211 SM
+3V_FW_ESD_R
NO STUFF R834 10K 5% 1/16W MF 402
NO STUFF R835 102K 1% 1/16W MF 402
2.5V REG
NO STUFF R836 332K 1% 1/16W MF 402
PLACE NEAR D23
NO STUFF C826 0.01UF 20% 16V CERM 402
NO STUFF R833 604K 1% 1/16W MF 402

2.5V REG: 2.50V - 2.15V
200MS - 500MS

F1 1.5AMP-33V SM
+FW_PWR1
L58 FERR-250-OHM SM

+3V_FW_ESD
D22 BAV99DW SOT-363
D18 BAV99DW SOT-363
D22 BAV99DW SOT-363
D18 BAV99DW SOT-363
C640 0.01UF 20% 16V CERM 402
C644 0.01UF 20% 16V CERM 402

PORT 1
1394a ONLY
514-0057

L52 260-OHM-330MA SM1 SYM_VER-2
L48 260-OHM-330MA SM1 SYM_VER-2
FW_TPA1P
FW_TPA1N
FW_TPB1P
FW_TPB1N
FW_TPO1P
FW_TPO1N
FW_TPI1P
FW_TPI1N
FW_VP1
FW_VGND1
CRITICAL J24 1394A F-RT-TH
TPO
TPO#
TPI
TPI#
VP
VGND

CLEAR OUT ALL PLANES UNDER TRANSFORMERS

R471 0 5% 1/10W MF 805
C662C666 0.01uF 0.01UF 20% 16V CERM 402
CHGND1

R816 0 5% 1/16W MF 402 EMI
CHGND1

FIREWIRE PORTS

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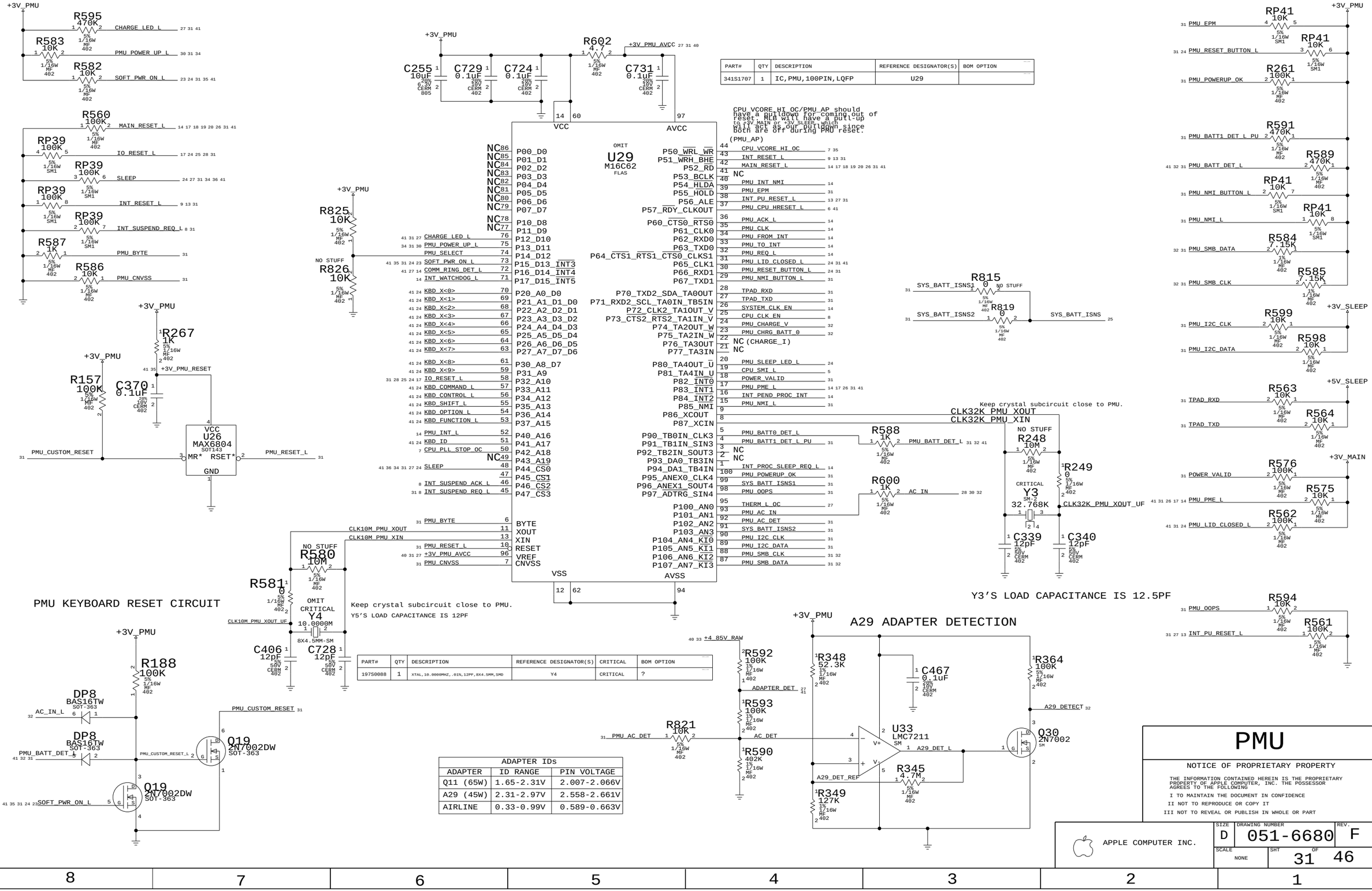
SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 30 OF 46	


+3V_PMU
R595 470K CHARGE_LED_L 27 31 41
R583 10K
R582 10K
PMU_POWER_UP_L 30 31 34
SOFT_PWR_ON_L 23 24 31 35 41
R560 100K MAIN_RESET_L 14 17 18 19 20 26 31 41
RP39 100K IO_RESET_L 17 24 25 28 31
RP39 100K SLEEP 24 27 31 34 36 41
RP39 100K INT_RESET_L 9 13 31
RP39 100K INT_SUSPEND_REQ_L 8 31
R587 1K PMU_BYTE 31
R586 10K PMU_CNVSS 31
+3V_PMU_AVCC 27 31 40
C255 10uF 20% 6.3V CERM 805
C729 0.1uF 20% 10V CERM 402
C724 0.1uF 20% 10V CERM 402
C731 0.1uF 20% 10V CERM 402
R602 4.7
VCC
AVCC
VSS
AVSS
U29 M16C62 FLAS
OMIT
NC86 P00_D0
NC85 P01_D1
NC84 P02_D2
NC83 P03_D3
NC82 P04_D4
NC81 P05_D5
NC80 P06_D6
NC79 P07_D7
NC78 P10_D8
NC77 P11_D9
P12_D10
P13_D11
P14_D12
P15_D13_INT3
P16_D14_INT4
P17_D15_INT5
P50_WRL_WR
P51_WRH_BHE
P52_RD
P53_BCLK
P54_HLDA
P55_HOLD
P56_ALE
P57_RDY_CLKOUT
P60_CTS0_RTS0
P61_CLK0
P62_RXD0
P63_TXD0
P64_CTS1_RTS1_CTS0_CLKS1
P65_CLK1
P66_RXD1
P67_TXD1
P70_TXD2_SDA_TA0OUT
P71_RXD2_SCL_TA0IN_TB5IN
P72_CLK2_TA1OUT_V
P73_CTS2_RTS2_TA1IN_V
P74_TA2OUT_W
P75_TA2IN_W
P76_TA3OUT
P77_TA3IN
P80_TA4OUT_U
P81_TA4IN_U
P82_INT0
P83_INT1
P84_INT2
P85_NMI
P86_XCOUT
P87_XCIN
P90_TB0IN_CLK3
P91_TB1IN_SIN3
P92_TB2IN_SOUT3
P93_DA0_TB3IN
P94_DA1_TB4IN
P95_ANEX0_CLK4
P96_ANEX1_SOUT4
P97_ADTRG_SIN4
P100_AN0
P101_AN1
P102_AN2
P103_AN3
P104_AN4_KI0
P105_AN5_KI1
P106_AN6_KI2
P107_AN7_KI3
P30_A8_D7
P31_A9
P32_A10
P33_A11
P34_A12
P35_A13
P36_A14
P37_A15
P40_A16
P41_A17
P42_A18
P43_A19
P44_CS0
P45_CS1
P46_CS2
P47_CS3
BYTE
XOUT
XIN
RESET
VREF
CNVSS
CPU_VCORE_HI_OC 7 35
INT_RESET_L 9 13 31
MAIN_RESET_L 14 17 18 19 20 26 31 41
PMU_INT_NMI 14
PMU_EPM 31
INT_PU_RESET_L 13 27 31
PMU_CPU_HRESET_L 6 41
PMU_ACK_L 14
PMU_CLK 14
PMU_FROM_INT 14
PMU_TO_INT 14
PMU_REQ_L 14
PMU_LID_CLOSED_L 24 31 41
PMU_RESET_BUTTON_L 24 31
PMU_NMI_BUTTON_L 31
TPAD_RXD 31
TPAD_TXD 31
SYSTEM_CLK_EN 14
CPU_CLK_EN 8
PMU_CHARGE_V 32
PMU_CHRG_BATT_0 32
PMU_SLEEP_LED_L 24
CPU_SMI_L 5
POWER_VALID 31
PMU_PME_L 14 17 26 31 41
INT_PEND_PROC_INT 14
PMU_NMI_L 31
PMU_BATT0_DET_L
PMU_BATT1_DET_L_PU 31
PMU_BATT_DET_L 31 32 41
PMU_POWERUP_OK 31
SYS_BATT_ISNS1 31
SYS_BATT_ISNS2 31
PMU_OOPS 31
PMU_I2C_CLK 31
PMU_I2C_DATA 31
PMU_SMB_CLK 31 32
PMU_SMB_DATA 31 32
AC_IN 28 30 32
THERM_L_OC 27
PMU_AC_IN 31
PMU_AC_DET 31
SYS_BATT_ISNS2 31
PMU_I2C_CLK 31
PMU_I2C_DATA 31
CLK10M_PMU_XOUT 11
CLK10M_PMU_XIN 13
PMU_RESET_L 10
+3V_PMU_AVCC 96
PMU_CNVSS 7
PMU_BYTE 6
CHARGE_LED_L 76
PMU_POWER_UP_L 75
PMU_SELECT 74
SOFT_PWR_ON_L 73
COMM_RING_DET_L 72
INT_WATCHDOG_L 71
KBD_X<0> 70
KBD_X<1> 69
KBD_X<2> 68
KBD_X<3> 67
KBD_X<4> 66
KBD_X<5> 65
KBD_X<6> 64
KBD_X<7> 63
KBD_X<8> 61
KBD_X<9> 59
IO_RESET_L 58
KBD_COMMAND_L 57
KBD_CONTROL_L 56
KBD_SHIFT_L 55
KBD_OPTION_L 54
KBD_FUNCTION_L 53
PMU_INT_L 52
KBD_ID 51
CPU_PLL_STOP_OC 50
SLEEP 48
INT_SUSPEND_ACK_L 46
INT_SUSPEND_REQ_L 45
CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. HLB will have a pull-up to +3V_MAIN or +3V_SLEEP which will act as our pulldown since both are off during PMU reset.
Keep crystal subcircuit close to PMU.
Y5'S LOAD CAPACITANCE IS 12PF
PART# 197S0088 QTY 1 DESCRIPTION XTAL,10.0000MHZ,.01%,12PF,8X4.5MM,SMD REFERENCE DESIGNATOR(S) Y4 CRITICAL CRITICAL BOM OPTION ?
PART# 341S1707 QTY 1 DESCRIPTION IC,PMU,100PIN,LQFP REFERENCE DESIGNATOR(S) U29 BOM OPTION
R825 10K NO STUFF
R826 10K
R580 10M NO STUFF
R581 0 OMIT
Y4 CRITICAL 10.0000M 8X4.5MM-SM
C406 12pF
C728 12pF
R267 1K
R157 100K
C370 0.1uF
PMU_CUSTOM_RESET
PMU_RESET_L
VCC
U26 MAX6804 SOT143
MR* RSET*
GND
PMU KEYBOARD RESET CIRCUIT
R188 100K
DP8 BAS16TW SOT-363
AC_IN_L
PMU_BATT_DET_L
SOFT_PWR_ON_L
PMU_CUSTOM_RESET_L
Q19 2N7002DW SOT-363
R815 0 NO STUFF
R819 0
SYS_BATT_ISNS
R588 1K
R600 1K
Keep crystal subcircuit close to PMU.
CLK32K_PMU_XOUT
CLK32K_PMU_XIN
R248 10M NO STUFF
R249 0
CRITICAL Y3 SM-2 32.768K
CLK32K_PMU_XOUT_UF
C339 12pF
C340 12pF
Y3'S LOAD CAPACITANCE IS 12.5PF
ADAPTER IDs
ADAPTER | ID RANGE | PIN VOLTAGE
Q11 (65W) | 1.65-2.31V | 2.007-2.066V
A29 (45W) | 2.31-2.97V | 2.558-2.661V
AIRLINE | 0.33-0.99V | 0.589-0.663V
A29 ADAPTER DETECTION
+4.85V_RAW
R592 100K
ADAPTER_DET
R593 100K
R590 402K
R821 10K
PMU_AC_DET
R348 52.3K
R349 127K
C467 0.1uF
R364 100K
A29_DETECT
A29_DET_L
A29_DET_REF
U33 LMC7211 SM
R345 4.7M
Q30 2N7002
RP41 10K PMU_EPM
RP41 10K PMU_RESET_BUTTON_L
R261 100K PMU_POWERUP_OK
R591 470K PMU_BATT1_DET_L_PU
R589 470K PMU_BATT_DET_L
RP41 10K PMU_NMI_BUTTON_L
RP41 10K PMU_NMI_L
R584 7.15K PMU_SMB_DATA
R585 7.15K PMU_SMB_CLK
R599 10K PMU_I2C_CLK
R598 10K PMU_I2C_DATA
R563 10K TPAD_RXD
R564 10K TPAD_TXD
R576 100K POWER_VALID
R575 10K PMU_PME_L
R562 100K PMU_LID_CLOSED_L
R594 10K PMU_OOPS
R561 100K INT_PU_RESET_L
+3V_SLEEP
+5V_SLEEP
+3V_MAIN
PMU
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APPLE COMPUTER INC.
SIZE D DRAWING NUMBER 051-6680 REV. F
SCALE NONE SHT 31 OF 46

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL
J27
87438-0433
M-RT-SM

DC INRUSH LIMITER

BACKFEED PROTECTION

+PBUS CURRENT LIMIT

BATTERY SWITCH-OVER CIRCUIT

PLACE R383 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

PLACE U24 NEXT TO R382

GREATER THAN 13.1V DETECT

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

BATTERY CONNECTOR

CRITICAL
J26
87438-0833
M-RT-SM

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

BATTERY CHARGER

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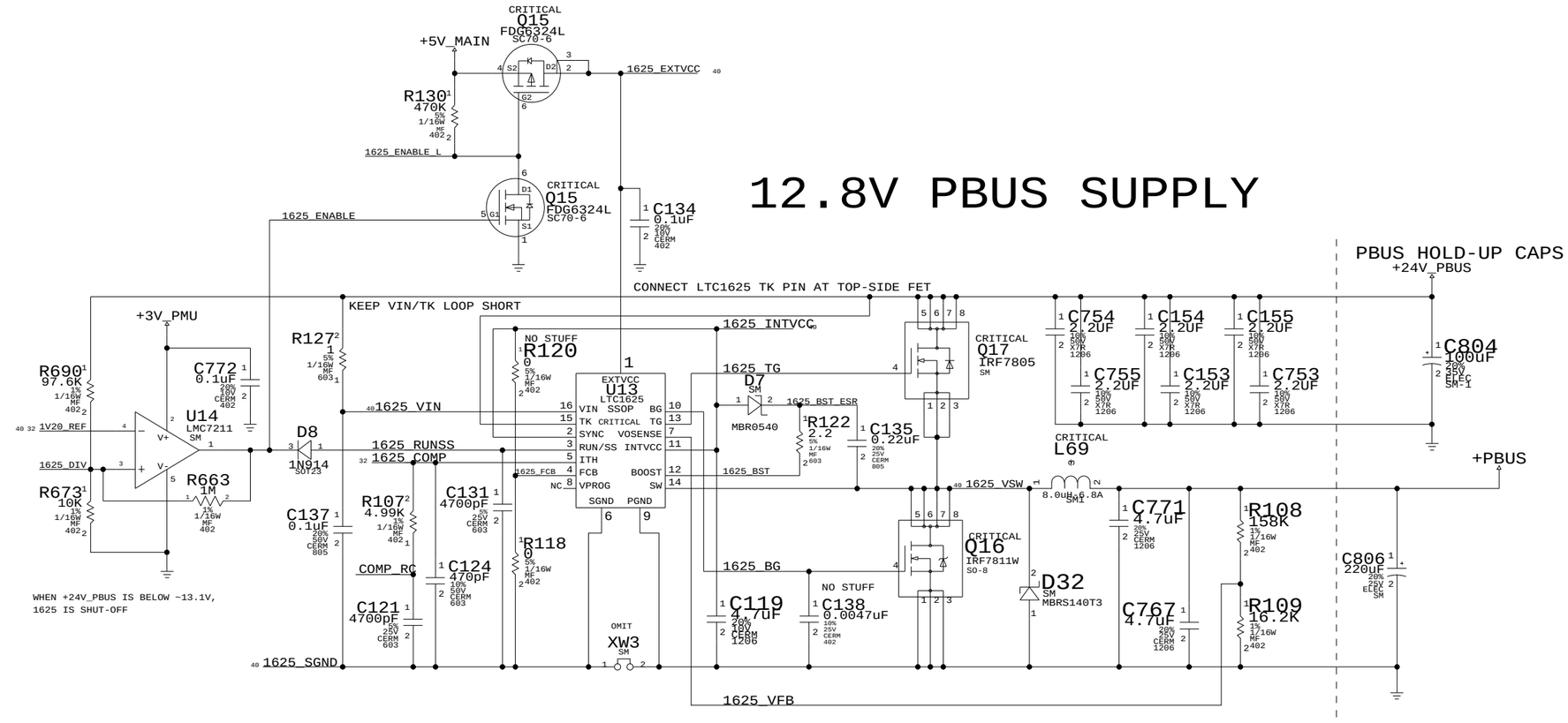
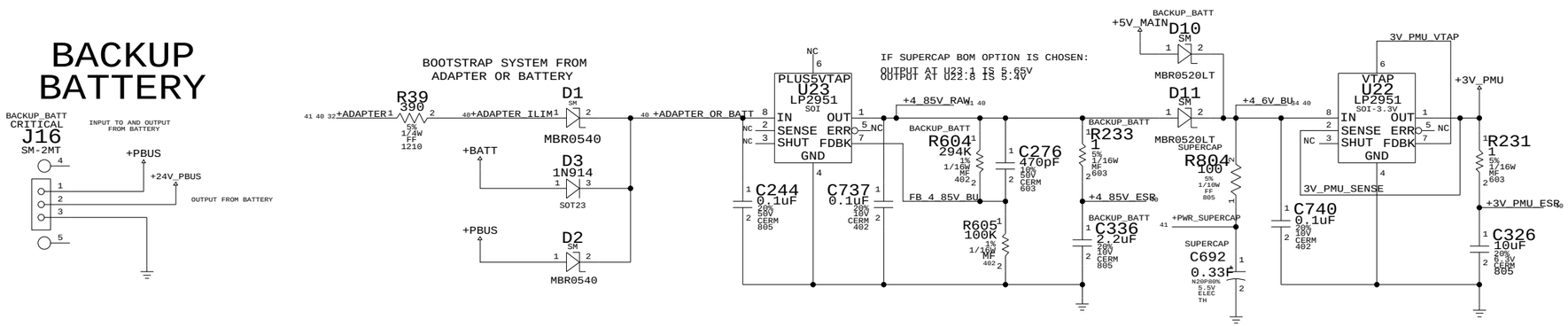
SIZE	DRAWING NUMBER	REV.
D	051-6680	F

SCALE	SHT	OF
NONE	32	46

12.8V PBUS SUPPLY



PMU SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S3575	1	RES,MF,1/16W,357K OHM,1%,0402,SMD	R604	?	SUPERCAP

12.8V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 33 OF 46	

3.3V/5V MAIN SUPPLY

+24V_PBUS

+5V_MAIN

+3V_MAIN

+5V_MAIN_AUD

+3V_MAIN_AUD

5V_RSNS

3V_RSNS

3707_INTVCC

5V_TG

5V_BOOST_ESR

5V_BOOST

5V_SW

5V_BG

3V_TG

3V_BOOST_ESR

3V_BOOST

3V_SW

3V_BG

5V_SNSP

5V_SNSM

3V_SNSP

3V_SNSM

5V_VOSNS

5V_ITH

5V_RUNSS

3V_VOSNS

3V_ITH

3V_RUNSS

3707_FSET

3707_FCB

3707_STBY

3707_SGND

5V_ITH_RC

3V_ITH_RC

5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L

3V START TO TURN ON ~25MS AFTER DCDC_EN_L

DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN

POWERDOWN DELAY IS AROUND 4MS-15.6MS

DISTRIBUTE CAPS ALONG TOP EDGE AND FAN CUT-OUT

DISTRIBUTE CAPS ALONG TOP EDGE AND FAN CUT-OUT

+4_6V_BU

DCDC_EN_L

LTC3707_START_RC

3V_5V_OK

THIS SIGNAL IS OPEN COLLECTOR TO GND WHEN POWER IS NOT GOOD

220PF IS USED TO QUIET NOISE ON PGOOD ONCE INTERNAL OPEN DRAIN IS DISENGAGED

DCDC_EN TRUTH TABLE

PMU_POWER_UP	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

SLEEP LEVEL SHIFTER (3V -> 5V)

+5V_SLEEP LOADS

1) FAN
2) Headphone amplifier
3) OPTICAL DRIVE
4) DVI
5) TRACKPAD

+3V_SLEEP LOADS

1) CPU PLL CONFIG CONTROL
2) INTREPID - I2C PULLUPS & OSCILLATOR
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULLUPS & HPD
7) BOOT BANGER
8) HARD DRIVE (IF USING 3V LOGIC)
9) WIRELESS
10) PMU - I2C PULLUPS

SLEEP_L_LS5_NET

SLEEP_NET_INV

SLEEP_NET

3V_SLEEP_PWREN_L

SLEEP_L_LS5

SLEEP_LS5

SLEEP_L_LS5_EN_L

SLEEP_LS5_EN_L

3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 34 OF 46	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.67GHZ (1.28VCORE) 1.300V->0.975V

1.50GHZ 1.200V->0.975V

1.67GHZ (1.26VCORE) 1.300V->0.975V

(VALUE WITHOUT OFFSET)

MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

Note:No stuff R67 to set skip mode of Vcore

(R93 CPU_BTR BOM OPTION SEE BOM TABLE)

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

	A/B_ =	
D<4..0>	Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, V = VA. B

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V*0.85*(Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

Connect MAX1717 GND pin 13 to GND at bottom-side FET

(CPU Vcore value with offset)

1.67GHZ 1.320V->0.990V (CPU SPEC: 1.280V -> 0.980V)

1.50GHZ 1.240V->0.990V (CPU SPEC: 1.200V -> 0.980V)

1.67GHZ(1.26VCORE) 1.300V->0.990V (CPU SPEC: 1.260V -> 0.980V)

ROUTE AS DIFFERENTIAL PAIR

Keep trace fat (40-100 mils) and short!!

Keep trace fat and short!!

Keep trace fat and short!!

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V CASE,SMD	C51,C52,C77,C78,C91,C92,C111	CRITICAL	
152S0242	1	IND,PWR,1.0UH,20,20.5A,SMD	L71	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2493	1	RES,MF,1/16W,2.49K OHM,1%,0402,SMD	R93	?	CPU_BTR_VCORE12
114S4023	1	RES,MF,1/16W,4.02K OHM,1%,0402,SMD	R97	?	CPU_BTR_VCORE12
116S1000	1	RES,MF,1/16W,0 OHM,5%,0402,SMD	R93	?	CPU_BST_VCORE126
114S1503	1	RES,MF,1/16W,1.5K OHM,1%,0402,SMD	R97	?	CPU_BST_VCORE126
114S2433	1	RES,MF,1/16W,2.43K OHM,1%,0402,SMD	R93	?	CPU_BST_VCORE13
114S4023	1	RES,MF,1/16W,4.02K OHM,1%,0402,SMD	R97	?	CPU_BST_VCORE13
114S2003	1	RES,MF,1/16W,2K OHM,1%,0402,SMD	R93	?	CPU_BTR_VCORE122
114S6043	1	RES,MF,1/16W,6.04K OHM,1%,0402,SMD	R97	?	CPU_BTR_VCORE122

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

Fmax Test Connections

NO STUFF J7 M-ST-SM-52465-1217

VCORE_GNDDIV_TEST, VCORE_GNDSNS_TEST, +3V_PMU_RESET, SOFT_PWR_ON_L, NC (RFU)

VCORE_D0, VCORE_D1, VCORE_D2, VCORE_D3, VCORE_D4

VCORE SUPPLY

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F

SCALE: NONE SHT 35 OF 46

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

M11 Power Shut down Sequencing

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 36 OF 46	

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2				
GROUP 0	126 MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ
	126 MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	126 MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	126 RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	126 RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	126 RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	126 RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ
	126 RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
	126 RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
GROUP 2	127 MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ
	127 MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	127 MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	127 RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	127 RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	127 RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	127 RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ
	127 RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	127 RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ
	128 RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz
	128 RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ
	128 RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
	128 RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
DDR RAM	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)			167 MHZ
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)			167 MHZ
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)			167 MHZ
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
ADDR	MEM_ADDR<12..0>	L:S::500	4					83 MHZ
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)			
	MEM_BA<1..0>	L:S::500	4					
	RAM_BA<1..0>	L:S:2000:3300	8		(200)			
CONTROL	MEM_CS_L<3..0>	L:S::500	4					
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)			
	MEM_CKE<3..0>	L:S::500	4					
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)			
	MEM_RAS_L	L:S::500 MIL	4					
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_CAS_L	L:S::500 MIL	4					
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_WE_L	L:S::500 MIL	4					
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)			
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8					
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7					

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK CPU UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT CPUFB OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	126 INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz
	126 INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz
	125 INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	125 CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz
	128 CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	128 CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
M11 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING	
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING	
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING	
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING	
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING	
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING	
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6680 | REV. F

SCALE NONE | SHT 37 OF 46

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS0	CPU_AACK_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ
	CPU_ARTRY_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_BG_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_BR_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_CI_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ
	CPU_DBG_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)			
	CPU_DRDY_L	L:S:1500 MIL:3200	MIL7		(250)			
	CPU_GBL_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_HIT_L	L:S:1500 MIL:2800	MIL7		(250)			
	CPU_OACK_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_OREQ_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TA_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TBST_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TEA_L	L:S:1500 MIL:3000	MIL7		(250)			
	CPU_TS_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)			
	CPU_TT<0..4>	L:S:1500:3400	7		(250)			
	CPU_WT_L	L:S:1500 MIL:3100	MIL7		(250)			

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

TMDS/DVO SIGNAL CONSTRAINTS

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALES

SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:300 MIL	100 OHM SPACING FOR TMDS	
SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:300 MIL	100 OHM SPACING FOR TMDS	
SI_TMDS_DN<0>	SI_TMDS_D0		100 OHM SPACING FOR TMDS	
SI_TMDS_DP<0>	SI_TMDS_D0		100 OHM SPACING FOR TMDS	
SI_TMDS_DN<1>	SI_TMDS_D1		100 OHM SPACING FOR TMDS	
SI_TMDS_DP<1>	SI_TMDS_D1		100 OHM SPACING FOR TMDS	
SI_TMDS_DN<2>	SI_TMDS_D2		100 OHM SPACING FOR TMDS	
SI_TMDS_DP<2>	SI_TMDS_D2		100 OHM SPACING FOR TMDS	
SI_TMDS_DN<3>	SI_TMDS_D3		100 OHM SPACING FOR TMDS	
SI_TMDS_DP<3>	SI_TMDS_D3		100 OHM SPACING FOR TMDS	
SI_TMDS_DN<4>	SI_TMDS_D4		100 OHM SPACING FOR TMDS	
SI_TMDS_DP<4>	SI_TMDS_D4		100 OHM SPACING FOR TMDS	
SI_TMDS_DN<5>	SI_TMDS_D5		100 OHM SPACING FOR TMDS	
SI_TMDS_DP<5>	SI_TMDS_D5		100 OHM SPACING FOR TMDS	

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

ATI_DVOD<23..0>	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610		
ATI_DVOD_DE	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		
ATI_DVO_HSYNC	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		
ATI_DVO_VSYNC	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		
ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:500 MIL	6	610.0000	165.0 MHz:::	
GPU_DVO_CLKP_R1	ATIDVOD:G:L:S:0 MIL:1100 MIL	6	610.0000	165.0 MHz:::	
GPU_DVO_CLKP_R2	ATIDVOD:G:L:S:0 MIL:1100 MIL	6	610.0000	165.0 MHz:::	

TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<0>	CONN_TMDS_D0		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<0>	CONN_TMDS_D0		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<1>	CONN_TMDS_D1		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<1>	CONN_TMDS_D1		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<2>	CONN_TMDS_D2		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<2>	CONN_TMDS_D2		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<3>	CONN_TMDS_D3		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<3>	CONN_TMDS_D3		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<4>	CONN_TMDS_D4		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<4>	CONN_TMDS_D4		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<5>	CONN_TMDS_D5		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<5>	CONN_TMDS_D5		500.0000	100 OHM SPACING FOR TMDS

GPU_R	GPU_R	500.0000	100 OHM SPACING
GPU_G	GPU_G	500.0000	100 OHM SPACING
GPU_B	GPU_B	500.0000	100 OHM SPACING

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F

SCALE: NONE

SHT 38 OF 46

Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
AGP	AGP_AD<15..0>	L:S:1050:1450	7					66 MHZ
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHZ
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ
	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ
AGP BYTES 2-3	AGP_AD<31..16>	L:S:1050:1450	7					66 MHZ
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHZ
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHZ
	AGP_SB_STB	L:S:1050 MIL:1450 MIL	4		(350)	8 MIL SPACING		66.00 MHZ
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL	4		(350)	8 MIL SPACING		66.00 MHZ
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_STOP_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_PAR	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_REQ_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_GNT_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_RBF_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710				(200)		100 MHZ
	UIDE_DATA<7>	U51.V1:RP19.3::600 MIL				(200)		100.0 MHZ
	UIDE_DATA<6..0>	L:S::600				(200)		100 MHZ
	UIDE_ADDR<2..0>	L:S::650			(200)	NEED TO MATCH DELAY TO 250		100 MHZ
	UIDE_RST_L	L:S::400 MIL				(200)		100.0 MHZ
	UIDE_DIOW_L	L:S::400 MIL				(200)		100.0 MHZ
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING		(200)		100.0 MHZ
	UIDE_DMACK_L	L:S::400 MIL				(200)		100.0 MHZ
	UIDE_CS0_L	L:S::500 MIL				(200)		100.0 MHZ
	UIDE_CS1_L	L:S::500 MIL				(200)		100.0 MHZ
	UIDE_DMARQ	L:S::400 MIL				(200)		100.0 MHZ
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING		(200)		100.0 MHZ
	UIDE_INTRQ	L:S::400 MIL				(200)		100.0 MHZ
	HD_DATA<15..0>	L:S:5000:6500	7			(200)		100 MHZ
	HD_ADDR<2..0>	L:S:5000:6500	7			(200)		100 MHZ
	HD_RESET_L	L:S:4000 MIL:6000 MIL	4		(200)	TOTAL UIDE+HD SKEW <500MIL		100.0 MHZ
	HD_DIOW_L	L:S:3000 MIL:5200 MIL	4			(200)		100.0 MHZ
	HD_DIOR_L	L:S:6100 MIL:6150 MIL	4	10 MIL SPACING		(200)		100.0 MHZ
	HD_DMACK_L	L:S:4500 MIL:6000 MIL	4			(200)		100.0 MHZ
	HD_CS0_L	L:S:3000 MIL:6000 MIL	4			(200)		100.0 MHZ
	HD_CS1_L	L:S:3000 MIL:6000 MIL	4			(200)		100.0 MHZ
	HD_DMARQ	L:S:4500 MIL:6000 MIL	4			(200)		100.0 MHZ
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL	4	10 MIL SPACING		(200)		100.0 MHZ
	HD_INTRQ	L:S:3000 MIL:5000 MIL	4					100.0 MHZ
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ
	EIDE_ADDR<2..0>	L:S::850						33 MHZ
	EIDE_CS0_L	L:S::850 MIL						33.00 MHZ
	EIDE_CS1_L	L:S::850 MIL						33.00 MHZ
	EIDE_RD_L	L:S::500 MIL						33.00 MHZ
	EIDE_WR_L	L:S::500 MIL						33.00 MHZ
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHZ
	EIDE_INT	L:S::500 MIL						33.00 MHZ
	EIDE_RST_L	L:S::500 MIL						33.00 MHZ
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHZ
	EIDE_DMARQ	L:S::500 MIL						33.00 MHZ
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHZ
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_DMAACK_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHZ
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)		100 MHZ
	ENET_RX_DV	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_RX_ER	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)		100 MHZ
	ENET_LINK_TXD<7..0>	L:S::600						100 MHZ
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL	4					100.0 MHZ
	ENET_LINK_TX_ER	L:S::400 MIL						100 MHZ
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL	4					100.0 MHZ
	ENET_LINK_TX_EN	L:S::400 MIL						100 MHZ
	ENET_MDIO	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_MDC	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_COL	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_CRS	L:S:8000 MIL:9000 MIL						100.0 MHZ
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)		100 MHZ
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)		98.304 MHZ
	FW_LINK_CNTL<1..0>	L:S:9000:10000						100 MHZ
	FW_PHY_CNTL<1..0>	L:S::300						98.304 MHZ
	FW_LINK_LREQ	L:S::300 MIL						100 MHZ
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL						98.304 MHZ
	FW_PINT	L:S:8500 MIL:9500 MIL						98.304 MHZ

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 11 MIL SPACING	
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_DN<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DP<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DN<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DP<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DN<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	TMDS_DP<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_DN<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_DP<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
USB 1.1 Zo = 90	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_TPAD_N	USB_TPAD_N	TPAD_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_TPAD_P	USB_TPAD_P	TPAD_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
USB 2.0 Zo = 90	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL			
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL			
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL			
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL			
REMOVE CONSTRAIN TO AVOID DRC OCCUR	1772_CSSN					
	1772_CSSP					
	1772_CSIN					
	1772_CSIP					
	3V_SNSM					
	3V_SNSP					
	5V_SNSM					
	5V_SNSP					
	THERM1_M_DM					
	THERM1_M_DP					
	THERM2_M_DM					
	THERM2_M_DP					
	THERM1_A_DM					
	THERM1_A_DP					
	THERM2_A_DM					
	THERM2_A_DP					

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.9MIL (TRACE WIDTH)
S = 5.6MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 39 OF 46	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+BATT	VOLTAGE=12.8V	MIN_LINE_WIDTH=10MIL	MIN_NECK_WIDTH=25MIL
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 24 41
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 41
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 41
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32 33 41
	I496 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32 40
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32 40
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32 41
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32 41
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	32
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 32
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	32
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	32
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	32
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	33
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	33
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	31 33
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	33 34
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	33
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	33
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	27 31
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 26 34
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 26
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10	41
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	24 41
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23 41
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23 41
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 23 41
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 23
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10 23 41
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	23
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	23
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	23 41
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	23 41
AUDIO	I435 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27 34
	I435 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27 34
	I435 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50	27
FAN	I438 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27 41
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41

I/O AREA		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 IN
INVERTER		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 IN
TRACKPAD	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 IN
LVDS	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 IN
	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 IN
	CHGND4			

ENET_CTAP_CHGND VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5 6 35 41
	CPU_AVDD	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5 6 7 8 15 16 35
	I386 CPU_AVDD_VIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5
	I386 CPU_AVDD_VOUT	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	11
INTREPID	I387 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	9
	VIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
CARDBUS	I386 +3V_SLEEP_PCCARD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 18
	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 18
ATI M11	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 19 21 41
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 12 19 21 22
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 22
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 19 22
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 19 20 21 22
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 12 15 16 19 21 22
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 22
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21 22
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 22
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 22
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
	I346 +GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	I347 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	21
	I348 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10	36
	I348 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	21
	I350 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	21
	I351 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10	21
	I352 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	21
	I353 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	36
	I354 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	36
	I355 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	36
	I360 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 22
	I361 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
ETHERNET 88E1111 NEC USB2.0 FW	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 28
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 28
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 28
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 28
	I318 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 17
	I317 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 17
	I362 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12 29
	I412 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	I345 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 29 30
	I410 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30 41
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30 41
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29 30
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	I414 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	I366 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	33
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 33
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10	33
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	33
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	33
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	33
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 32 33
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 34
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	34
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 36
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 36
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 36
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 36
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	36
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 36
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 36
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 36
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 36
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8	36
	2_5V_ILIM		MIN_LINE_WIDTH=8	36
	MAX1715_TON		MIN_LINE_WIDTH=8	36
	MAX1715_SKIP		MIN_LINE_WIDTH=8	36
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	36
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 36
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 35
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10 35
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 35
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 35
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 35
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 35
	VCORE_ILIM		MIN_LINE_WIDTH=8	35
	VCORE_REF		MIN_LINE_WIDTH=8	35
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	35
	VCORE_CC		MIN_LINE_WIDTH=8	35
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	35 41
	VCORE_TIME		MIN_LINE_WIDTH=8	35
	VCORE_VGATE		MIN_LINE_WIDTH=8	14 35
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	35
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	35
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	35
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	35
	I437 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10	35
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 21
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 21
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 21
	1778_ION		MIN_LINE_WIDTH=8	21
	1778_ITH		MIN_LINE_WIDTH=8	21
	1778_ITH_RC		MIN_LINE_WIDTH=8	21
	1778_VFB		MIN_LINE_WIDTH=8	21 41
	1778_FCB		MIN_LINE_WIDTH=8	21
	1778_VRNG		MIN_LINE_WIDTH=8	21
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 36
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 36
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 36
	1_8V_VFB		MIN_LINE_WIDTH=8	36
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8	36
	LTC3411_ITH		MIN_LINE_WIDTH=8	36
	LTC3411_SYNC		MIN_LINE_WIDTH=8	36
	LTC3411_SHDN		MIN_LINE_WIDTH=8	36
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 14
CY28512D LMU CONN	I436 +3V_MAIN_SSCG	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	I436 +3V_MAIN_LMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 24
OPT DRIVER	I436 +5V_SLEEP_OPT	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 26

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 40 OF 46	

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
FUNC TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	J2 JTAG_ASIC_TMS	TRUE			13 28
	J3 JTAG_ASIC_TDI	TRUE			13
	J1 JTAG_ASIC_TDO_TP	TRUE			28
	J4 JTAG_ASIC_TCK	TRUE			13 28
	J6 JTAG_ASIC_TRST_L	TRUE			13 28
	J5 CPU_CHKSTP_OUT_L	TRUE			5
	J7 CPU_SRESET_L	TRUE			5
	J9 CPU_HRESET_L	TRUE			5 6 7
	J8 JTAG_CPU_TMS	TRUE			5 6
	J10 JTAG_CPU_TDI	TRUE			5 6
	J12 JTAG_CPU_TDO_TP	TRUE			5
	J11 JTAG_CPU_TCK	TRUE			5 6
	J13 JTAG_CPU_TRST_L	TRUE			5 6
	J18 INT_JTAG_TEI	TRUE			13
	J20 INT_TST_MONIN_PD	TRUE			13
	J19 INT_TST_MONOUT_TP	TRUE			13
	J21 INT_TST_PLLEN_PD	TRUE			13
INT I2C	J15 INT_I2C_CLK0	TRUE			6 11 13 24
	J14 INT_I2C_DATA0	TRUE			6 11 13 24
	J16 INT_I2C_CLK1	TRUE			13 14 24 25 27
	J17 INT_I2C_DATA1	TRUE			13 14 24 25 27
PWR/GND	J21 +PBUS	TRUE			40
	J21 +24V_PBUS	TRUE			40
	J25 GPU_VCORE	TRUE			19 21 40
	J24 1778_VFB	TRUE			21 40
	J27 CPU_VCORE_SLEEP	TRUE			5 6 35 40
	J26 VCORE_FB	TRUE			35 40
	J21 +1_8V_MAIN	TRUE			40
	J21 +2_5V_MAIN	TRUE			40
	J21 +5V_MAIN	TRUE	2		40 41
	J22 +5V_SLEEP	TRUE	2		40 41
	J22 +3V_MAIN	TRUE	4		24 40
		TRUE		1000	IN
	J22 +3V_PMU	TRUE			40
CARDBUS DVI	K36 CBUS_DET_1_L	TRUE		2000	18
	K35 CBUS_DET_2_L	TRUE		2000	18
	K40 TMDS_CONN_CLKN	TRUE		1000	23 38
	K39 TMDS_CONN_CLKP	TRUE		1000	23 38
	K42 VGA_R	TRUE		1000	23
	K41 VGA_G	TRUE		1000	23
	K44 VGA_B	TRUE		1000	23
	K43 VGA_HSYNC	TRUE		1000	23
	K46 VGA_VSYNC	TRUE		1000	23
	K45 DVI_DDC_CLK_UF	TRUE		1000	23
	K47 DVI_DDC_DATA_UF	TRUE		1000	23
	K48 DVI_HPD_UF	TRUE		1000	23
	K49 +5V_DDC_SLEEP	TRUE		2000	23 40
		TRUE	2	2000	IN
CHGND1		TRUE	6	1000	IN
LVDS	K52 LVDS_L0N			1000	21 23 39
	K51 LVDS_L0P			1000	21 23 39
	K53 LVDS_L1N			1000	21 23 39
	K55 LVDS_L1P			1000	21 23 39
	K54 LVDS_L2N			1000	21 23 39
	K57 LVDS_L2P			1000	21 23 39
	K56 CLKLVDS_LN	TRUE		1000	21 23 39
	K58 CLKLVDS_LP	TRUE		1000	21 23 39
	K59 LVDS_DDC_CLK	TRUE		1000	21 23
	K60 LVDS_DDC_DATA	TRUE		1000	21 23
	K62 +3V_LCD	TRUE	2	2000	23 40
	K22 +3V_SLEEP	TRUE		2000	40 41
		TRUE	2	2000	IN
CHGND4		TRUE	6	1000	IN
INVERTER	K67 +14V_INV	TRUE		2000	23 40
	K66 +5V_INV_SW	TRUE		2000	23 40
	K68 BRIGHT_PWM	TRUE		2000	23
	K24 INV_GND	TRUE		2000	23
		TRUE		1000	IN
S-VIDEO	K70 TV_C	TRUE		2000	23
	K72 TV_Y	TRUE		2000	23
	K71 TV_COMP	TRUE		2000	23
	K73 TV_GND1	TRUE		2000	23 40
	K74 TV_GND2	TRUE		2000	23 40
LIO	K76 INT_I2S0_SND_TO_DAC	TRUE		1000	14 27
	K75 INT_I2S0_SND_LRCLK	TRUE		1000	14 27
	K78 INT_I2S0_SND_MCLK	TRUE		1000	14 27 37
	K83 INT_I2S0_SND_SCLK	TRUE		1000	14 27
	K82 INT_I2S0_SND_FROM_ADC	TRUE		1000	14 27
	K77 SND_HP_MUTE_L	TRUE		1000	14 27
	K79 SND_AMP_MUTE	TRUE		1000	27
	K84 SND_HW_RESET_L	TRUE		1000	14 27
	K85 SND_HP_SENSE_L	TRUE		1000	14 27
	K86 SND_LIN_SENSE_L	TRUE		1000	14 27
	K81 INT_I2C_CLK2	TRUE		1000	14 27
	K80 INT_I2C_DATA2	TRUE		1000	14 27
	K87 ADAPTER_DET	TRUE		1000	27 31
	K88 CHARGE_LED_L	TRUE		1000	27 31
	K89 NEC_LUSB_OCI_UF	TRUE		1000	17 27
	K90 NEC_LUSB_PPON	TRUE		1000	17 27
	K22 +5V_MAIN	TRUE	2	2000	40 41
	K22 +5V_SLEEP	TRUE	2	3000	40 41
	K22 +3V_SLEEP	TRUE		2000	40 41

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	K94 NEC_USB_DAM	TRUE			17 27 39
	K95 NEC_USB_DAP	TRUE			17 27 39
	K95 NEC_USB_DBM	TRUE			17 27 39
	K97 NEC_USB_DBP	TRUE			17 27 39
	K98 BT_USB_DM	TRUE			14 27 39
	K99 BT_USB_DP	TRUE			14 27 39
	K10 USB_TPAD_N	TRUE			14 24 39
	K10 USB_TPAD_P	TRUE			14 24 39
RT. USB WIRELESS	K10 NEC_RUSB_PPON	TRUE			17 27
	K10 NEC_RUSB_OCI_UF	TRUE			17 27
	K10 PCI_AD<0..31>	TRUE		1000	9 12 17 18 26 39
	K10 PCI_FRAME_L	TRUE		1000	12 17 18 26 39
	K10 PCI_TRDY_L	TRUE		1000	12 17 18 26 39
	K10 PCI_IRDY_L	TRUE		1000	12 17 18 26 39
	K10 PCI_DEVSEL_L	TRUE		1000	12 17 18 26 39
	K10 PCI_STOP_L	TRUE		1000	12 17 18 26 39
	K11 PCI_PAR	TRUE		1000	12 17 18 26 39
	K11 AIRPORT_PCI_REQ_L	TRUE		1000	12 26
	K11 AIRPORT_PCI_GNT_L	TRUE		1000	12 26
	K11 AIRPORT_PCI_INT_L	TRUE		1000	14 26
	K11 MAIN_RESET_L	TRUE		1000	14 17 18 19 20 26 31
	K11 CLK33M_AIRPORT	TRUE		1000	12 26 37
	K11 PMU_PME_L	TRUE		1000	14 17 26 31
	K11 ROM_ONBOARD_CS_L	TRUE		1000	9
	K11 ROM_OE_L	TRUE		1000	9 12
	K11 ROM_CS_L	TRUE		1000	9 12
	K11 ROM_RW_L	TRUE		1000	9 12
	K12 RF_DISABLE_L	TRUE		1000	26
	K12 AIRPORT_CLKRUN_L	TRUE		1000	26
	K12 +3V_AIRPORT	TRUE	4	2000	40
		TRUE	6	1000	IN
OPTICAL	K12 EIDE_OPTICAL_DATA<0..15>	TRUE		2000	26 39
	K12 EIDE_OPTICAL_DMA_RQ	TRUE		2000	26 39
	K12 EIDE_OPTICAL_READ_L	TRUE		2000	26 39
	K12 EIDE_OPTICAL_DMAACK_L	TRUE		2000	26 39
	K12 EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	26 39
	K12 EIDE_OPTICAL_CS0_L	TRUE		2000	26 39
	K12 EIDE_OPTICAL_CS1_L	TRUE		2000	26 39
	K13 EIDE_OPTICAL_RST_L	TRUE		2000	26 39
	K13 EIDE_OPTICAL_WR_L	TRUE		2000	26 39
	K13 EIDE_OPTICAL_IOCHRDY	TRUE		2000	26 39
	K13 EIDE_OPTICAL_INT	TRUE		2000	26 39
TRACKPAD	K13 +5V_TPAD_SLEEP	TRUE		3000	40
	K13 TPAD_F_TXD	TRUE		3000	
	K13 TPAD_F_RXD	TRUE		3000	
	K13 SOFT_PWR_ON_L	TRUE		3000	23 24 31 35
MODEM/ SERIAL	K14 COMM_RESET_L	TRUE		4000	14 27
	K14 COMM_SHUTDOWN	TRUE		4000	
	K14 COMM_RING_DET_L	TRUE		4000	14 27 31
	K14 COMM_TXD_L	TRUE		4000	14 27
	K14 COMM_TRXC	TRUE		4000	14 27
	K14 COMM_GPIO_L	TRUE		4000	14 27
	K14 COMM_DTR_L	TRUE		4000	14 27
	K14 COMM_RTS_L	TRUE		4000	14 27
	K14 COMM_RXD	TRUE		4000	14 27
KEYBOARD	K14 KBD_ID	TRUE		3000	24 31
	K15 KBD_INTL	TRUE		3000	
	K15 KBD_JIS	TRUE		3000	
	K15 KBD_CAPSLOCK_LED	TRUE		3000	
	K15 KBD_NUMLOCK_LED	TRUE		3000	
	K15 KBD_FUNCTION_L			3000	24 31
	K15 KBD_COMMAND_L			3000	24 31
	K15 KBD_OPTION_L			3000	24 31
	K15 KBD_CONTROL_L			3000	24 31
	K15 KBD_SHIFT_L			3000	24 31
	K15 KBD_X<0..9>			3000	24 31
	K16 KBD_Y<0..7>			3000	
BATTERY	K16 +BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	32 40
	K16 BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	32 40
	K16 BATT_CLK	TRUE		1000	32
	K16 BATT_DATA	TRUE		1000	32
	K16 PMU_BATT_DET_L	TRUE		1000	31 32
FANS	K16 +FAN_PWR	TRUE		3000	27 40
	K16 FAN1_TACH	TRUE		3000	27
	K16 FAN2_TACH	TRUE		3000	27
	K17 FAN1_GND	TRUE		3000	40
	K17 FAN2_GND	TRUE		3000	40
ETHERNET	K17 MDI_P<0..3>	TRUE		1000	28 39
	K17 MDI_M<0..3>	TRUE		1000	28 39
FIREWIRE	K17 FW_TPO0P	TRUE		1000	29 30 39
	K17 FW_TPO0N	TRUE		1000	29 30 39
	K17 FW_TPO0R	TRUE		1000	30
	K17 FW_TPI0P	TRUE		1000	29 30 39
	K18 FW_TPI0N	TRUE		1000	29 30 39
	K18 +FW_VP0	TRUE		1000	30 40
	K18 FW_VGND	TRUE		1000	41

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	K18 FW_TPO1P	TRUE		1000	30 39
	K18 FW_TPO1N	TRUE		1000	30 39
	K18 FW_TPI1P	TRUE		1000	30 39
	K18 FW_TPI1N	TRUE		1000	30 39
	K18 +FW_VP1	TRUE		1000	30 40
	K18 FW_VGND	TRUE		1000	41
DC PWR IN	K18 +ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	32 33 40
LMU/ALS	K28 ST7_SLEEP_LED_H	TRUE			24
	K28 PMU_SLEEP_LED	TRUE			24
	K28 PMU_LID_CLOSED_L	TRUE			24 31
	K28 LMU_DETECT	TRUE			24
		TRUE	6	1000	IN
			(100 MIL PROBE PREFERRED)		
MISC.	K19 SLEEP_LED	TRUE			24
	K19 PMU_KB_RESET_L	TRUE			
	K19 SLEEP	TRUE			24 27 31 34 36
	K19 PMU_CPU_HRESET_L	TRUE			6 31
	K19 BB_RESET_L	TRUE			6
	K24 +3V_PMU_RESET	TRUE			31 35
	K25 MMM_ACC_X_AXIS	TRUE			25
	K25 MMM_ACC_Y_AXIS	TRUE			25
	K25 MMM_ACC_Z_AXIS	TRUE			25
	K25 MMM_ACC_SELFTEST	TRUE			25
	K25 +BATT_ISNS_P	TRUE			25
	K25 +PPBATT_ISNS_N	TRUE			25
	K25 +PWR_SUPERCAP	TRUE			33
	REMOVE CONSTRAIN FOR UNUSED FUNCTIONAL TP				
	K28 +3V_HALL_EFFECT				24 40
	K28 LID_CLOSED_L				24
	K28 TMDS_DN<0..2>				20 23 39
	K28 TMDS_DP<0..2>				20 23 39

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6680 | REV. F

SCALE NONE | SHT 41 OF 46

REVISION HISTORY

EVT2 RELEASE

08/13/04 - 1. CHANGE EXT TMDS SWING RESISTORS TO 510 OHM (R869, R876), REMOVE SI_RESET PULL HIGH
2. CHANGE RGB SIGNAL INPEDENCE (R341, R342, R346, R456, R458, R462)
3. ADD 2 RESISTORS (NO STUFF) BETWEEN FAN_PWM AND FAN_PWM_L OF FAN1 AND FAN2
4. CHANGE 2 CAPS (C233, C803) TO IMPROVE FEEDBACK PROTECTION AND PBUS CURRENT LIMIT CIRCUIT
5. MODIFY CPU_VCORE VID AND CPU_VCORE SETTING

08/16/04 - 1. MODIFY CPU_AVDD SETTING
08/20/04 - 1. ADD TRACKPAD POWER +5V_TPAD CONTROL CIRCUIT
09/01/04 - 1. CHANGE ALL FONTS INTO SMALL ONES
09/02/04 - 1. MODIFT CPU_VCORE VID AND CPU_VCORE SEETING AGAIN
2. MODIFY CPU_AVDD SEETING AGAIN
3. CHANGE INT TMDS DAMPING RESISTERS (R760-R767) TO 0 OHM
09/03/04 - 1. ADD MMM CIRCUIT, ARRANGE 2 INTREPID GPIOS FOR MM_FFIRQ_L, MM_SIRQ_L AND PULL UP RESISTORS R801, R802
2. ADD R803 BETWEEN DP6 AND DCDC_IN
3. ADD R804 AND SUPERCAP C692 ON +4_6V_BU
4. CHANGE TRACKPAD CONNECTOR J10 AND PIN OUT

09/06/04 - 1. ADD EMI SOLUTION L12
09/07/04 - 1. CHANGE TRACKPAD CONNECTOR PIN OUT
09/08/04 - 1. ADD BATTERY CURRENT SENSOR CIRCUIT
09/09/04 - 1. ADD EMI SOLUTION R816; ADD MMM RESET CIRCUIT
09/10/04 - 1. MODIFY FIREWIRE PORT0 POWER CIRCUIT
2. ADD NET FROM BATTERY CURRENT SENSOR CIRCUIT TO PMU
09/13/04 - 1. ADD CURRENT LIMITER R821 BETWEEN PMU(U29) AND U33
2. ADD PULL UP AND PULL DOWN RESISTORS FOR MMM SENSOR

DVT RELEASE

09/27/04 - 1. ADD ST MMM SENSOR CIRCUIT
10/14/04 - 2. ADD FIREWIRE POWER PROTECT CIRCUIT
10/15/04 - 3. CHANGE EXT_TMDS TERMINAL RESISTERS AND V SWINING RESISTOR
10/22/04 - 4. CHANGE FAN CONTROLLER FROM ADT7460 TO ADT7467
11/02/04 - 5. CHANGE BBANG IC TO ATTINY2313

PVT RELEASE

12/17/04 - 1. REMOVE ALL OPEN JUMPER
12/17/04 - 2. SCHEMATIC RELEASE FOR PRODUCTION

PVT RELEASE (REV C)

02/11/05 - 1. CHANGE FW F3 TO 740S0018

PRODUCTION RELEASE (REV D)

04/12/05 - 1. ADD MPU R1.4
2. CHANGE 88E1111 B1(338S0223) TO PRIMARY AND B0 (338S0079) TO SECONDARY

PRODUCTION RELEASE (REV E)

08/24/05 - 1. ADD MPU R1.5 (337S3217 AND 337S3218)
08/25/05 - 1. ADD 341S1792 (BOOTROM,4.9.1F3)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6680 | REV. F

SCALE NONE | SHT 42 OF 46

8	7	6	5	4	3	2	1

D

C

B

A

*** Signal Cross-Reference for the entire design ***

```
PCI_STOP_L       12A7< 12C7<> 17B7<> 18B7<> 26C5<>
                 39C5> 41C3>
PCI_TRDY_L       12B7< 12C7<> 17B7<> 18A7<> 26C5<>
                 39C5> 41D3>
PLL_STOP_L        7C4<> 7C8<>
PMU_ACK_L        14C2< 31C4<>
PMU_AC_DET       31A5< 31B4<>
PMU_AC_IN        31B4<>
PMU_BATT0_DET_L  31B4<>
PMU_BATT1_DET_L_PU  31B4<> 31D2<
PMU_BATT_DET_L   31A8<> 31B3< 31D2< 32A4<> 41A3>
PMU_BYTE         31B6< 31C7<
PMU_CHARGE_V     31C4<> 32B8<>
PMU_CHRG_BATT_B  31C4<> 32A8<>
PMU_CLK          14C2<> 31C4<>
PMU_CNVSS        31B6< 31C7<
PMU_CPU_HRESET_L  6A2< 6C3<> 31C4<> 41C1>
PMU_CUSTOM_RESET  31A7<> 31B8<
PMU_CUSTOM_RESET_L  31A8<>
PMU_EPM          31C4<> 31D2<
PMU_FROM_INT     14C2<> 31C4<>
PMU_I2C_CLK      31B4<> 31C2<
PMU_I2C_DATA     31B4<> 31C2<
PMU_INT_L        14B5<> 14B7< 31B6<>
PMU_INT_NMI      14B5<> 14B7< 31D4<>
PMU_KB_RESET_L   41C1>
PMU_LID_CLOSED_L  24A1< 24D6<> 31B2< 31C4<> 41D1>
PMU_NMI_BUTTON_L  31C2< 31C4<>
PMU_NMI_L        31C2< 31C4<>
PMU_OOPS         31B2< 31B4<>
PMU_PME_L        14A5<> 17A8< 26D5<> 31B2< 31C4<>
                 41C3>
PMU_POWERUP_OK   31B4<> 31D2<
PMU_POWER_UP_L   30C8<> 31C6<> 31D7< 34B8<
PMU_RFQ_L        14B7< 14C2> 31C4<>
PMU_RESET_BUTTON_L  24A7< 31C4<> 31D2<
PMU_RESET_L      31B6< 31B7>
PMU_SELECT       31C6<>
PMU_SLEEP_LED    24C7<> 24D6<> 41D1>
PMU_SLEEP_LED_L  24C8<> 31C4<>
PMU_SMB_CLK      31B4<> 31C2< 32A3<
PMU_SMB_DATA     31B4<> 31C2< 32A2<
PMU_TO_INT       14C2<> 31C4<>
POWER_UP         30D7<>
POWER_VALID      31B2< 31C4<>
PP3V3_MMM        25C8< 25D5<
PP3V3_MMM_PIC    25C1< 25D5<
PP3V3_SI_AVCC1   20C7< 20D7<
PP3V3_SI_AVCC2   20C5< 20D7<
PP3V3_SI_PVCC1   20C7<
PP3V3_SI_PVCC2   20C5<
PP3V3_SI_VCC1    20C7< 20D8<
PP3V3_SI_VCC2    20C5< 20D7<
PWR_BUTTON_L     24A7< 24B3<>
RAM_ADDR<0>      9B4< 11B3<> 11B6<>
RAM_ADDR<12..0>  37A5>
RAM_ADDR<1>      9B4< 11B5<> 11B8<>
RAM_ADDR<2>      9B4< 11B3<> 11B6<>
RAM_ADDR<3>      9B4< 11B5<> 11B8<>
RAM_ADDR<4>      9B4< 11B3<> 11B6<>
RAM_ADDR<5>      9B4< 11B5<> 11B8<>
RAM_ADDR<6>      9B4< 11B3<> 11B6<>
RAM_ADDR<7>      9B4< 11B5<> 11B8<>
RAM_ADDR<8>      9B4< 11B3<> 11B6<>
RAM_ADDR<9>      9A4< 11B5<> 11B8<>
RAM_ADDR<10>     9A4< 11B5<> 11B8<>
RAM_ADDR<11>     9A4< 11B3<> 11B6<>
RAM_ADDR<12>     9A4< 11B5<> 11B8<>
RAM_BA<0>        9A4< 11B5<> 11B8<>
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RAM_CS_L<3..0>   37A5>
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RAM_DATA_A<7..0>  37D5>
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RAM_DATA_A<6>    10B8<> 11D8<>
RAM_DATA_A<7>    10B8<> 11D6<>
RAM_DATA_A<8>    10B8<> 11D8<>
RAM_DATA_A<15..8>  37C5>
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RAM_DATA_A<10>   10C7<> 11D6<>
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RAM_DATA_A<31..24>  37C5>
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RAM_DATA_B<15..8>  37C5>
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RAM_DATA_B<10>   10C8<> 11D5<>
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RAM_DATA_B<25..24>  37C5>
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SI_RESET_L       20B6< 21C7<>
SI_RESET_L_R     20B4< 20B7< 20D7<
SI_SECONDARY     20A8< 20D5<>
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SND_HW_RESET_L   14A8< 14B5<> 27D7<> 41A6>
SND_LIN_SENSE_L  14B5<> 27C8<> 41A6>
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ST7_SLEEP_LED_H  24C5<> 24C6<> 24D6<> 41D1>
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SYSCLK_CPU_UF    8A5<> 37D1>
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SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 37C1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 37C1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 37C1>
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SYSCLK_DDRCLK_B0_L  9C4< 11D5<> 37C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 37D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 37D1>
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SYSCLK_DDRCLK_B1_L  9D4< 11A3<> 37C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 37D1>
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THERM_L_OC       27B1<> 31B4<>
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TMDS_CONN_CLKP   23C6<> 23C7<> 38C1> 41C6>
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TMDS_DN<3>       20B1< 20B2< 23B4<> 38B1>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	F
SCALE: NONE	SHT 44 OF 46	

*** Part Cross-Reference for the entire design ***

Ref	Part	Page
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J2	CON_4RT_WRIB	24
J3	CON_M40ST_D4MT_SM	27
J4	CON_4RT_WRIB	23
J5	CON_M80ST_D4MT_SM	18
J6	CON_F80ST_D4MT_SM	26
J7	CON_12	35
J8	CON_2RTSM_125	24
J9	CON_F1ST_S2MT_SM	14
J10	CON_M16ST_D_SMA	24
J12	CON_M50SM_5MM	26
J13	CON_M50SM_5MM	26
J14	CON_F30RT_S2MT_SM	23
J15	CON_F10RT_S2MT_SM	27
J16	CON_3RTSM_125	33
J17	CON_M16ST_D_SMA	27
J18	CON_M4RT_S2MT_SM	27
J19	CON_F20ST_D_SM	24
J20	CON_F9RT_1394B_S6MT_SMA	30
J21	CON_F5RT_MINIDIN_TH	23
J22	CON_F30RT_T6MT_TH1	23
J23	CON_RJ45_10RT_S4MT_TH1	28
J24	CON_F6RT_S4MT_TH1	30
J25	CON_F400RT_DDRDIMM_SM3	11
J26	CON_M8RT_S_SM	32
J27	CON_M4RT_S_SM	32
J28	CON_10STSM_5087	27
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RP2	RPAK4P	8
RP3	RPAK4P	8
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RP5	RPAK4P	14
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RP15	RPAK4P	14
RP16	RPAK4P	13
RP17	RPAK4P	9
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RP31	RPAK4P	9
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RP33	RPAK4P	12
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RP35	RPAK4P	13
RP36	RPAK4P	12
RP37	RPAK4P	29
RP38	RPAK4P	29
RP39	RPAK4P	31
RP40	RPAK10P2C	24

RP41	RPAK4P	31
RP42	RPAK10P2C	24
RP43	RPAK4P	17
RP44	RPAK4P	17
RP45	RPAK4P	17
RP46	RPAK10P2C	6
RP47	RPAK4P	14
RP61	RPAK2P	20
RP70	RPAK2P	20
RP72	RPAK2P	20
RP74	RPAK2P	35
RP75	RPAK2P	20
SH1	SHLD_3P_EMI	4
U1	COMPARATOR_LMC7211	32
U2	NC7S32	23
U3	AMP_MAX4172	32
U4	PWR_CNTRL_TPS2211	18
U5	FAN2558	5
U6	MAX1772	32
U7	MAX1717	35
U8	PCI1510GGU	18
U9	SN74AUC1G08	6
U10	SN74AUC1G08	6
U11	FEPR_1MX8	9
U12	SN74AUC1G04	7
U13	LTC1625	33
U14	COMPARATOR_LMC7211	33
U15	PIC16F818_QFN	25
U16	CBTV4020	10
U17	UPD720101_FBGA	17
U18	CBTV4020	10
U19	MAX1715	36
U20	KXM52	25
U21	741125	24
U22	VREG_LP2951	33
U23	VREG_LP2951	33
U24	SIL178	20
U25	SIL178	20
U26	MAX6804	31
U27	CBTV4020	10
U28	CBTV4020	10
U29	M16C62	31
U30	CLK_GEN_CY25811	19
U31	CLK_GEN_CY28512	14
U32	LTC1778	21
U33	COMPARATOR_LMC7211	31
U34	VREG_MM1571J	22
U35	LTC3707	34
U36	TSB81BA3A	29
U37	VREG_LM2594	29
U38	VREG_LT1962	29
U39	741G32	23
U40	741G32	23
U41	INA138	25
U42	COMPARATOR_LMC7211	23
U43	TRANSCEIVER_88E1111	28
U44	LTC1761	29
U45	LTC3405	28
U46	LTC3411	36
U47	RAGE_MBLTY_M11_CSP64_667	19 21 22
U48	TRA_SI5467BDQ	36
U49	VREG_LT1962	14
U50	TRA_SI3447DV	36
U51	INTREPID 8 9 12 13 14 15	
U52	EEPROM_32KX8_M24256B	6
U53	ADT7467	27
U54	ATTINY2313	6
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U56	APOLLO_MPC7447A_360	5 6
U57	COMPARATOR_LMC7211	32
U58	LI53L02AQ	25
U59	COMPARATOR_LMC7211	30
U60	VREG_MM1571J	22
XW1	SHORT	32
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XW3	SHORT	33
XW4	SHORT	21
XW5	SHORT	21
XW6	SHORT	21
XW7	JUMPER	21
XW8	SHORT	36
XW9	SHORT	21
XW10	SHORT	36
XW11	SHORT	21
XW12	SHORT	21
XW13	SHORT	34
XW14	SHORT	23
XW15	SHORT	23
XW16	JUMPER	22
XW17	SHORT	36
XW18	JUMPER	26
XW19	JUMPER	33
XW20	JUMPER	34
XW21	SHORT	36
XW22	JUMPER	34
XW23	SHORT	36
XW24	JUMPER	36
XW25	SHORT	36
XW26	JUMPER	36
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XW33	JUMPER	36
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XW36	SHORT	25
XW37	SHORT	25
Y1	CRYSTAL	17
Y2	CRYSTAL	14
Y3	CRYSTAL_4PIN	31
Y4	CRYSTAL	31
Y5	CRYSTAL_4PIN	28
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