1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

LINK

02/23/2004

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
03		316008	ENGINEERING RELEASED	02/23/04	?

Module Components

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2835	1	IC,PPC970,1.8GHz,1.1V,80C,25W,576CBGA	U2900	CRITICAL	
343S0284	1	IC,U3LITE,V1.1,300MM,PBGA	U3	CRITICAL	
343S0283	1	IC,ASIC,SHASTA,V1.1,484BALL,PBGA	U2300	CRITICAL	
338S0154	1	IC,ATI,M11-CSP64,NO HEATSPREADER	U4900	CRITICAL	M11CSP64
338S0158	1	IC,ATI,M11-CSP128,NO HEATSPREADER	U4900	CRITICAL	M11CSP128
343S0288	1	IC,ASIC,VESTA,V1.1	U8600	CRITICAL	
341S1340	1	BOOTROM,PROTO,Q51	U7500	CRITICAL	
341S1394	1	SMU,PROTO,Q51	U1300	CRITICAL	

Alternates Components

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0282	343S0284		U3	U3L,V1.1,200MM,PBGA

_DRAWING
TITLE=LINK
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 18:35:53 2004

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

Apple Computer Inc.

TITLE
SCHEMATIC ,LINK

DRAWING NUMBER 051-6532 | REV. 03

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SYSTEM BLOCK DIAGRAM

J700
Nicky (PWR) Connector
P.7

Power Supply & Charger
P.7-12

J750
Battery Connector
P.7

U2900
CPU
NEO 10S
P.26-29

ELASTIC INTERFACE
44-BIT/Directional
APPLE PI
1.2V/600MHz

AGP BUS
4X/8X
1.5V/0.8V
32BITS
267/533MHZ

AGP
PAGE 35
APPLE PI
PAGE 25
U3
U3LITE
CORE
PAGE 19
HYPERTRANSPORT
PAGE 42
MISC
PAGE 21
MAIN MEMORY
PAGE 32

U1300
SMU
P.13

I2C
Level shifting
P.17

I2C buses

RTC
P.13

Max1668
Thermal
P.15

MEMORY BUS
2.5V
333MHz
128BITS

J4010/J4020
DDR SDRAM DIMM 0

DDR SDRAM DIMM 1
SODIMM Connector
P.34

HYPERTRANSPORT
8-BIT/Direction
1.2V/400MHZ
CONTROL = 2.5V

U4900
ATI
M11
64/128MB
P.36,38-40

MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)

TMDS
RGB
DDC
J5900
DVI-I Connector
P.41

S-Video/Comp
J5960
S-Video Connector
P.41

LVDS

J5980
Inverter Connector
P.41

J5970
LCD Panel Connector
P.41

U2600
Pulsar Clock Gen
P.23-24

EI Clocks
VSP Clock
HT Clocks
AGP Clocks
PCI Clocks
SATA Clock

J1600
LEFT USB Bluetooth Connector
P.16

ENET Pairs
4 Datapairs @125MHz
J8700
Gigabit Ethernet Connector
P.54

U8600
VESTA
Core
PAGE 12
ETHERNET
PAGE 53
FIREWIRE
PAGE 56

J8350
Hard DRIVE Connector
P.51

133MHz/3.3V/16 Bit

U8150
Serial ATA Bridge
P.50

1.5Gbps/1.2V/1 Bit/Directonal

HYPERTRANSPORT
PAGE 43
SATA
PAGE 49
SATA1
SATA2
U2300
SHASTA
ETHERNET
PAGE 52
FIREWIRE
PAGE 55

8-bit TX & 8-bit RX
GMII (3.3V/125MHz)

1394 OHCI (3.3V/98MHz)

Not Used

FW-A Pairs
2 Datapairs @200MHz
J9010
Firewire A Connector
P.57

FW-B pairs
2 Datapairs @400MHz
J9020
Firewire B Connector
P.57

J8300
OPTICAL DRIVE Connector
P.51

133MHz/3.3V/16 Bit

UATA
PAGE 49
CORE
PAGE 20
PCI
PAGE 44
GPIO/PCI64
PAGE 22
I2S
PAGE 22
SCCA SCCB
I2S0 I2S1 I2S2

J1699
SMU/JR Debug Connector
P.16

J790
Backup Battery
Right USB Connector
P.7

J7800
Cardbus Connector
P.48

33MHZ
16/32 BITS
3.3V/5V

PCI BUS
32BITS
33MHZ
3.3V

J7600
Airport Extreme Connector
PAGE 46

U7800
Cardbus
PCI1510
PAGE 48

U7700
USB 2.0
uPD720101
PAGE 47

U7500
BOOTROM
PAGE 45

J9500
Sound (Kazoo) Connector
P.60

Sleep LED
P.18

J9400
Modem Connector
P.59

USB 1.1 (Low/Full Speed)

USB 2.0 (Low/Full/High Speed)

PORT = USB 2.0 (Low/Full/High Speed)

Bluetooth = USB 1.1 (Low/Full Speed)

USB 1.1

J2130
USB Trackpad Connector
P.18

KB LED
P.18

SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE: NONE

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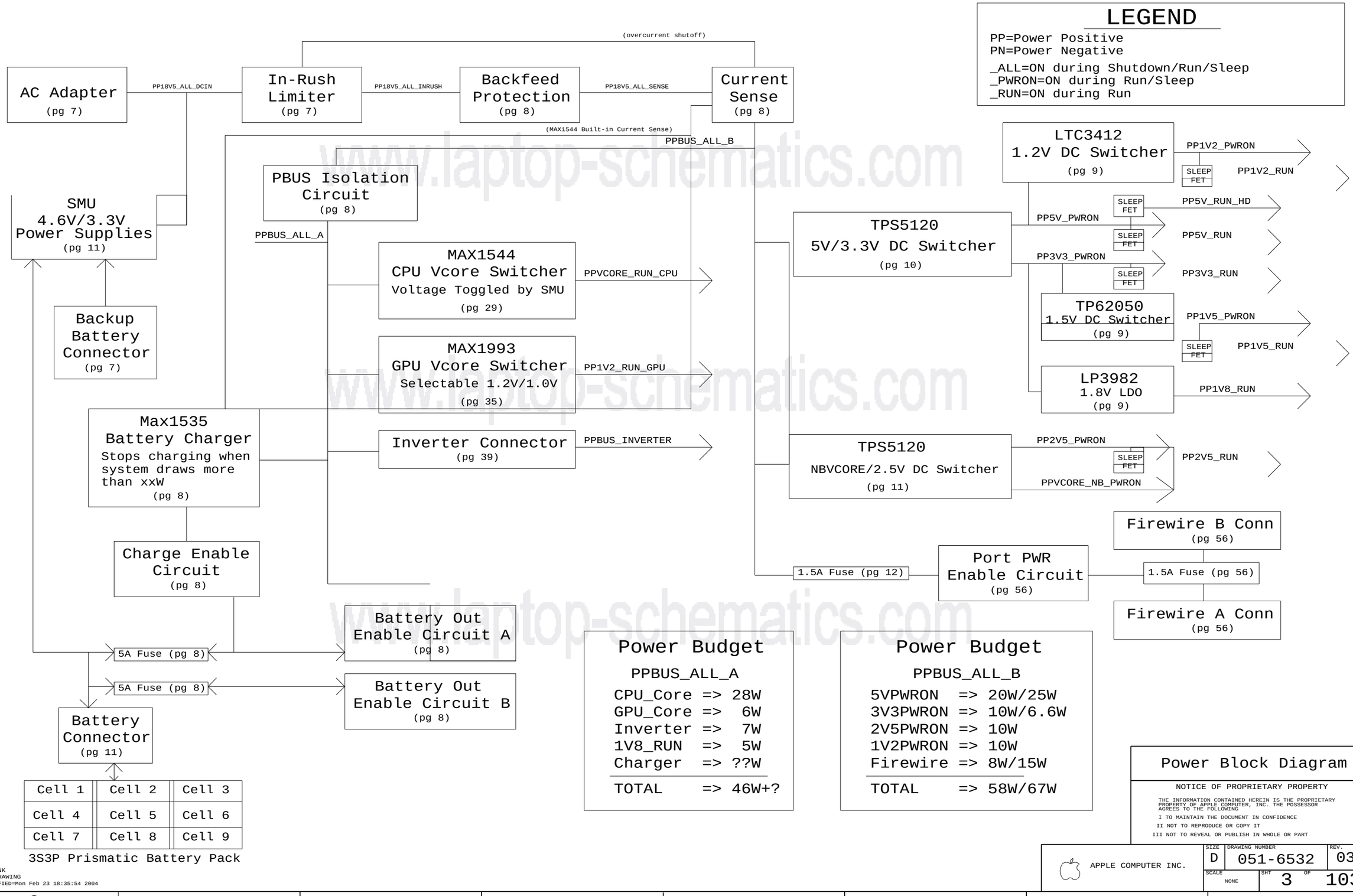

Revision Notes

1/14/04
1) moved Q3001-Q3004,D3001-D3002,R3044,R3046,R3048,R3070,R3050,R3052,R3054 from Page 27 to page 16 to allow sync with Gila
2) moved AGP_Vref (R4802,R4803,C4818) circuit to M11 specific page (49)
3) changed R2191 to pulldown on SYS_LED
** sync with Gila **
1/20/04
1) added 10 mil MIN_LINE_WIDTH and MIN_NECK_WIDTH to BKFD_PROT_EN_L
2) changed MIN_LINE_WIDTH of PPBUS_CHGR_LDO to 10 mils
3) moved 1790 (backup battery/R_VSB connector) to page 18 for syncing with Logic
4) moved J1600 (BT/USB connector) to page 18 for syncing with Logic
5) moved C800,C805 (PBus hold-up caps) to page 19 for syncing with Logic
6) moved Z79900-Z79903 (EMI vias) to page 18 for syncing with Logic
7) moved SP5900-SP5905 and SP9900 to (Speaker wire clips) to page 18 for syncing with Logic
8) moved Z1500-Z1505, Z7910, and Z7911 (Plated screw holes) to page 18 for syncing with Logic
9) moved B5010 to page 18 for syncing with Logic
10) moved J2130 (trackpad connector) to page 18 for syncing with Logic
11) changed C2150 to 20%
12) added 10 mil MIN_LINE_WIDTH and MIN_NECK_WIDTH to KBDLED_ANODE and KDBLED_RETURN
13) changed C2115 to R2116 (3.32K 1% 402) to divide ALS output to 2.5V
** sync with Logic **
2/2/04
1) changed PCI_ from shasta to PCI_SB to allow desktops to insert series R's
2) added pg 73 to alias PCI_SB nets back to PCI to reconnect
3) changed R2150 to 8.25 to reduce LED drive current to 20mA
4) changed Q2113 to FDC700 FET in Q5900
5) changed SMU_ADAPTER_ID to SMU_ONEWIRE
6) added R1820 and R1821 to divide ALS_Cvrtout down to 2.5V
7) added alias from TP_SATA_CLK2SM to SATA_CLK2SM
2/3/04
1) changed PPVCORE_RUN_CPU connection to XW592 to _PP1V5_RUN_FET
2/6/04
1) changed C720 to 0.22uF
2) changed R900 and R818 to 1/2W 1206 10mohm
3) changed C1900 to NO_STUFF
4) removed Q1117 and C1114
5) changed L1115 to 2.2UH IHLP5050CE (152S0152)
6) changed C1121 to 680pF 402
7) changed R1102 to 20K 1% 402
8) added MIN_LINE_WIDTH and MIN_NECK_WIDTH properties to CPUVCORE_CM_N and CPUVCORE_CS_N
9) added MIN_LINE_WIDTH and MIN_NECK_WIDTH properties to ALS1_PHOTODIODE and ALS1_OP_IN
2/7/04
1) changed R5019 to 26.7K 1% to increase GPU Vcore current limit (rdar://3510721)
2) sync with Gila (Q45) to fix several power disconnects
3) added aliases on page 5 to set unused CKE, CS, and MUX controls back to TP
4) sync with Logic (Q43) to get DVO contraints
2/10/04
1) changed R3671 to 100K 0.1% to adjust the Tdiode range
2) changed C3671 to 10uF 20% 6.3V to adjust the Tdiode range
3) changed R3672 to 40.2K 0.1% to adjust the Tdiode range
4) changed R3676 to 100K 0.1% to adjust the Tdiode range
5) changed C3676 to 10uF 20% 6.3V to adjust the Tdiode range
6) changed R3677 to 40.2K 0.1% to adjust the Tdiode range
7) mirrored FL9020 and FL9021 to fix layout
2/11/04
1) changed L970 to 152S0154 (10uH) to reduce size
2/12/04
1) removed 197S0703 as alternate for 197S0037 (25MHz_Vesta_crystal)
2) changed all references to SMU_MANUAL_RESET_L to SMU_RESET_L

2/19/04
1) removed DC current limit circuit (U870 and associated discretes)
2) added BOMOPTION for 2.8V CMU_AVdd_LDO
3) changed R4809 to 2.2 ohm 603, C4811 to 1uF 402, and C4816 to 0.1uF 402 in U3Lite AGP Avdd filter.
4) changed R1610 (series R on SMU_ONEWIRE output) to 0 ohm
5) added R1611 (1K pullup to PP3V3_ALL) on ADAPTER_ID to power SMU_ONEWIRE interface
2/23/04
1) changed C8160-C8160 (SATA_AC_coupling_caps) to 0.01uF per Marvell recommendation
2) added NO_TEST properties to CPUVCORE_GNDSENSE and CPUVCORE_SENSE

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 4 OF 103	

Page Notes

Power aliases required by this page:
N/A (Most aliases are on this page)

Signal aliases required by this page:
N/A (Most aliases are on this page)

BOM options provided by this page:
(NONE)

AGP Signal Aliasing

GPU is D3cold

PCI_RESET_L (48 47 46 45 5) — MAKE_BASE=TRUE — ALIAS — GPU_RESET_L (37 41)

PCI Signal Aliasing

CardBus is D3cold

PCI_RESET_L (48 47 46 45 5)	MAKE_BASE=TRUE	ALIAS	PCI_CBUS_RESET_L (49)
PCI_CLK33M_AIRPORT (6)	MAKE_BASE=TRUE	ALIAS	PCI_CLK_P3 (25)
			PCI_CLK33M_AIRPORT (47)
PCI_CLK33M_CBUS	MAKE_BASE=TRUE	ALIAS	PCI_CLK_GP1 (25)
			PCI_CLK33M_CBUS (49)
PCI_CLK33M_USB2	MAKE_BASE=TRUE	ALIAS	PCI_CLK_GP0 (25)
			PCI_CLK33M_USB2 (48)
SATA_CLK25M	MAKE_BASE=TRUE	ALIAS	PCI_CLK_P4 (25)
			SATA_CLK25M (51)
PCI_CLK33M_SB_EXT (45 25)	MAKE_BASE=TRUE	ALIAS	PCI_CLK_P1 (25)

USB Signal Aliasing

USB "0": Left USB Port

USB2_N<0> (59 6)		ALIAS	USB2_LT_N (17) MAKE_BASE=TRUE
USB2_P<0> (59 6)		ALIAS	USB2_LT_P (17) MAKE_BASE=TRUE
USB2_PWREN<0> (59 6)		ALIAS	LTUSB_PWREN (17) MAKE_BASE=TRUE
USB2_OC<0> (59 6)		ALIAS	LTUSB_OVERCURRENT (17) MAKE_BASE=TRUE

USB "1": Right USB Port

USB2_N<1> (59 6)		ALIAS	USB2_RT_N (17) MAKE_BASE=TRUE
USB2_P<1> (59 6)		ALIAS	USB2_RT_P (17) MAKE_BASE=TRUE
USB2_PWREN<1> (59 6)		ALIAS	RTUSB_PWREN (17) MAKE_BASE=TRUE
USB2_OC<1> (59 6)		ALIAS	RTUSB_OVERCURRENT (17) MAKE_BASE=TRUE

USB "2": BlueTooth

USB2_N<2> (59 6)		ALIAS	USB_BT_N (17) MAKE_BASE=TRUE
USB2_P<2> (59 6)		ALIAS	USB_BT_P (17) MAKE_BASE=TRUE
USB2_PWREN<2> (59)		ALIAS	TP_USB2_PWREN2 MAKE_BASE=TRUE
USB2_OC<2> (59)		ALIAS	USB2_OC2_PU MAKE_BASE=TRUE

USB "3": MicroDash Modem

USB2_N<3> (59 6)		ALIAS	USB_MODEM_N (60) MAKE_BASE=TRUE
USB2_P<3> (59 6)		ALIAS	USB_MODEM_P (60) MAKE_BASE=TRUE
USB2_PWREN<3> (59)		ALIAS	TP_USB2_PWREN3 MAKE_BASE=TRUE
USB2_OC<3> (59)		ALIAS	USB2_OC3_PU MAKE_BASE=TRUE

USB "4": Trackpad/Keyboard

USB2_N<4> (59 6)		ALIAS	USB_TPAD_N (17) MAKE_BASE=TRUE
USB2_P<4> (59 6)		ALIAS	USB_TPAD_P (17) MAKE_BASE=TRUE
USB2_PWREN<4> (59)		ALIAS	TP_USB2_PWREN4 MAKE_BASE=TRUE
USB2_OC<4> (59)		ALIAS	USB2_OC4_PU MAKE_BASE=TRUE

SMU Signal Aliasing

SMU_SLEEP (13)		ALIAS	SYS_SLEEP (10 11 25) MAKE_BASE=TRUE
SMU_WARM_RESET_L (22 13)			SYS_WARM_RESET_L (22 23 45 48) MAKE_BASE=TRUE

Test Point Aliasing

EXT_LED_L		ALIAS	TP_EXT_LED_L MAKE_BASE=TRUE
FAN_RPM2 (13)		ALIAS	TP_FAN_RPM2 MAKE_BASE=TRUE
FAN_TACH2 (13)		ALIAS	TP_FAN_TACH2 MAKE_BASE=TRUE
FAN_TACH3 (13)		ALIAS	TP_FAN_TACH3 MAKE_BASE=TRUE
FAN_TACH4 (13)		ALIAS	TP_FAN_TACH4 MAKE_BASE=TRUE
FAN_TACH5 (13)		ALIAS	TP_FAN_TACH5 MAKE_BASE=TRUE
I2C_SMU_D_SCL (13)		ALIAS	TP_I2C_SMU_D_SCL MAKE_BASE=TRUE
NB_PMR_OBSV (22)		ALIAS	TP_NB_PMR_OBSV MAKE_BASE=TRUE
NB_THMI (22)		ALIAS	TP_NB_THMI MAKE_BASE=TRUE
NB_THMO (22)		ALIAS	TP_NB_THMO MAKE_BASE=TRUE
SATA_RXD_P2_C (50)		ALIAS	TP_SATA_RXD_P2 MAKE_BASE=TRUE
SATA_RXD_N2_C (50)		ALIAS	TP_SATA_RXD_N2 MAKE_BASE=TRUE
SATA_TXD_P2 (50)		ALIAS	TP_SATA_TXD_P2 MAKE_BASE=TRUE
SATA_TXD_N2 (50)		ALIAS	TP_SATA_TXD_N2 MAKE_BASE=TRUE

More Test Point Aliasing

EI_CPU1_CLK_N_R (25)		ALIAS	TP_EI_CPU1_CLK_N MAKE_BASE=TRUE
EI_CPU1_CLK_P_R (25)		ALIAS	TP_EI_CPU1_CLK_P MAKE_BASE=TRUE
CPU1_HTBEN_R (25)		ALIAS	TP_CPU1_HTBEN_R MAKE_BASE=TRUE
EI_CPU1_SYNC_R (25)		ALIAS	TP_EI_CPU1_SYNC_R MAKE_BASE=TRUE
RAM_CKE_R<2> (33)		ALIAS	TP_RAM_CKE_R<2>
RAM_CKE_R<3> (33)		ALIAS	TP_RAM_CKE_R<3>
RAM_CKE_R<6> (33)		ALIAS	TP_RAM_CKE_R<6>
RAM_CKE_R<7> (33)		ALIAS	TP_RAM_CKE_R<7>
RAM_CS_L_R<2> (33)		ALIAS	TP_RAM_CS_L_R<2>
RAM_CS_L_R<3> (33)		ALIAS	TP_RAM_CS_L_R<3>
RAM_CS_L_R<10> (33)		ALIAS	TP_RAM_CS_L_R<10>
RAM_CS_L_R<11> (33)		ALIAS	TP_RAM_CS_L_R<11>
RAM_MUXEN0 (33)		ALIAS	TP_RAM_MUXEN0
RAM_MUXEN4 (33)		ALIAS	TP_RAM_MUXEN4

PBUS PWR

PPBUS_ALL_A (6) — VOLTAGE=18.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PPBUS_ALL_A	(8 17 42)
ALIAS	PPVIN_CPUVCORE	(31)
ALIAS	PPVIN_GPUVCORE	(38)
ALIAS	PPBUS_INV	(42)
ALIAS	PPBUSA_BBATT	(17)

PPBUS_ALL_B (6) — VOLTAGE=18.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PPBUS_ALL_B	(8 17)
ALIAS	PPVIN_5V3VPWRON	(10)
ALIAS	PPVIN_2V5_NBVCORE_PWRON	(11)
ALIAS	PPBUS_FW	(12)
ALIAS	PPBUSB_BBATT	(17)

CPU/GPU Core PWR

PPVCORE_CPU_REG (32 31) — ALIAS — PPVCORE_RUN_CPU (6) MAKE_BASE=TRUE, VOLTAGE=1.1V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil — ALIAS — PPVCORE_CPU (27 29 30 31 32)

PPVCORE_GPU_REG (38) — ALIAS — XW510 (JUMPER OPEN) — ALIAS — PP1V2_RUN_GPU (6) MAKE_BASE=TRUE, VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil — ALIAS — PPVCORE_GPU (37 39)

PPVCORE_GPU_REG: MAKE_BASE=TRUE, VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

Graphic PWR

PP2V5_RUN (5) — R505 0 5% 1/10W FF 805 — PP2V5_GPU (40) — ALIAS — PP2V5_GPU: MAKE_BASE=TRUE, VOLTAGE=2.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP3V3_RUN (6) — R502 0 5% 1/10W FF 805 — PP3V3_GPU (37 39 40) — ALIAS — PP3V3_GPU: MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP3V3_GPU — ALIAS — PP3V3_AGP (35): VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP2V5_RUN (5) — ATI_MEMIO_1V8 R503 0 5% 1/4W FF 1210 — ATI_MEMIO_2V5 R501 0 5% 1/4W FF 1210 — PPVCORE_GPUFB (37 40) — ALIAS — PPVCORE_GPUFB: MAKE_BASE=TRUE, VOLTAGE=1.0V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP3V3_PWRON — R599 100K 5% 1/16W ME 402 — SYS_WARM_RESET_L: MAKE_BASE=TRUE

PP1V8_RUN (6 5) — R504 0 5% 1/10W FF 805 — PP1V8_GPU (37 39 40 41) — ALIAS — PP1V8_GPU: MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP1V5_RUN — R500 0 5% 1/10W FF 805 — PP1V5_GPU_AGP (37 39 40) — ALIAS — PP1V5_GPU: MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

_PWRON PWR

PP5V_PWRON_REG (10) — ALIAS — XW520 (JUMPER OPEN) — ALIAS — PP5V_PWRON: VOLTAGE=5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP5V_PWRON_REG: MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PP5V_PWRON_AUDIO	(61)
ALIAS	PP5V_PWRON_MODEM	(60)
ALIAS	PP5V_PWRON_LTUSB	(17)
ALIAS	PP5V_PWRON_RTUSB	(17)
ALIAS	PP5V_PWRON_SLEEPLED	(19)
ALIAS	PP5V_PWRON_TPAD	(17)
ALIAS	PP5V_PWRON_3V3ALL	(11)
ALIAS	PP5V_PWRON_FAN	(15)
ALIAS	PP5V_PWRON_GPUVCORE	(38)
ALIAS	PP5V_PWRON_SERIAL	(16)
ALIAS	PPVIN_1V2PWRON	(9)
ALIAS	PP5V_PWRON_5VRUN	(10)
ALIAS	PP5V_CBUS	(49)
ALIAS	PP5V_CPUVCORE_VDD	(31)
ALIAS	PP5V_CPUTHERM	(32)

PP3V3_PWRON_REG (10) — ALIAS — XW530 (JUMPER OPEN) — ALIAS — PP3V3_PWRON: VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP3V3_PWRON_REG: MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PP3V3_PWRON_AUDIO	(61)
ALIAS	PP3V3_PWRON_MODEM	(60)
ALIAS	PP3V3_PWRON_SB	(18 21 23 45)
ALIAS	PPPCIG4_PWRON_SB	(21)
ALIAS	PPPCI32_PWRON_SB	(21)
ALIAS	PP3V3_PWRON_USB	(59)
ALIAS	PP3V3_PWRON_BT	(17)
ALIAS	PP3V3_PWRON_ALS1	(19)
ALIAS	PPVIN_1V5PWRON	(9)
ALIAS	PP3V3_PWRON_THERM	(15)
ALIAS	PP3V3_PWRON_3V3RUN	(10)
ALIAS	PP3V3_CBUS	(49)
ALIAS	PP3V3_CPUTHERM	(32)
ALIAS	PP3V3_PWRON_1V8RUN	(9)

PP2V5_PWRON_REG (11) — ALIAS — XW540 (JUMPER OPEN) — ALIAS — PP2V5_PWRON: VOLTAGE=2.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP2V5_PWRON_REG: MAKE_BASE=TRUE, VOLTAGE=2.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PP2V5_PWRON_SB	(21 23 45 56)
ALIAS	PP2V5_PWRON_HT	(44)
ALIAS	PP2V5_PWRON_DIMM	(35)
ALIAS	PP2V5_ENET	(55)
ALIAS	PP2V5_HT	(43)
ALIAS	PPSPD_DIMM	(35)
ALIAS	PP2V5_PWRON_2V5RUN	(11)
ALIAS	PP2V5_PWRON_1V8RUN	(9)
ALIAS	PP2V5_PWRON_RAM	(24 33)

PP1V5_PWRON_REG (9) — ALIAS — XW560 (JUMPER OPEN) — ALIAS — PP1V5_PWRON: VOLTAGE=1.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP1V5_PWRON_REG: MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PPVCORE_PWRON_PULSAR	(24)
ALIAS	PP1V5_PWRON_1V5RUN	(9)
ALIAS	PP1V5_PWRON_NB_AVDD	(26 33 36 43)

PP1V2_PWRON_REG (9) — ALIAS — XW561 (JUMPER OPEN) — ALIAS — PP1V2_PWRON: VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP1V2_PWRON_REG: MAKE_BASE=TRUE, VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PP1V2_PWRON_DISK_SB	(50)
ALIAS	PP1V2_PWRON_HT	(44)
ALIAS	PP1V2_PWRON_SB	(23)
ALIAS	PPVCORE_PWRON_SB	(21)
ALIAS	PP1V2_PWRON_1V2RUN	(9)

ONLY ONE CAN BE CLOSED Between XW560/XW561!!!

PPVCORE_NB_REG (11) — ALIAS — XW552 (JUMPER OPEN) — ALIAS — PPVCORE_PWRON_NB (20)

PPVCORE_NB_REG: MAKE_BASE=TRUE, VOLTAGE=1.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PPVCORE_PWRON_NB: MAKE_BASE=TRUE, VOLTAGE=1.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ONLY ONE CAN BE CLOSED Between XW550/XW551!!!

XW552 Always close

GND — VOLTAGE=0V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

Chassis Grounds

GND_CHASSIS_DVI (17)	VOLTAGE=0V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil	ALIAS	GND_CHASSIS_DVI_TOP (42)
GND_CHASSIS_INVERTER (17)	VOLTAGE=0V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil	ALIAS	GND_CHASSIS_INV (42)
GND_CHASSIS_LVDS (6)	VOLTAGE=0V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil	ALIAS	GND_CHASSIS_LVDS (42)
		ALIAS	GND_CHASSIS_ENET (55)
		ALIAS	GND_CHASSIS_FW_PORT1 (58)
		ALIAS	GND_CHASSIS_FW_PORT2 (58)
		ALIAS	GND_CHASSIS_DVI_BOTTOM (42)
GND_CHASSIS_IO (6 17)	VOLTAGE=0V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil	ALIAS	GND_CHASSIS_SVIDEO (42)

_RUN PWR

PP3V3_ALL_LDO (11) — ALIAS — PP3V3_ALL: VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PP3V3_ALL_ACIN	(7)
ALIAS	PP3V3_ALL_DCILIM	
ALIAS	PP3V3_ALL_HALLEFFECT	(17)
ALIAS	PP3V3_ALL_RTC	(13)
ALIAS	PP3V3_ALL_SMU	(13 16 18)

2.5V SMU VRef

PP2V5_SMU_VREF (32) — MAKE_BASE=TRUE — ALIAS — PPVREF_SMU (13)

PP5V_RUN_FET (10) — ALIAS — PP5V_RUN: VOLTAGE=5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PP5V_RUN_KBDLED	(19)
ALIAS	PP5V_UATA	(52)
ALIAS	PPBU_RUN_FW	(12)
ALIAS	PP5V_RUN_CPU	(16 29)

PP5V_RUN_HD_FET (10) — ALIAS — PP5V_RUN_HD (6): VOLTAGE=5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PP5V_PATA	(52)
ALIAS	PP5V_RUN_AUDIO	(61)

PP3V3_RUN_FET (10) — ALIAS — PP3V3_RUN: VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PP3V3_SATABR	(51)
ALIAS	PP3V3_PATA	(52)
ALIAS	PPVIO_PCI_USB2	(48)
ALIAS	PPVIO_PCI_CBUS	(49)
ALIAS	PP3V3_PCI	(23 45 46 47 48 49)
ALIAS	PP3V3_SB_PCI	(45)
ALIAS	PP3V3_CPUVCORE	(31)
ALIAS	PP3V3_RUN_FAN	(15)
ALIAS	PP3V3_RUN_SI	(41)

PP2V5_RUN_FET (11) — ALIAS — PP2V5_RUN: VOLTAGE=2.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PP2V5_PCI	(49)
ALIAS	PP2V5_RUN_CPU	(29)

PP1V8_RUN_LDO (9) — ALIAS — XW518 (JUMPER OPEN) — ALIAS — PP1V8_RUN: VOLTAGE=1.8V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil — ALIAS — PP1V8_SATABR (51)

PP1V8_RUN_LDO: MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP1V5_RUN_FET (9 5) — ALIAS — PP1V5_RUN: VOLTAGE=1.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PP1V5_AGP	(36 37)
ALIAS	PPVCORE_PULSAR	(24)

PP1V2_RUN_FET (9) — ALIAS — PP1V2_RUN: VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

ALIAS	PP1V2_HT	(22 43)
ALIAS	PP1V2_PULSAR	(24)

ONLY ONE CAN BE CLOSED Between XW590/XW591!!!

XW590 (JUMPER OPEN) — ALIAS — PP1V2_EI_NB (18 26): VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

XW591 (JUMPER OPEN)

PP1V5_RUN_FET (9 5) — XW592 (JUMPER OPEN) — PP1V2_EI_CPU (18 27 28 29): VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

Power Connections

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 5 OF	103

FUNCTIONAL TEST POINTS

Wireless
Within 1" of connector

FUNC_TEST=TRUE
PCI_AD<0> 45 46 47 48 49 62
PCI_AD<1> 45 46 47 48 49 62
PCI_AD<2> 45 46 47 48 49 62
PCI_AD<3> 45 46 47 48 49 62
PCI_AD<4> 45 46 47 48 49 62
PCI_AD<5> 45 46 47 48 49 62
PCI_AD<6> 45 46 47 48 49 62
PCI_AD<7> 45 46 47 48 49 62
PCI_AD<8> 45 46 47 48 49 62
PCI_AD<9> 45 46 47 48 49 62
PCI_AD<10> 45 46 47 48 49 62
PCI_AD<11> 45 46 47 48 49 62
PCI_AD<12> 45 46 47 48 49 62
PCI_AD<13> 45 46 47 48 49 62
PCI_AD<14> 45 46 47 48 49 62
PCI_AD<15> 45 46 47 48 49 62
PCI_AD<16> 45 46 47 48 49 62
PCI_AD<17> 45 46 47 48 49 62
PCI_AD<18> 45 46 47 48 49 62
PCI_AD<19> 45 46 47 48 49 62
PCI_AD<20> 45 46 47 48 49 62
PCI_AD<21> 45 47 48 49 62
PCI_AD<22> 45 47 48 49 62
PCI_AD<23> 45 47 48 49 62
PCI_AD<24> 45 46 47 48 49 62
PCI_AD<25> 45 46 47 48 49 62
PCI_AD<26> 45 46 47 48 49 62
PCI_AD<27> 45 46 47 48 49 62
PCI_AD<28> 45 46 47 48 49 62
PCI_AD<29> 45 46 47 48 49 62
PCI_AD<30> 45 46 47 48 49 62
PCI_AD<31> 45 46 47 48 49 62
PCI_FRAME_L 45 47 48 49 62
PCI_TRDY_L 45 47 48 49 62
PCI_IRDY_L 45 47 48 49 62
PCI_DEVSEL_L 45 47 48 49 62
PCI_STOP_L 45 47 48 49 62
PCI_PAR 45 47 48 49 62
PCI_CBE_L<0> 45 47 48 49 62
PCI_CBE_L<1> 45 47 48 49 62
PCI_CBE_L<2> 45 47 48 49 62
PCI_CBE_L<3> 45 47 48 49 62
PCI_SLOTA_REQ_L 45 47
PCI_SLOTA_GNT_L 45 47
PCI_SLOTA_INT_L 23 47
PCI_SLOTA_IDSEL 47
PCI_CLK33M_AIRPORT 5
TP_AIRPORT_PME_L 47
TP_AIRPORT_RF_DISABLE 47
AIRPORT_CLKRUN_L_PD 47
PP3V3_RUN 5 6 X 4

GND x 4

DVI/VGA
Within 1" of connector

TMDS_DN<0> 41 42 62
TMDS_DP<0> 41 42 62
TMDS_DN<1> 41 42 62
TMDS_DP<1> 41 42 62
TMDS_DN<2> 41 42 62
TMDS_DP<2> 41 42 62
TMDS_CONN_CLKN 42 62
TMDS_CONN_CLKP 42 62
VGA_R 42
VGA_G 42
VGA_B 42
VGA_VSYNC 42
VGA_HSYNC 42
DVI_DDC_CLK_UF 42
DVI_DDC_DATA_UF 42
DVI_HPD_UF 42
PP5V_RUN_DDC 42
GND_CHASSIS_IO 5 17

GND x 1

LVDS
Within 1" of connector

LVDS_L0N 39 42
LVDS_L0P 39 42
LVDS_L1N 39 42
LVDS_L1P 39 42
LVDS_L2N 39 42
LVDS_L2P 39 42
CLKLVDS_LN 39 42
CLKLVDS_LP 39 42
LVDS_U0N 39 42
LVDS_U0P 39 42
LVDS_U1N 39 42
LVDS_U1P 39 42
LVDS_U2N 39 42
LVDS_U2P 39 42
CLKLVDS_UN 39 42
CLKLVDS_UP 39 42
LVDS_DDC_CLK 39 42
LVDS_DDC_DATA 39 42
PP3V3_LCD 42
GND_CHASSIS_LVDS 5

2 x GND

INVERTER
Within 1" of connector

PPBUS_ALL_A 5 6
PP5V_INVERTER 42
BRIGHT_PWM 42

1 x GND

S-Video
Within 1 of connector

TV_GND1 42
TV_GND2 42
TV_C 42
TV_Y 42
TV_COMP 42

PATA (SATA Bridge)
Within 1" of connector

PATA_DD<0> 51 52
PATA_DD<1> 51 52
PATA_DD<2> 51 52
PATA_DD<3> 51 52
PATA_DD<4> 51 52
PATA_DD<5> 51 52
PATA_DD<6> 51 52
PATA_DD<7> 51 52
PATA_DD<8> 51 52
PATA_DD<9> 51 52
PATA_DD<10> 51 52
PATA_DD<11> 51 52
PATA_DD<12> 51 52
PATA_DD<13> 51 52
PATA_DD<14> 51 52
PATA_DD<15> 51 52
PATA_DMARQ_R 52
PATA_DMACK_L 51 52
PATA_DA<0> 51 52
PATA_DA<1> 51 52
PATA_DA<2> 51 52
PATA_CS0_L 51 52
PATA_CS1_L 51 52
PATA_RESET_L 51 52
PATA_DSTROBE_R 52
PATA_HSTROBE 51 52
PATA_STOP 51 52
PATA_INTRQ_R 52
PP5V_RUN_HD 5 x4
PPLOGIC_PATA 52 x3

GND x 5

Battery Conn
Within 1" of connector

PPBATT_ALL_F 7 x2
I2C_SMU_E_SCL 13 18 (I2C_BATT_SCL)
I2C_SMU_E_SDA 13 18 (I2C_BATT_SDA)
BATT_DET_L 7
GND_BATT 7 x2

DC-in Connectors
Within 1" of connector

PP18V5_ALL_DCIN 7 11 x 3

GND x 3

UATA (Optical)
Within 2" of connector

UATA_DD<0> 50 52
UATA_DD<1> 50 52
UATA_DD<2> 50 52
UATA_DD<3> 50 52
UATA_DD<4> 50 52
UATA_DD<5> 50 52
UATA_DD<6> 50 52
UATA_DD<7> 50 52
UATA_DD<8> 50 52
UATA_DD<9> 50 52
UATA_DD<10> 50 52
UATA_DD<11> 50 52
UATA_DD<12> 50 52
UATA_DD<13> 50 52
UATA_DD<14> 50 52
UATA_DD<15> 50 52
UATA_DMARQ_R 52
UATA_DMACK_L 50 52
UATA_DA<0> 50 52
UATA_DA<1> 50 52
UATA_DA<2> 50 52
UATA_CS0_L 50 52
UATA_CS1_L 50 52
UATA_RESET_L 50 52
UATA_DSTROBE_R 52
UATA_HSTROBE 50 52
UATA_STOP 50 52
UATA_INTRQ_R 52
PP5V_RUN x4

GND x 5

Trackpad
Within 3" of connector

I2C_SMU_B_SCL 13 18 (I2C_DS1775_SCL)
I2C_SMU_B_SDA 13 18 (I2C_DS1775_SDA)
SYS_OVERTEMP_L 13 15 17 23 25
USB2_N<4> 5 59
USB2_P<4> 5 59
KBDLED_ANODE 17 19
KBDLED_RETURN 17 19
SYS_DOOR_AJAR (SYS_LID_OPEN)
SYS_POWER_BUTTON_L 6 13 16 17 42
PP3V3_PWRON 17 25
PP5V_PWRON 6 11
PP3V3_ALL 6
PP3V3_RUN 5 6

Firewire B
Within 1" of connector

FW_PORT1_TPA_P_FL 58
FW_PORT1_TPA_N_FL 58
FW_PORT1_TPB_P_FL 58
FW_PORT1_TPB_N_FL 58
FW_PORT1_AREF 58
GND_FW_PORT1_VG 58
PPFW_PORT1_VP 58

Firewire A
Within 1" of connector

FW_PORT2_TPA_P_FL 58
FW_PORT2_TPA_N_FL 58
FW_PORT2_TPB_P_FL 58
FW_PORT2_TPB_N_FL 58
PPFW_PORT2_VP 58
GND_FW_PORT2_VG 58

Fan Connectors
Within 2" of connector

FAN_RPM0 13 15
FAN_TACH0 13 15
FAN_RPM1 13 15
FAN_TACH1 13 15
PP5V_PWRON 6 11 x2 one by each fan

GND x 2 - one by each fan

BT/USB Flex
Within 2" of connector

USB2_N<2> 5 59 (USB_BT_N)
USB2_P<2> 5 59 (USB_BT_P)
USB2_N<0> 5 59 (USB2_LT_N)
USB2_P<0> 5 59 (USB2_LT_P)
USB2_PWREN<0> 5 59 (LTUSB_PWREN)
ALS0_OUT 13 17
USB2_OC<0> 5 59 (LTUSB_OVERCURRENT)
ALS_GAIN_BOOST 13 17 19
ADAPTER_ID 17

PP3V3_PWRON x 1
PP5V_PWRON x 1
GND x 1

Backup Battery/USB Flex
Within 2" of connector

PPBUS_ALL_B 5 6
PPBUS_ALL_A 5 6
SYS_POWERUP 14
USB2_N<1> 5 59 (USB2_RT_N)
USB2_P<1> 5 59 (USB2_RT_P)
USB2_PWREN<1> 5 59 (RTUSB_PWREN)
USB2_OC<1> 5 59 (RTUSB_OVERCURRENT)

PP5V_PWRON x 1
GND x 1

Sound Connector
Within 2" of connector

I2S0_DEV_TO_SB_DTI_F 61
I2S0_BITCLK_F 61
I2S0_MCLK_F 61
I2S0_SYNC_F 61
I2S0_SB_TO_DEV_DTO_F 61
I2S2_DEV_TO_SB_DTI_F 61
I2S2_BITCLK_F 61
I2S2_SYNC_F 61
AUDIO_GPIO_11 23 61
AUDIO_EXT_MCLK_SEL 23 61
AUDIO_LO_MUTE_L 23 61
AUDIO_SPKR_MUTE_L 23 61
AUDIO_LO_DET_L 23 61
AUDIO_LO_OPTICAL_PLUG_L 23 61
AUDIO_LI_DET_L 23 61
AUDIO_LI_OPTICAL_PLUG_L 23 61
I2S0_RESET_L_F 61
I2S2_RESET_L_F 61
SLEEPLED_ANODE 19 61 x4
GND_AUDIO 61 x3
PP5V_PWRON_AUDIO 61 x2
PP3V3_PWRON_AUDIO 61

GND x 2

Modem Connector
Within 3" of connector

I2S1_SB_TO_DEV_DTO 16 23 60
I2S1_BITCLK 16 23 60
I2S1_SYNC 16 23 60
I2S1_RESET_L 16 23 60
I2S1_MCLK 16 23 60
I2S1_DEV_TO_SB_DTI 16 23 60
USB2_N<3> 5 59 (USB_MODEM_N)
USB2_P<3> 5 59 (USB_MODEM_P)
MODEM_RING2SYS_L 23 60
UDASH_SDOWN 23 60
I2C_SB_SCL 18 23 (I2C_MODEM_SCL)
I2C_SB_SDA 18 23 (I2C_MODEM_SDA)

ROM Control
Within 2" of U7500

ROM_ONBOARD_CS_L 46 47
ROM_OE_L 45 46 47
ROM_CS_L 45 46 47
ROM_WE_L 45 46 47

MISC

JTAG_NB_TMS 22
JTAG_NB_TDI 22
JTAG_NB_TDO 22
JTAG_NB_TCK 22
JTAG_NB_TRST_L 22
JTAG_SB_TMS 18 23
JTAG_SB_TDI 18 23
JTAG_SB_TDO 23
JTAG_SB_TCK 18 23
JTAG_SB_TRST_L 18 23
JTAG_VESTA_TMS 12
JTAG_VESTA_TDI 12
JTAG_VESTA_TDO 12
JTAG_VESTA_TCK 12
JTAG_VESTA_TRST_L 12
JTAG_CPU_TMS 18 27 28
JTAG_CPU_TDI 18 27 28
JTAG_CPU_TDO 18 27 28
JTAG_CPU_TCK 18 27 28
JTAG_CPU_TRST_L 27 28
SMU_RESET_L 13 16 19
SYS_POWER_BUTTON_L 6 13 16 17 42
SYS_RESET_BUTTON_L 13 16
PP1V8_RUN 5
PP2V5_PWRON
PPBUS_ALL_B 5 6
PP3V3_ALL 6
PPVCORE_RUN_CPU 5
PP1V2_RUN_GPU 5
(SMU_BOOT_BUSY) CPU_VID<4> 13 31
(SMU_BOOT_SCLK) CPU_VID<5> 13
SMU_BOOT_CNVSS 13 16
SMU_BOOT_TXD 13 16
SMU_BOOT_RXD 13 16
(SMU_BOOT_CE) SYS_POWERUP_L 13 14

Functional Testpoints

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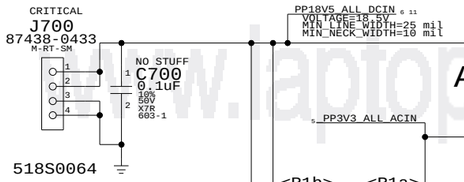
SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 6 OF 103	

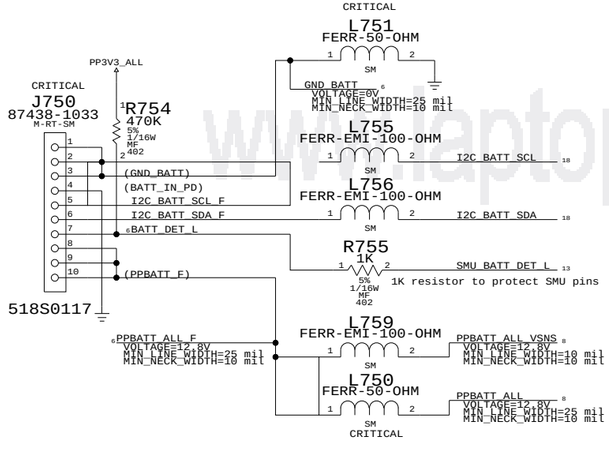
DC Power Input

(DC-In jack and associated circuit are on separate baord)



DC Inrush Limiter

Main Battery Connector



Place L759 as close to J750 as possible

Power Connectors

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 7 OF 103	

DC-IN Input Current Limiter

Place U800 and U870 near R800

CRITICAL
Q850
SI4405DY
SO-8

PP18V5_ALL_INRUSH

PP18V5_ALL_SENSE
VOLTAGE=18.5V
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

R850 49.9K 1% 1/16W MF 402

BKFD_PROT_EN_L_DIV
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil

C851 0.1uF 20% 25V CERM 603

R851 68K 5% 1/16W MF 402

BKFD_PROT_EN_L
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil

Q800
2N7002DW
SOT-363
SMU_ACIN

CRITICAL
R800
0.010
1% 1/2W ME 1206

PPBUS_ALL_B

CRITICAL
Q880
SI4435DY
SOI

PPBUS_ALL_A

R880 470K 5% 1/16W MF 402

CHGR_PBUS_EN_L_DIV
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil

R881 330K 5% 1/16W MF 402

SMU_ACIN

R882 100K 5% 1/16W MF 402

DP800
BAS16TW
SOT-363

CHGR_PBUS_EN_L

Q882
2N7002DW
SOT-363

CHGR_ACIN_RC

C882 0.01UF 10% 16V CERM 402

Keep short and route as pair

Battery Switch-over Circuit

PPBATT_ALL

Battery Charge Path

Battery charge FET is open when not charging

F895 5AMP-125V SM-2

F899 5AMP-125V SM-2

CRITICAL
Q890
SI4435DY
SOI

PPBATT_ALL_FUSEA
VOLTAGE=12.6V
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

PPBATT_ALL_FUSEB
VOLTAGE=12.6V
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

PPBATT_CHGR_OUT

R890 470K 5% 1/16W MF 402

PPBUS_ALL_A

PPBUS_ALL_B

CRITICAL
Q895
SUD45P03
TO-252

CRITICAL
Q899
SUD45P03
TO-252

R895 470K 5% 1/16W MF 402

R899 470K 5% 1/16W MF 402

CHGR_CHARGE_EN_L_DIV

BATT_PBUSB_EN_L
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil

R891 100K 5% 1/16W MF 402

BATT_PBUSA_EN_L
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil

R896 100K 5% 1/16W MF 402

R898 100K 5% 1/16W MF 402

CHGR_CHARGE_EN_L

BATT_PBUS_EN_L

Q882
2N7002DW
SOT-363
SMU_CHARGE_BATT

R892 100K 5% 1/16W MF 402

SMU_ACIN_L

DP800
BAS16TW
SOT-363

R897 158K 1% 1/16W MF 402

Q800
2N7002DW
SOT-363

BATT_ACIN_L_RC

C897 10UF 20% 25V CERM 805

When AC is disconnected, P-channel FETs turn on
RC time is 480K * 10uF @ 3.3V
When AC is connected, P-channel
FETs are quickly turned off (diode)

SMBus Battery Charger

(PP18V5_ALL_SENSE)
(PP18V5_ALL)

R801 4.7 5% 1/16W MF 402

R802 4.7 5% 1/16W MF 402

C801 0.47UF 20% 50V CERM 1206

C802 0.47UF 20% 50V CERM 1206

CHGR_REF

R824 100K 1% 1/16W MF 402

R820 100K 1% 1/16W MF 402

C830 0.1UF 20% 10V CERM 402

C825 1UF 20% 10V CERM 603

PP5V4_CHGR_LDO
VOLTAGE=5.4V
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil

R830 100K 5% 1/16W MF 402

R826 33 5% 1/16W MF 402

PPBUS_ALL_A

NO STUFF
D800
1N914
SOT23

NO STUFF
R805 100K 1% 1/16W MF 402

NO STUFF
R806 13K 1% 1/16W MF 402

C800 1uF 20% 25V CERM 805

VDD_LDO

C831 0.1UF 20% 25V CERM 402

C805 4.7uF 20% 25V CERM 1206

C806 4.7uF 20% 25V CERM 1206

C807 4.7uF 20% 25V CERM 1206

C808 4.7uF 20% 25V CERM 1206

CHGR_CSSP
CHGR_CSSN
CHGR_DCIN
CHGR_ACIN
I2C_CHGR_SCL
I2C_CHGR_SDA
CHGR_CMIN
CHGR_VMAX
CHGR_CCS
CHGR_CCI
CHGR_CCV
CHGR_CSIP
CHGR_CSIN

U800
MAX1535A
QFN
CRITICAL

SMU_ACIN

R823 0 5% 1/16W MF 402

CHGR_DHIV
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil

CHGR_DHI
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

CHGR_DLOV_RC
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil

CHGR_DLO
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

CHGR_DLOV
CHGR_DAC
CHGR_THM
CHGR_REF

CRITICAL
Q810
SI4835BDY
SOI

PPBATT_CHGR_RSNS
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

PPBATT_CHGR_SW
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

CRITICAL
L810
10uH
SM1

CRITICAL
R810
0.010
1% 1/2W ME 1206

PPBATT_CHGR_OUT
VOLTAGE=12.6V
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

R811 1 5% 1/16W MF 603

R812 1 5% 1/16W MF 603

CRITICAL
Q811
SI4336DY
SO-8

C811 0.001uF 10% 50V CERM 402

C812 4.7uF 20% 25V CERM 1206

C813 4.7uF 20% 25V CERM 1206

C814 4.7uF 20% 25V CERM 1206

C815 4.7uF 20% 25V CERM 1206

C816 4.7uF 20% 25V CERM 1206

CRITICAL
C818
33UF
20% 25V ELEC SM1

R827 0 5% 1/16W MF 402

R828 0 5% 1/16W MF 402

R825 20.5K 1% 1/16W MF 402

R822 30K 1% 1/16W MF 402

R821 169K 1% 1/16W MF 402

C822 0.01UF 20% 16V CERM 402

CHGR_CCS_RC
CHGR_CCI_RC
CHGR_CCV_RC

C824 0.01UF 20% 16V CERM 402

C823 0.01UF 20% 16V CERM 402

C826 1UF 20% 10V CERM 603

C829 1UF 20% 10V CERM 603

R829 100K 5% 1/16W MF 402

C820 0.1UF 20% 16V CERM 402

XW800 SM

D810 SM MBRS140T3

C827 0.1UF 20% 25V CERM 603

C828 0.1UF 20% 25V CERM 603

GND_CHGR
VOLTAGE=0V
MIN_LINE_WIDTH=15 mil
MIN_NECK_WIDTH=10 mil

SMU_CHARGE_BATT_L

PPBATT_ALL_VSNS

Q877
2N7002DW
SOT-363
SMU_CHARGE_BATT

SMBus Battery Charger

APPLE COMPUTER INC.

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D	051-6532	03
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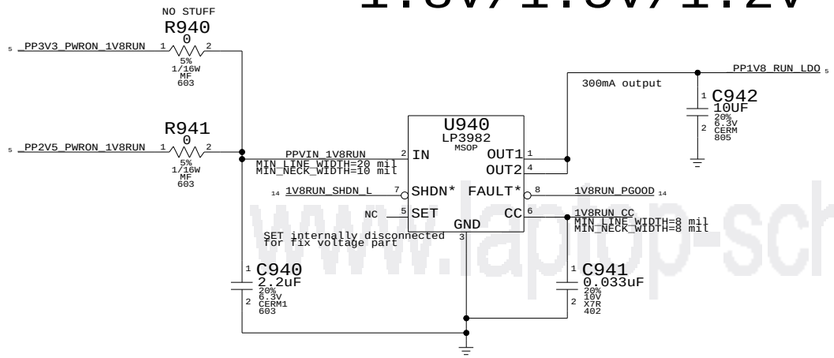
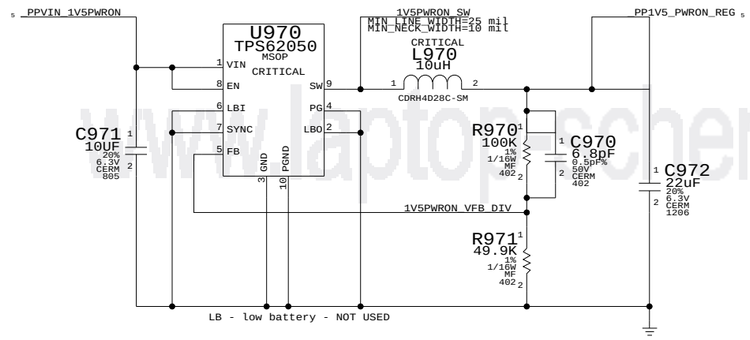
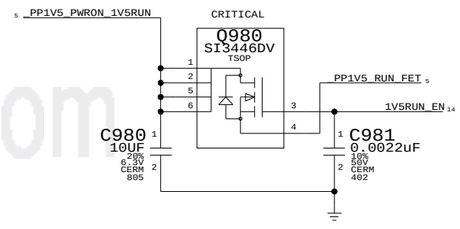
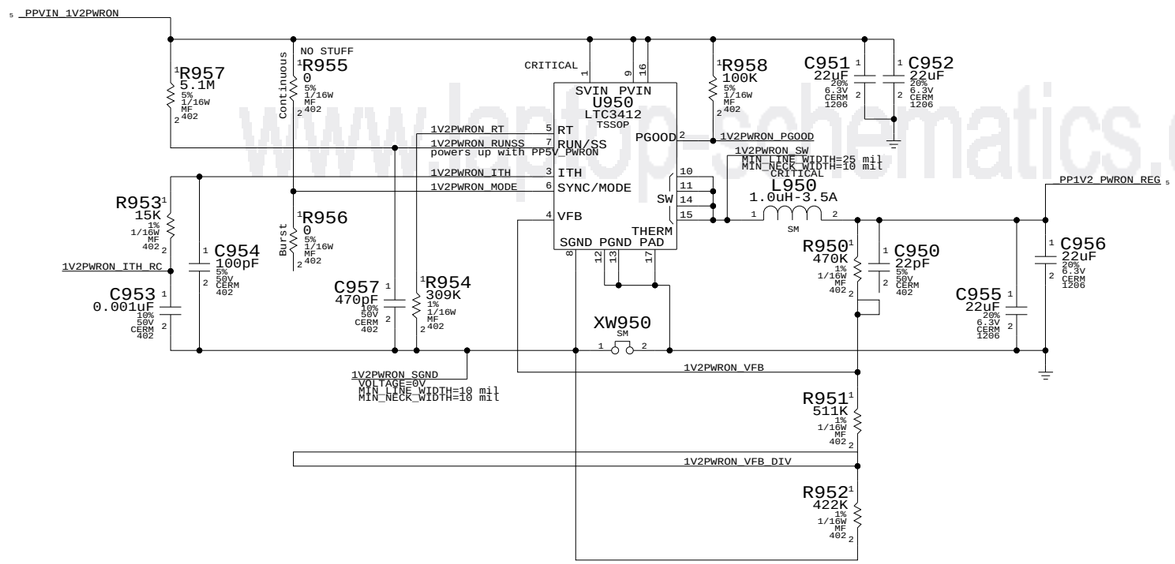
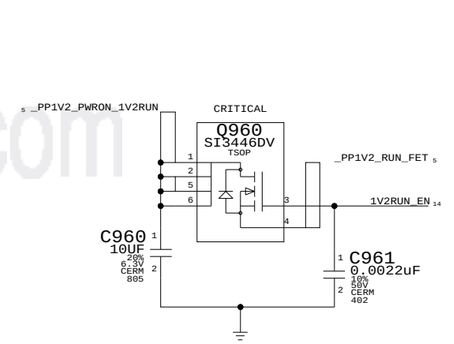
1.8V/1.5V/1.2V MAIN SUPPLIES











1.8V/1.5V Supplies

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
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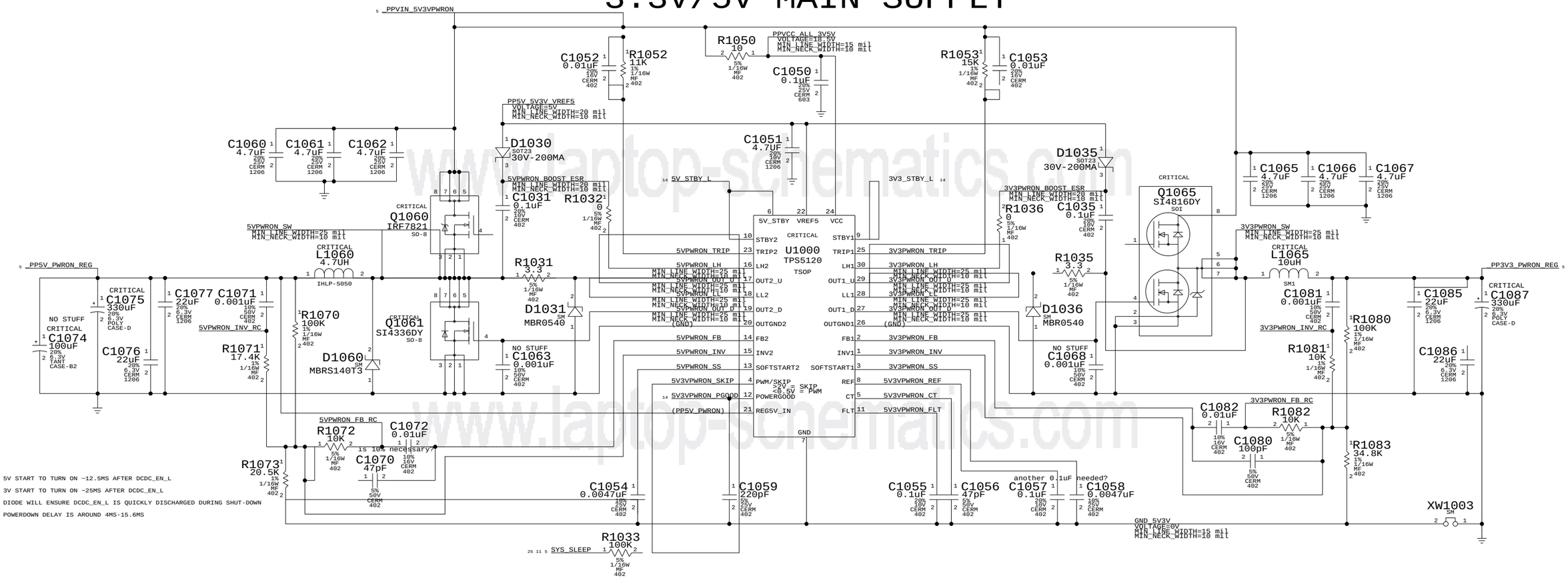
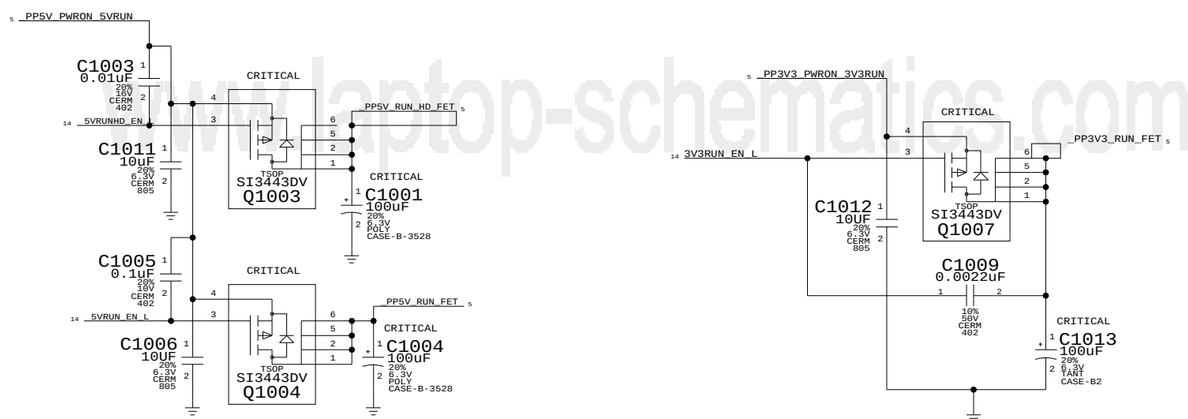
3.3V/5V MAIN SUPPLY





3.3V/5V REGULATOR

NOTICE OF PROPRIETARY PROPERTY

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APPLE COMPUTER INC.

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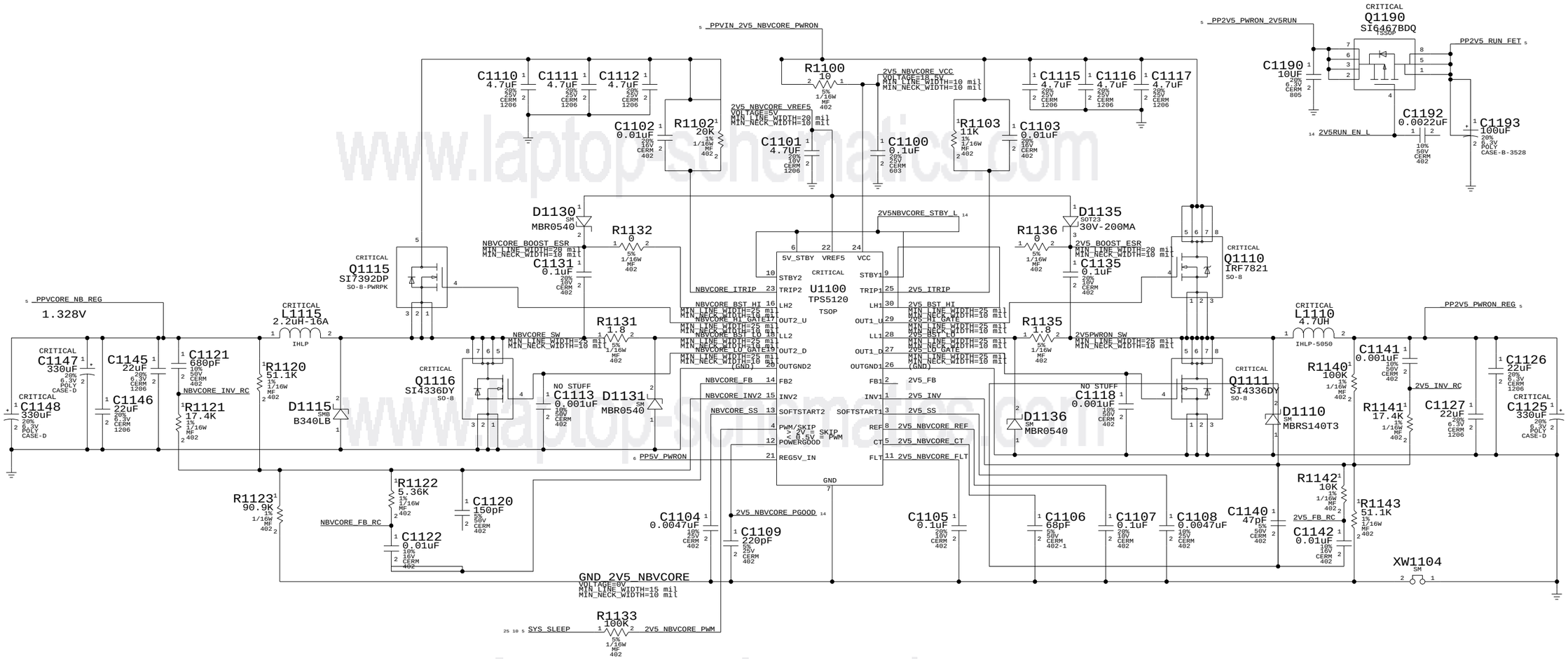
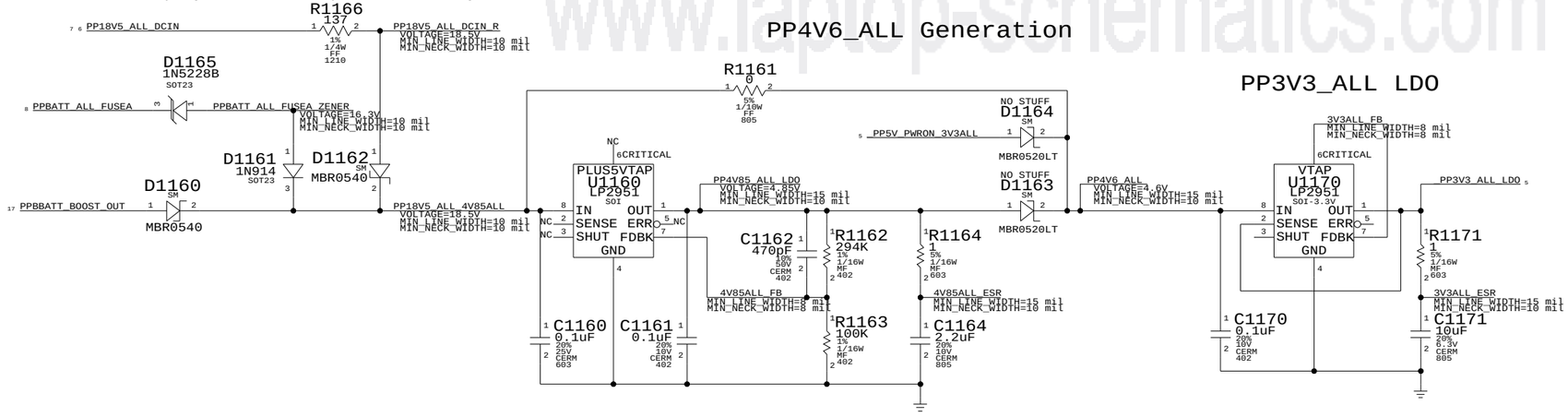
D	051-6532	03

SCALE	SHT
NONE	10 OF 103

2.5V/NBVCORE MAIN SUPPLIES



Bootstrap system from adapter or battery



PP4V6_ALL Generation

PP3V3_ALL LDO

2.5V/NBVCORE/PMU SUPPLIES

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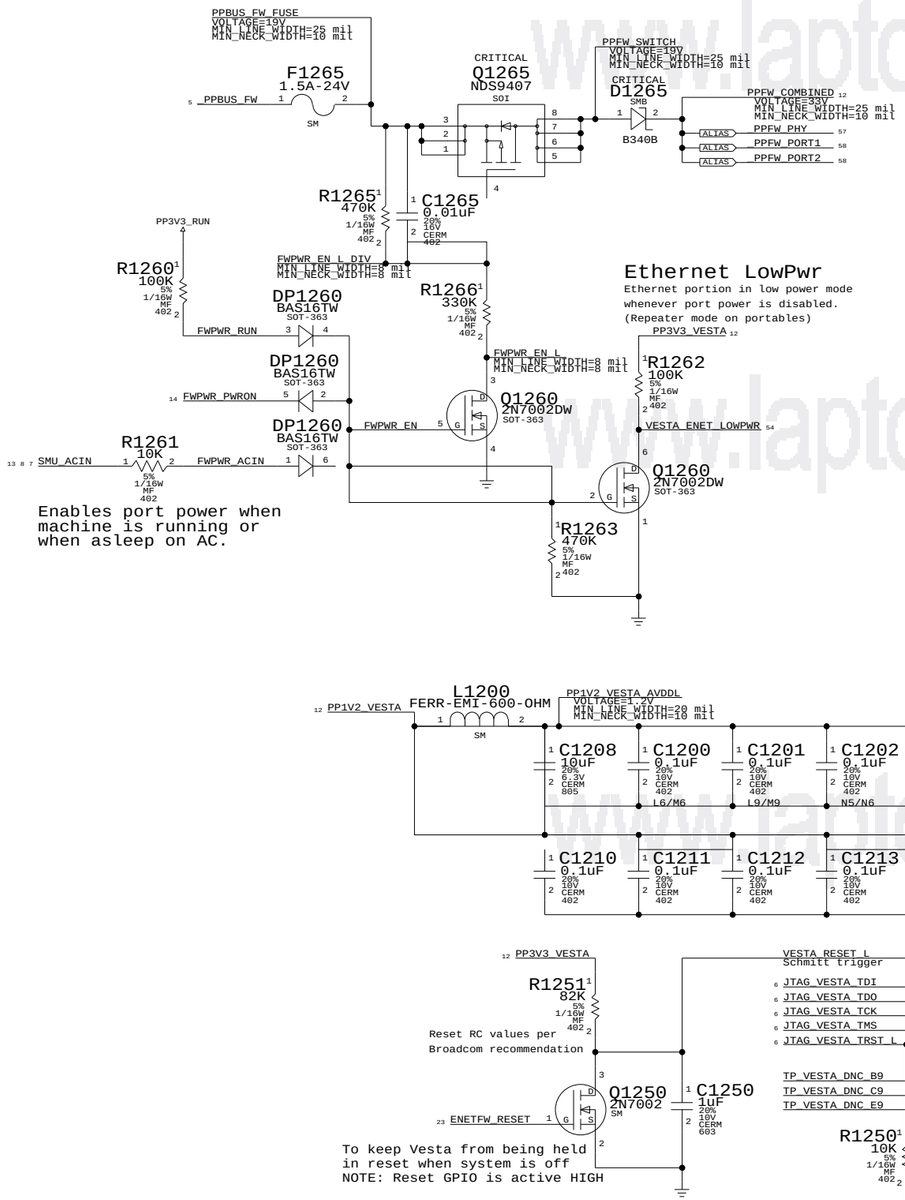
Page Notes

Power aliases required by this page:
- _PPBUS_FW (system supply for bus power)
- _PP12V_RUN_FW (backup PHY power)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

Port Power Switch

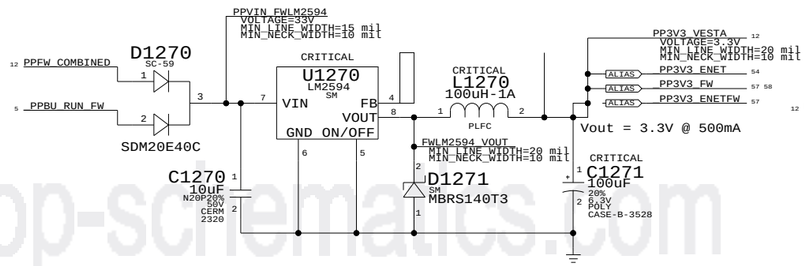


Ethernet LowPwr

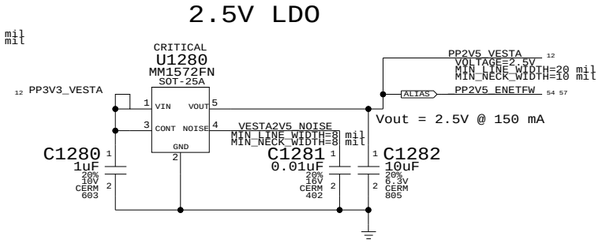
Ethernet portion in low power mode whenever port power is disabled. (Repeater mode on portables)

Enables port power when machine is running or when asleep on AC.

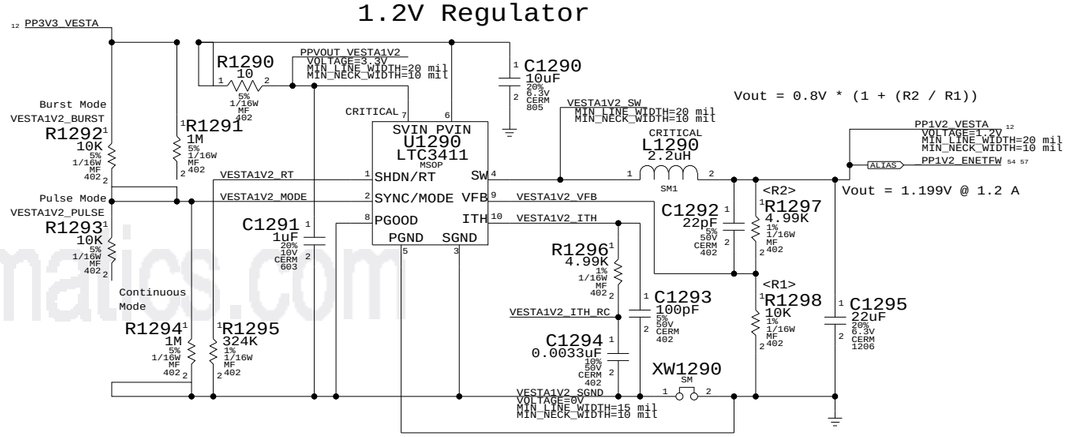
3.3V Regulator

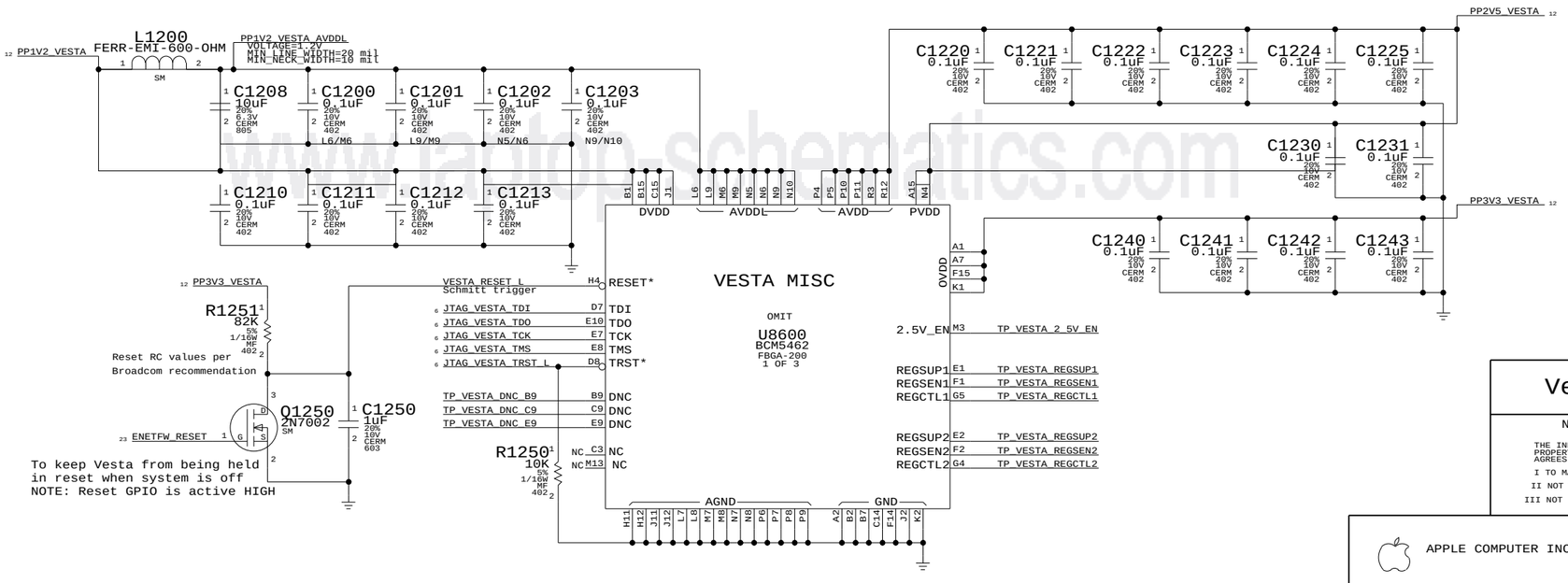


2.5V LDO



1.2V Regulator





Master: Link

Vesta Core / Misc

APPLE COMPUTER INC.

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_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:03:46 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	15 MIL SPACING		SMU_CLK10M_XIN 13
	15 MIL SPACING		SMU_CLK10M_XOUT 13
	15 MIL SPACING		SMU_CLK10M_XOUT_R 13
RTC_CLK32K_XTAL	15 MIL SPACING		RTC_CLK32K_X1 13
	15 MIL SPACING		RTC_CLK32K_X2 13

Page Notes

Power aliases required by this page:
- _PP3V3_ALL_SMU
- _PP3V3_ALL_RTC
- _PP3V3_PWRON_SMU
- _PPVREF_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

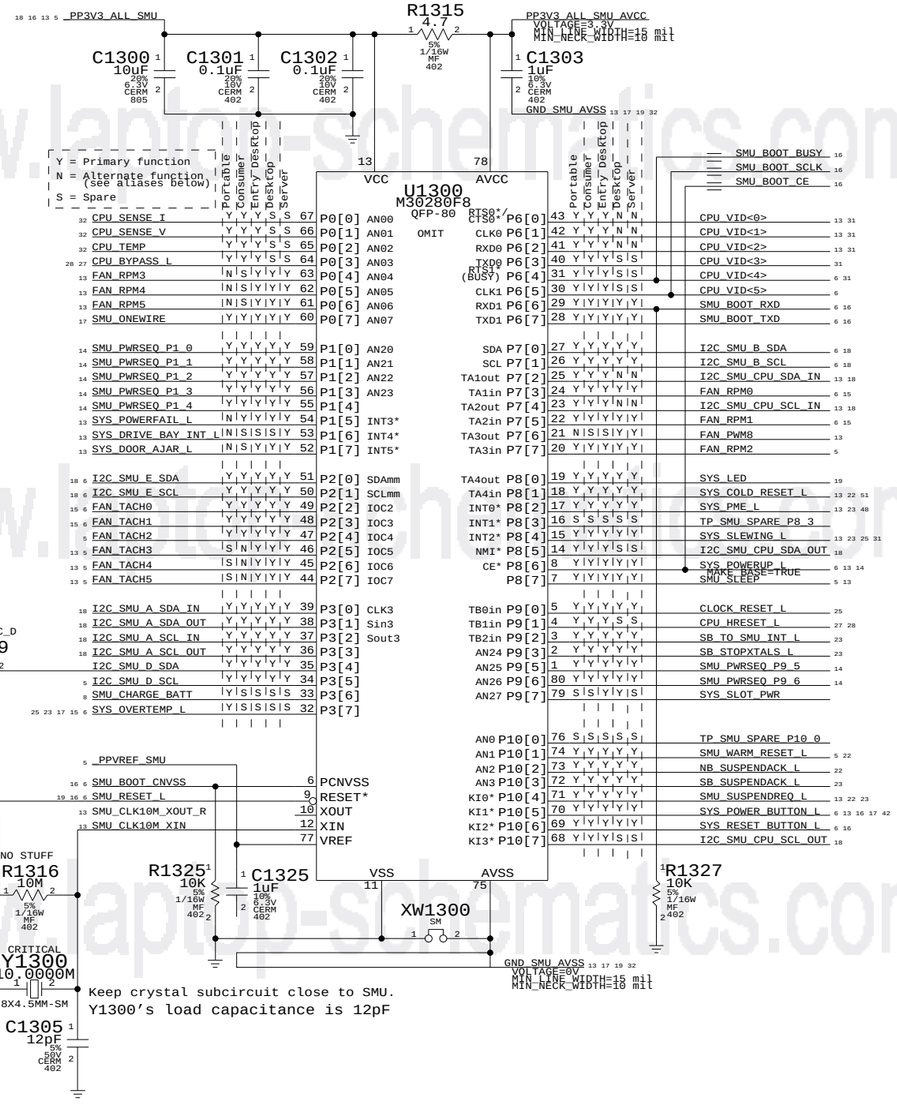
NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

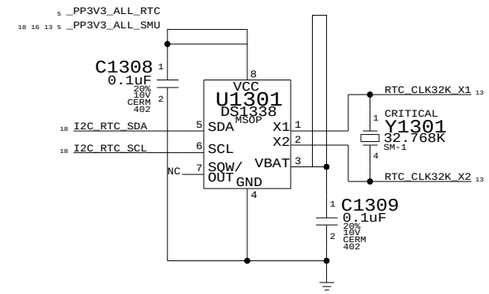
NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

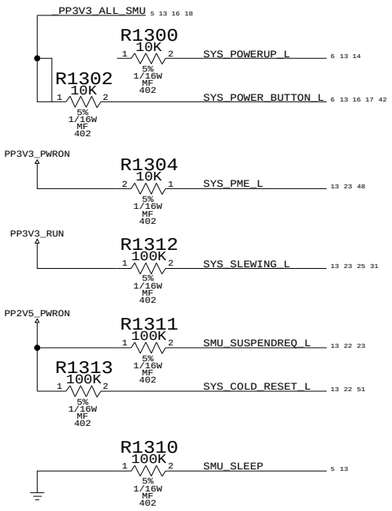
System Management Unit



Real Time Clock



SMU Pull-ups / pull-down



Alternate Functions

Portable

	Port		
FAN_RPM3	0.4	ALS0_OUT	6 17
FAN_RPM4	0.5	ALS1_OUT	19
FAN_RPM5	0.6	ALS_GAIN_BOOST	6 17 19
SYS_POWERFAIL_L	1.5	SMU_ACIN	7 8 12
SYS_DRIVE_BAY_INT_L	1.6	SMU_BATT_DET_L	7
SYS_DOOR_AJAR_L	1.7	SYS_LID_OPEN	17
FAN_PWM8	7.6	SYS_KBDLED	19

Consumer

	Port	
FAN_TACH3	2.5	SYS_LED_RED
FAN_TACH4	2.6	SYS_LED_GREEN
FAN_TACH5	2.7	SYS_LED_BLUE

Tower & Server

	Port	
CPU_VID<0>	6.0	FAN_TACH6
CPU_VID<1>	6.1	FAN_TACH7
CPU_VID<2>	6.2	FAN_TACH8
I2C_SMU_CPU_SDA_IN	7.2	FAN_PWM6
I2C_SMU_CPU_SCL_IN	7.4	FAN_PWM7

Master: Link

System Management Unit

APPLE COMPUTER INC.

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POWER-UP
SLEEP
WAKE
SHUT-DOWN

ACTIVE-LOW, OUTPUT, PUSH-PULL
SYS_POWERUP_L
100K pull-up to 3.3V_ALL on pg 13
R1400 0 5% 1/16W MF 402
SYS_POWERUP_L_R

PP3V3_ALL
R1401 68K 5% 1/16W MF 402
TPS5120 needs a pull-up stronger than 82.5K
SYS_POWERUP
Q1400 2N7002DW SOT-363
R1402 0 5% 1/16W MF 402 → 5V_STBY_L
R1403 0 5% 1/16W MF 402 → FWPWR_PWRON

ACTIVE-HIGH, OUTPUT, PUSH-PULL
SMU_PWRSEQ_P1_0 (ALIAS) SYS_PWRSEQ_1 MAKE_BASE=TRUE
R1410 0 5% 1/16W MF 402 → 3V3_STBY_L
R1411 0 5% 1/16W MF 402 → 2V5NBVCORE_STBY_L
R1412 100K 5% 1/16W MF 402

PP5V_PWRON
R1429 100K 5% 1/16W MF 402

ACTIVE-HIGH, OUTPUT, PUSH-PULL
SMU_PWRSEQ_P1_1 (ALIAS) SYS_PWRSEQ_2 MAKE_BASE=TRUE
Q1400 2N7002DW SOT-363
SYS_PWRSEQ_2_L
R1420 100K 5% 1/16W MF 402 → 5VRUN_EN_L
R1421 100K 5% 1/16W MF 402 → 5VRUNHD_EN_L
R1422 100K 5% 1/16W MF 402 → 3V3RUN_EN_L

ACTIVE-LOW, OUTPUT, PUSH-PULL
SMU_PWRSEQ_P1_2 (ALIAS) SYS_PWRSEQ_3_L MAKE_BASE=TRUE
R1430 0 5% 1/16W MF 402 → 2V5RUN_EN_L

PP5V_RUN
R1435 100K 5% 1/16W MF 402
SYS_PWRSEQ_3_LS5
Q1435 2N7002DW SOT-363
R1436 100K 5% 1/16W MF 402 → 1V5RUN_EN
R1437 100K 5% 1/16W MF 402 → 1V2RUN_EN

PP3V3_RUN
R1448 100K 5% 1/16W MF 402

ACTIVE-HIGH, OUTPUT/INPUT, OPEN-COLLECTOR
SMU_PWRSEQ_P1_3 (ALIAS) SYS_PWRSEQ_4 MAKE_BASE=TRUE
R1440 100K 5% 1/16W MF 402 → CPUVCORE_SHDN_L
R1441 100K 5% 1/16W MF 402 → 1V8RUN_SHDN_L
R1449 0 5% 1/16W MF 402

PP3V3_RUN
R1458 100K 5% 1/16W MF 402

5V3VPWRON_PGOOD (ALIAS)
2V5_NBVCORE_PGOOD (ALIAS)
PWRON_REGS_PGOOD MAKE_BASE=TRUE

ACTIVE-HIGH, OUTPUT/INPUT, OPEN-COLLECTOR
SMU_PWRSEQ_P1_4 (ALIAS) SYS_PWRSEQ_5 MAKE_BASE=TRUE
R1450 0 5% 1/16W MF 402 → GPUVCORE_SHDN_L
R1451 0 5% 1/16W MF 402 → CPU_AVDD_EN
R1459 0 5% 1/16W MF 402 ← 1V8RUN_PGOOD

ACTIVE-LOW, OUTPUT, PUSH-PULL
SMU_PWRSEQ_P9_5 (ALIAS) SYS_PWRSEQ_6_L MAKE_BASE=TRUE

PP5V_RUN
R1465 100K 5% 1/16W MF 402
R1469 0 5% 1/16W MF 402 ← GPUVCORE_PGOOD
SYS_PWRSEQ_6_LS5 MAKE_BASE=TRUE
Q1435 2N7002DW SOT-363
(ALIAS) VCORE_SWITCHING
R1466 100K 5% 1/16W MF 402 → GPUVDD15_EN
R1467 0 5% 1/16W MF 402 → GPUPVDD_EN

ANALOG INPUT, SENSE > 1.7V
SMU_PWRSEQ_P9_6 (ALIAS) SYS_PWRSEQ_7 MAKE_BASE=TRUE
XW1470 SM → PP1V8_GPU_PVDD
Used to see if last rail is up

Power Sequencing

APPLE COMPUTER INC.

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	THERM	MAX1989_D1	MAX1989_D1_P
	THERM	MAX1989_D1	MAX1989_D1_N
	THERM	MAX1989_D2	MAX1989_D2_P
	THERM	MAX1989_D2	MAX1989_D2_N
	THERM	MAX1989_D3	MAX1989_D3_P
	THERM	MAX1989_D3	MAX1989_D3_N
	THERM	MAX1989_D4	MAX1989_D4_P
	THERM	MAX1989_D4	MAX1989_D4_N
	THERM	THERM_1	THERM_1_P
	THERM	THERM_1	THERM_1_N
	THERM	THERM_2	THERM_2_P
	THERM	THERM_2	THERM_2_N
	THERM	THERM_3	THERM_3_P
	THERM	THERM_3	THERM_3_N
	THERM	THERM_1B	THERM_1B_P
	THERM	THERM_1B	THERM_1B_N
	THERM	THERM_2B	THERM_2B_P
	THERM	THERM_2B	THERM_2B_N
	THERM	THERM_3B	THERM_3B_P
	THERM	THERM_3B	THERM_3B_N

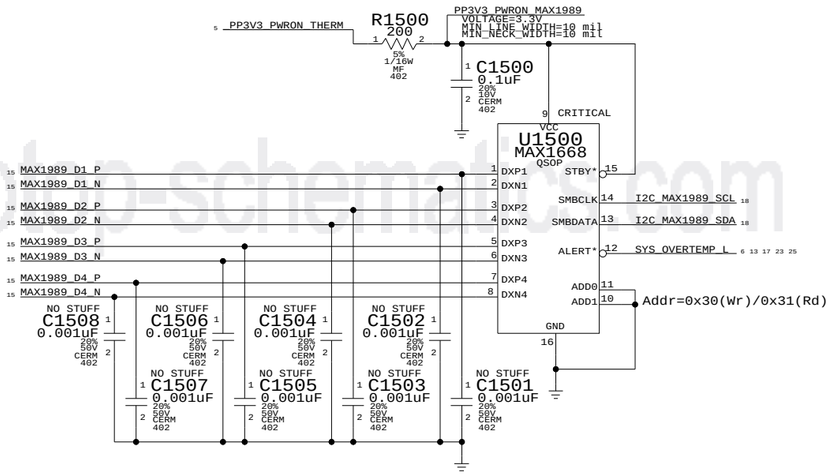
Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_THERM
- _PP5V_PWRON_FAN

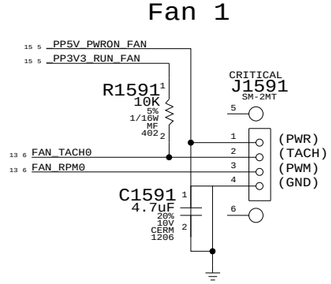
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- THERM_x / THERM_xB
  Selects between primary and backup thermal sensors for each of the available remote sensor locations.

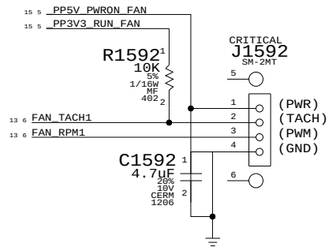
MAX1989 Thermal Sensor



Fan 1



Fan 2

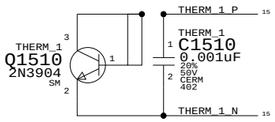


Remote Temperature Sensors

Place each cap close to associated transistor

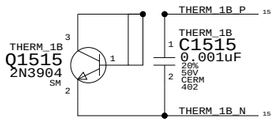
Remote 1

Place close to CPU_VCORE



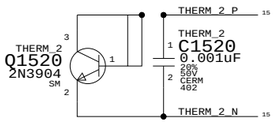
Remote 1 (Backup)

Place close to 5V/3.3V



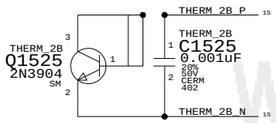
Remote 2

Place close to CPU



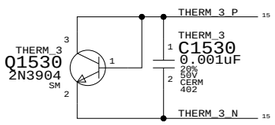
Remote 2 (Backup)

Place close to U3Lite



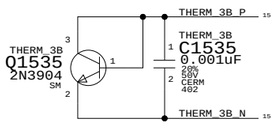
Remote 3

Place close to Shasta/GPU_Vcore



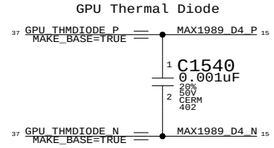
Remote 3 (Backup)

Place close to bottom RAM



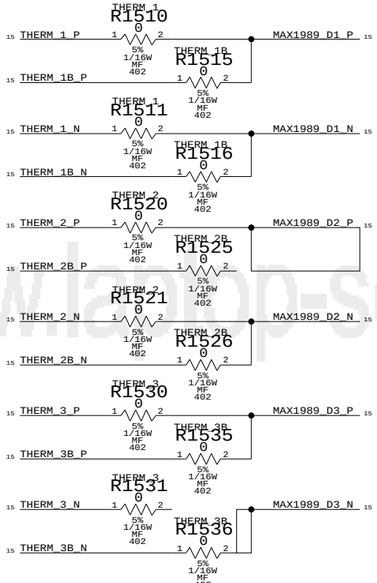
Remote 4

GPU Thermal Diode



Sensor Selection

First 3 MAX1668 inputs can connect to two different sensors. These resistors should be close to MAX1668, minimizing stubs.



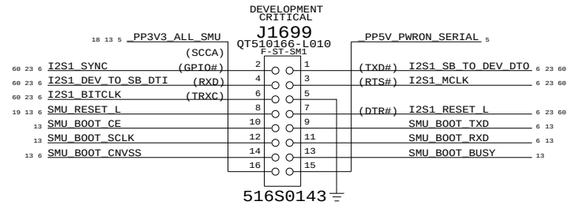
Thermal Sensor / Fans

APPLE COMPUTER INC.

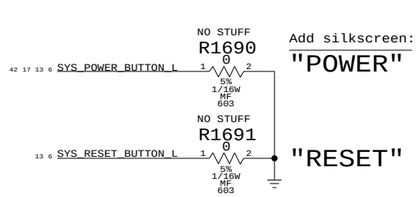
SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 15 OF 103	

SMU Download / Serial Debug Connector

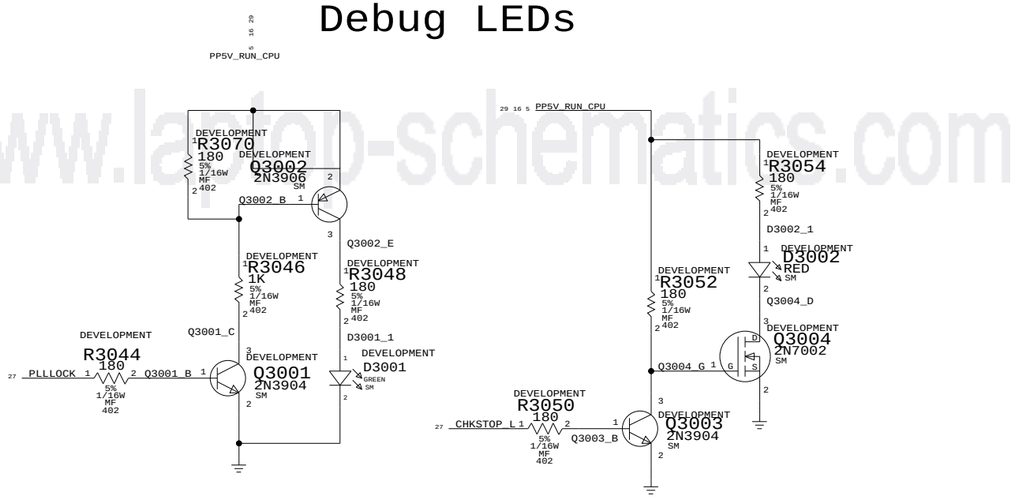
SCC same pins have pinout as modem connector to
allow serial debug flex to use either connector



Debug "Buttons"



Debug LEDs

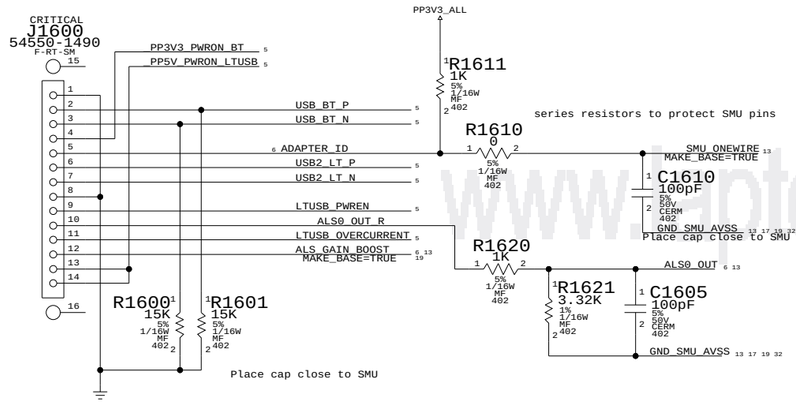


INTERNAL I/O CONNECTORS

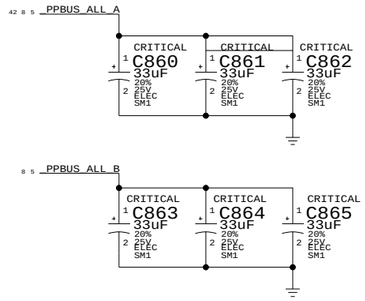
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 16 OF 103	

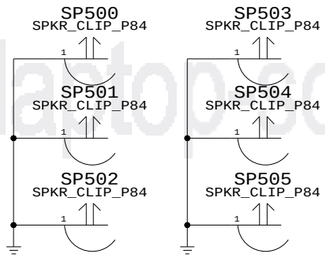
BlueTooth / Left USB Flex Connector



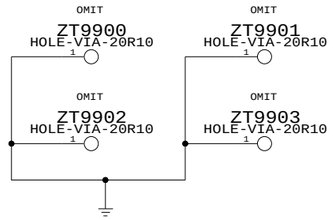
PPBUS Hold-Up Caps



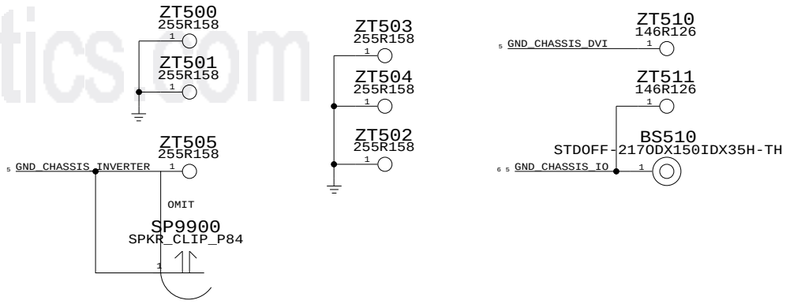
Speaker Clips



For EMI around ENET magnetic

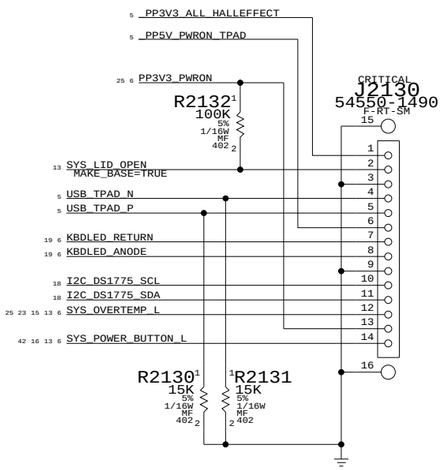


CPU Heat Sink Graphic Heat Sink Right I/O area



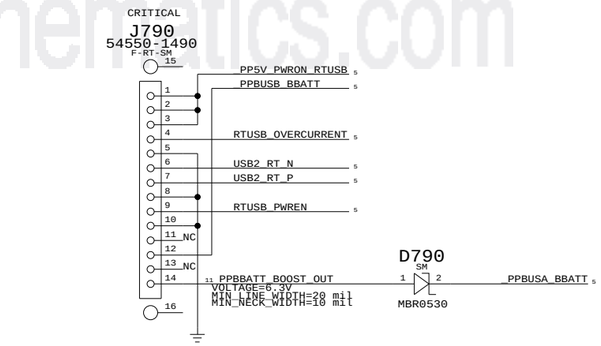
for EMI testing only

USB Trackpad Connector



overtemp may need pull-up resistor

Backup Battery / Right USB Flex Connector



_PPBUSB_BBATT is both an input and an output for backup battery circuit. _PPBUSA_BBATT is an output only.

Q51 Specific connectors

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 18 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
I2C_SMU_A_OUT	I2C	I2C_SMU_A_OUT	I2C_SMU_A_SCL_OUT 13 18
I2C_SMU_A_OUT	I2C	I2C_SMU_A_OUT	I2C_SMU_A_SDA_OUT 13 18
I2C_SMU_A_IN	I2C	I2C_SMU_A_IN	I2C_SMU_A_SCL_IN 13 18
I2C_SMU_A_IN	I2C	I2C_SMU_A_IN	I2C_SMU_A_SDA_IN 13 18
I2C_SMU_CPU_OUT	I2C	I2C_SMU_CPU_OUT	I2C_SMU_CPU_SCL_OUT 13 18
I2C_SMU_CPU_OUT	I2C	I2C_SMU_CPU_OUT	I2C_SMU_CPU_SDA_OUT 13 18
I2C_SMU_CPU_IN	I2C	I2C_SMU_CPU_IN	I2C_SMU_CPU_SCL_IN 13 18
I2C_SMU_CPU_IN	I2C	I2C_SMU_CPU_IN	I2C_SMU_CPU_SDA_IN 13 18
	I2C		I2C_CPU_A_SCL 18 27
	I2C		I2C_CPU_A_SDA 18 27
	I2C		SMU_CPU_JTAG_OR_I2C 18
	I2C		I2C_CPU_A_SDA_TO_SMU 18
I2C_SMU_B	I2C	I2C_SMU_B	I2C_SMU_B_SCL 6 13 18
I2C_SMU_B	I2C	I2C_SMU_B	I2C_SMU_B_SDA 6 13 18
I2C_NB_B	I2C	I2C_NB_B	I2C_NB_B_SCL 18 22
I2C_NB_B	I2C	I2C_NB_B	I2C_NB_B_SDA 18 22
I2C_NB_C	I2C	I2C_NB_C	I2C_NB_C_SCL 18 22
I2C_NB_C	I2C	I2C_NB_C	I2C_NB_C_SDA 18 22
I2C_SB	I2C	I2C_SB	I2C_SB_SCL 6 18 23
I2C_SB	I2C	I2C_SB	I2C_SB_SDA 6 18 23

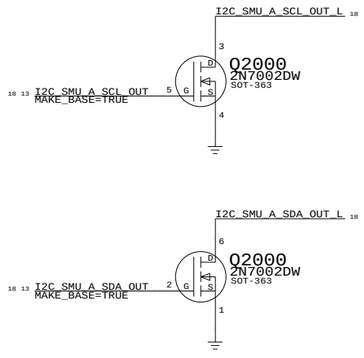
Page Notes

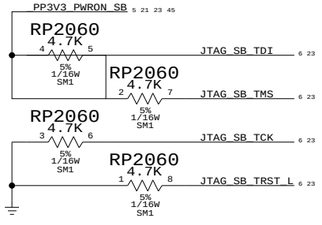
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

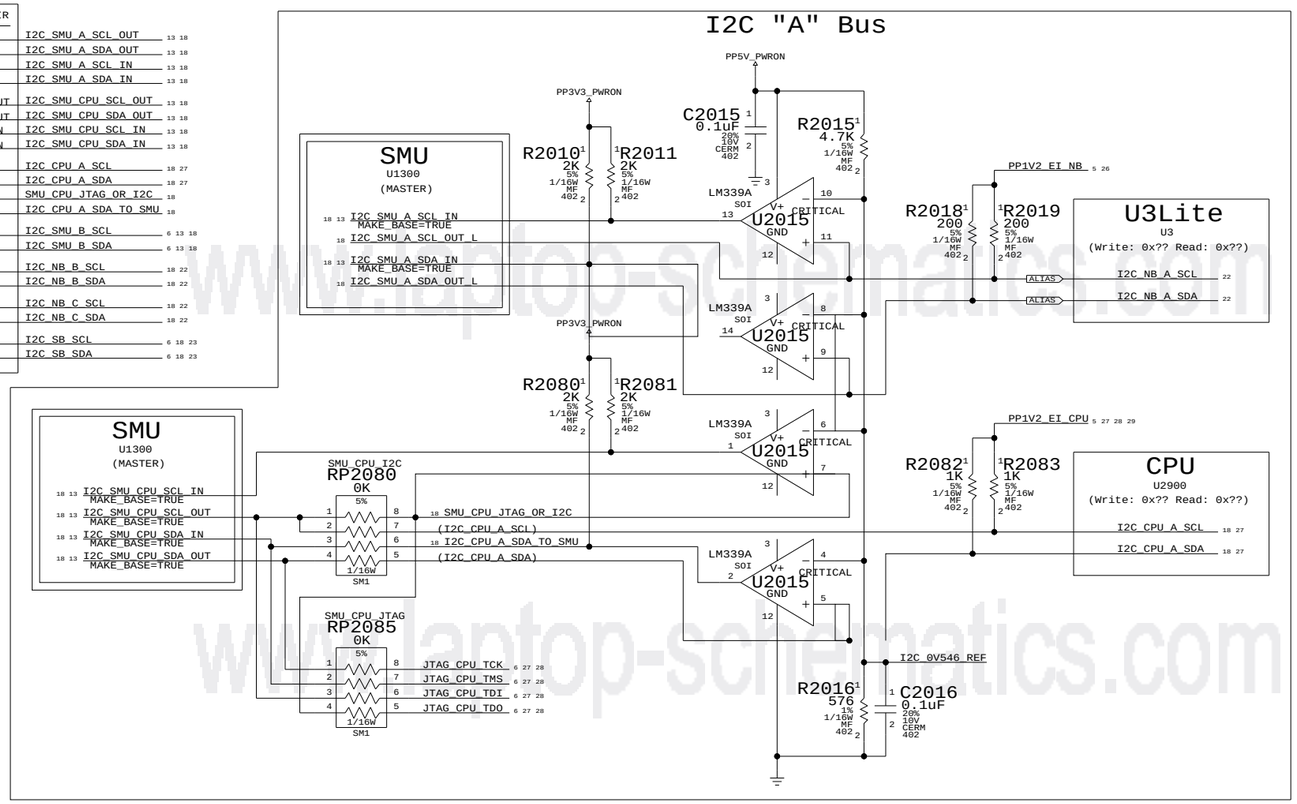
BOM options provided by this page:
(NONE)

U3 Lite I2C inversion

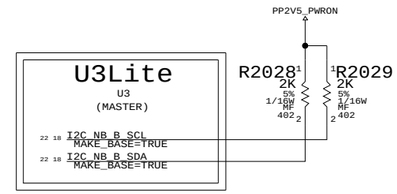




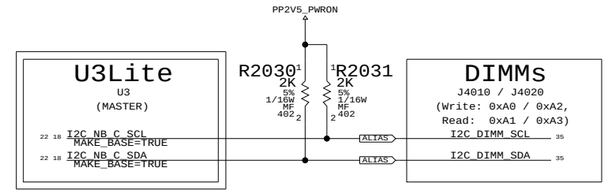
I2C "A" Bus



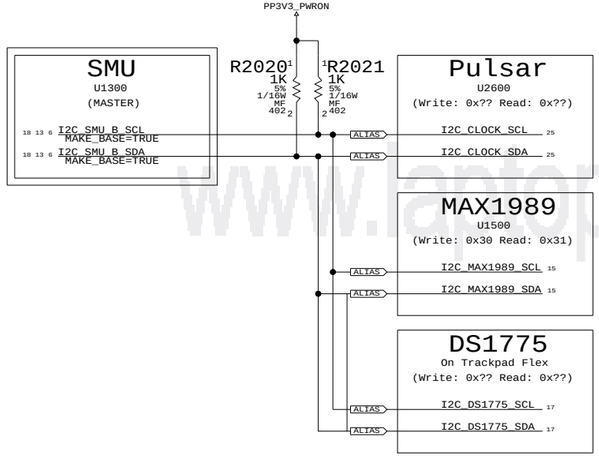
NorthBridge I2C "B" Bus



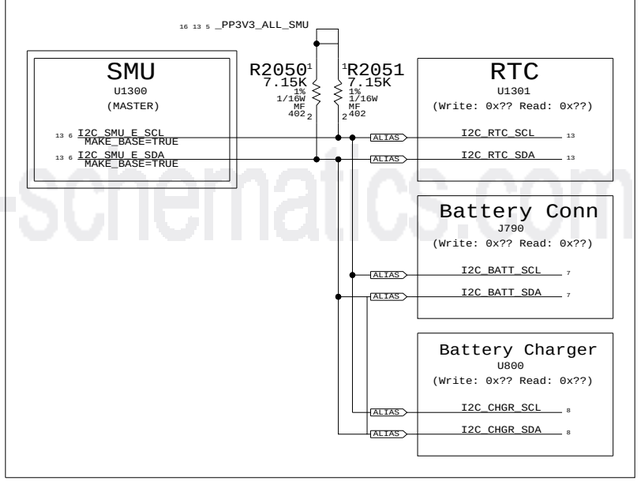
NorthBridge I2C "C" Bus



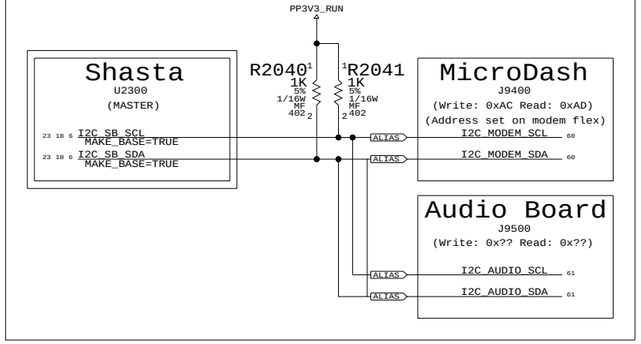
I2C "B" Bus



I2C "E" Bus



SouthBridge I2C Bus

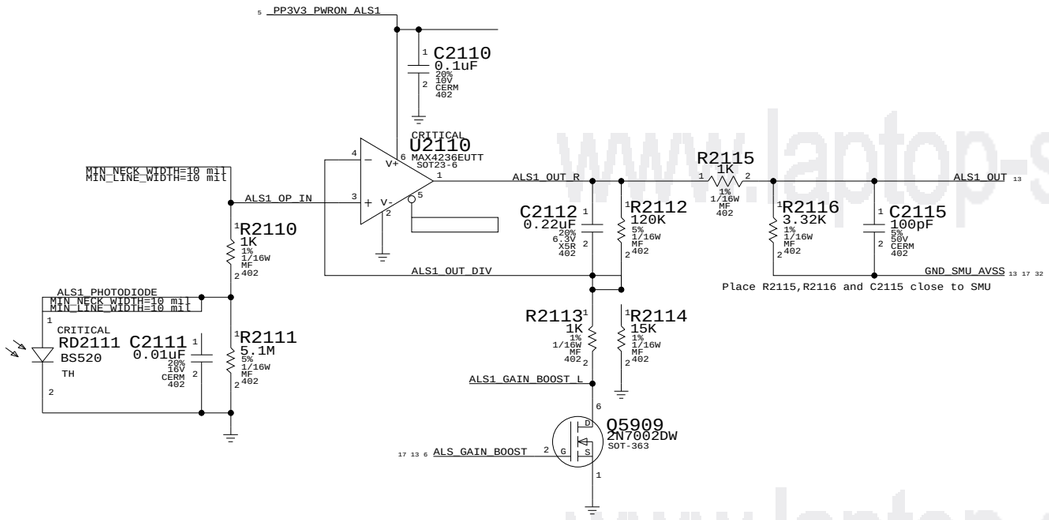


I2C CONNECTIONS

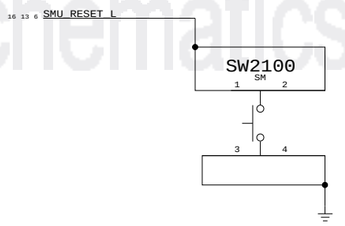
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 20 OF 103	

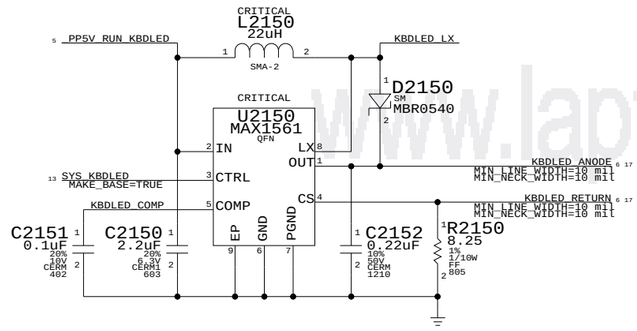
Ambient Light Sensor #1



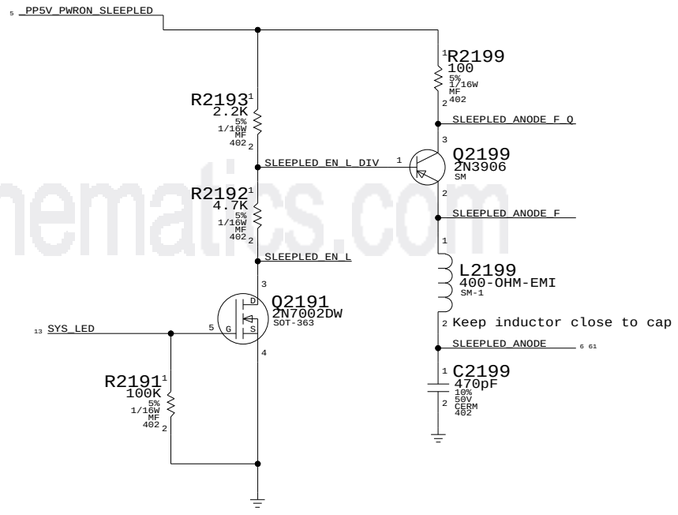
SMU / System Reset Button



Keyboard LED Driver



Sleep LED Circuit



SMU ALS/LEDs

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APPLE COMPUTER INC.

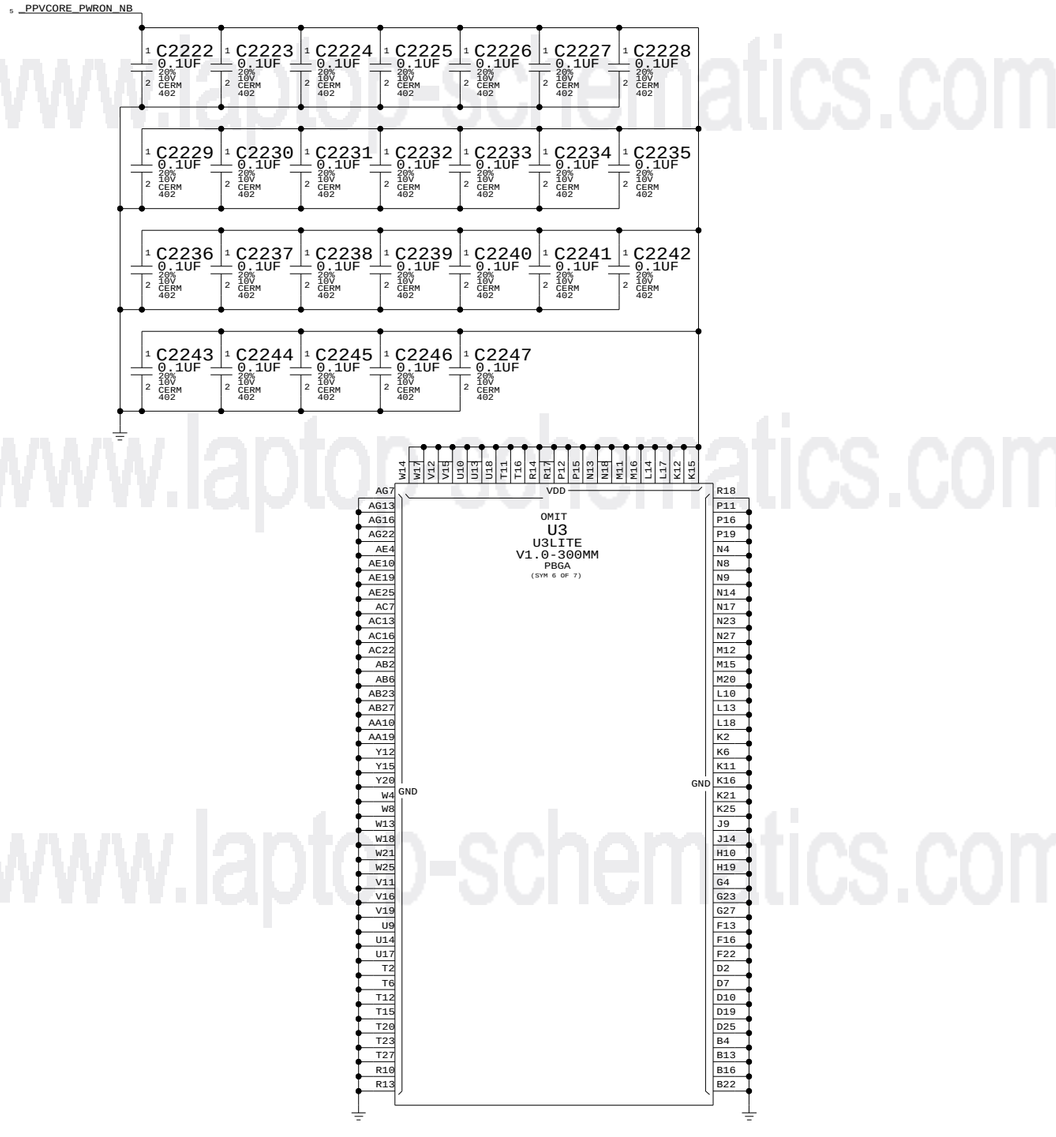
SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 21 OF 103	

Page Notes

Power aliases required by this page:
- _PPVCORE_PWRON_NB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Master: Link

U3Lite Core Power

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	22	103

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:04:04 2004

Page Notes

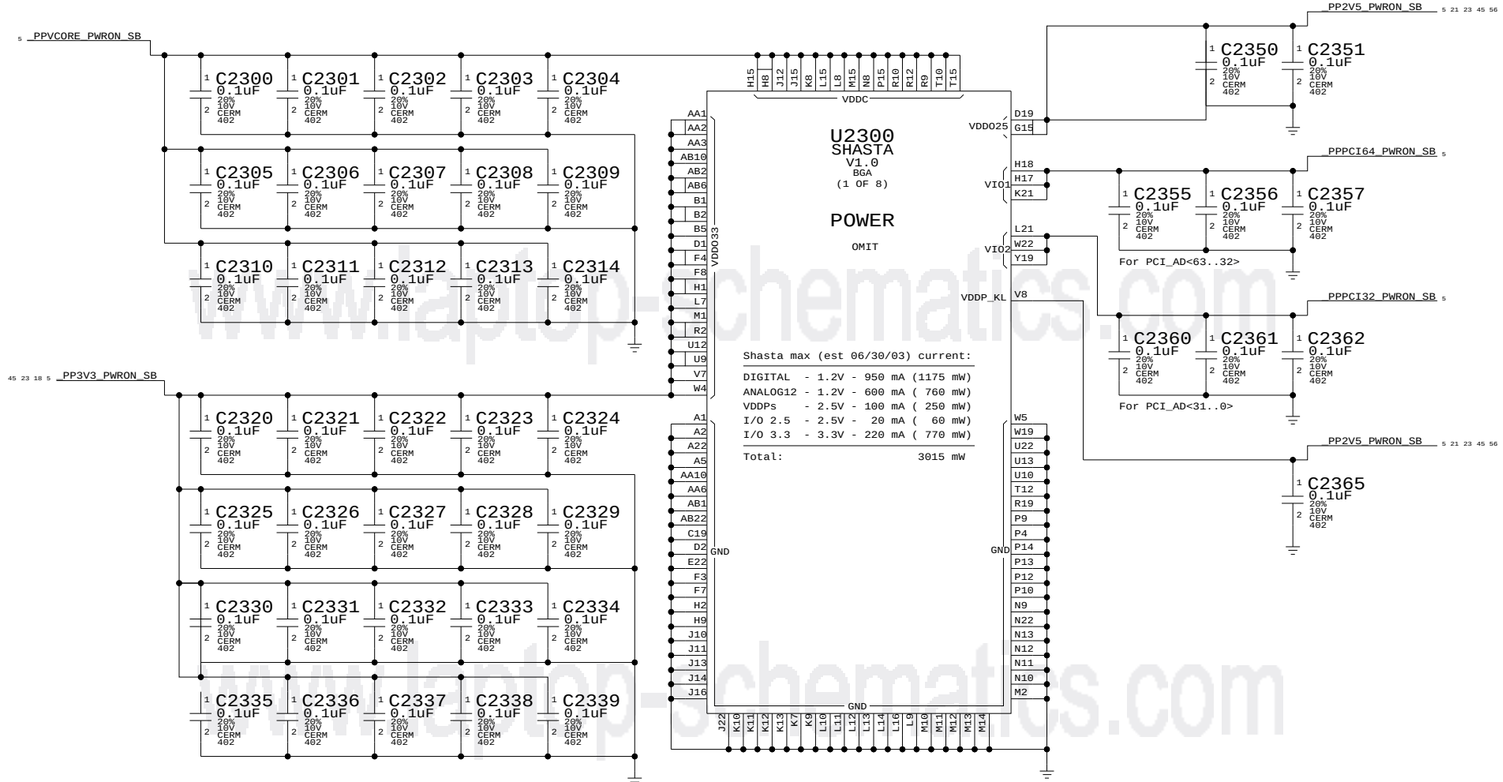
Power aliases required by this page:
- _PPPCI64_PWRON_SB (to 5V or 3.3V)
- _PPPCI32_PWRON_SB (to 5V or 3.3V)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PPVCORE_PWRON_SB (1.2V)

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect _PPPCI32_PWRON_SB to appropriate PCI bus voltage and _PPPCI64_PWRON_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.



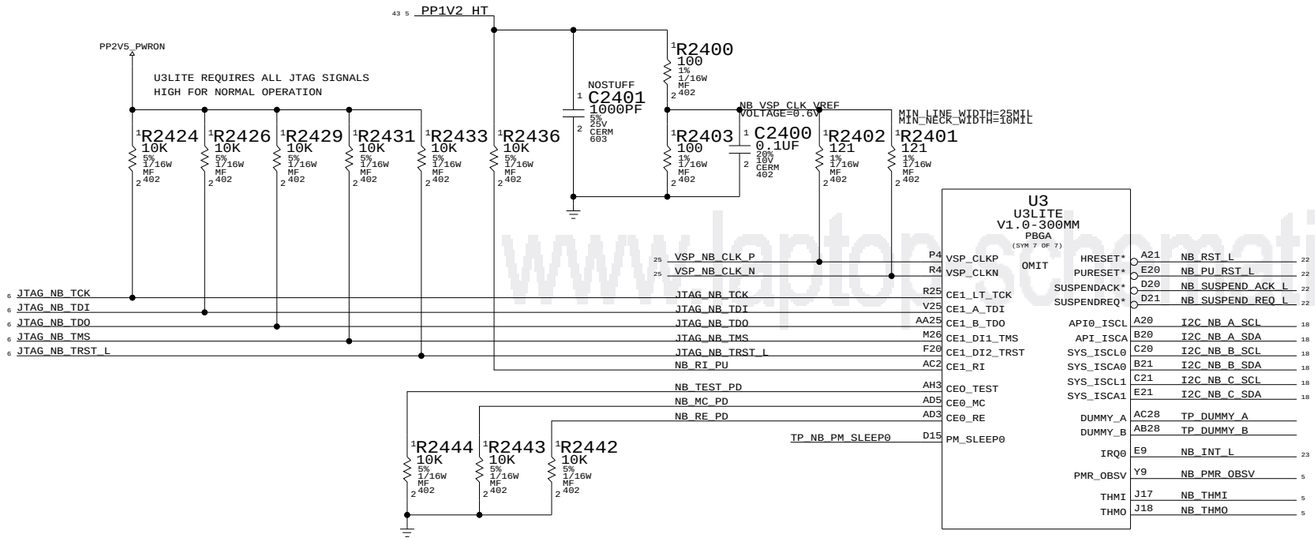
Master: Link

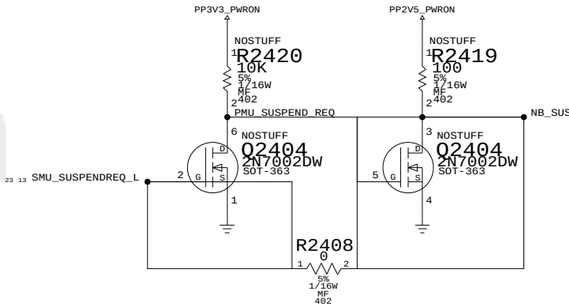
Shasta Core Power

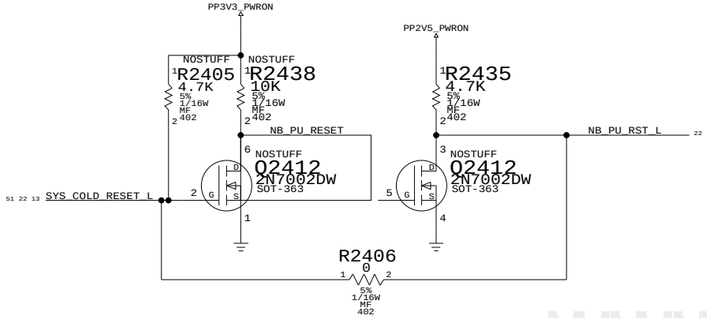
APPLE COMPUTER INC.

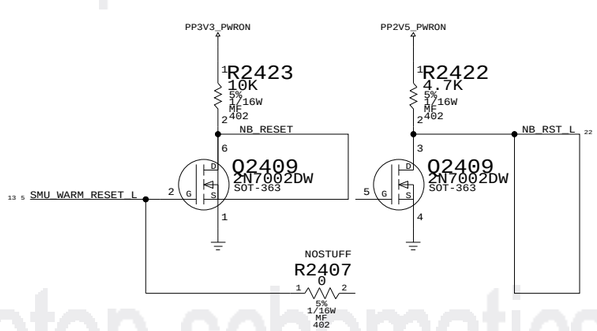
SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 23 OF 103	

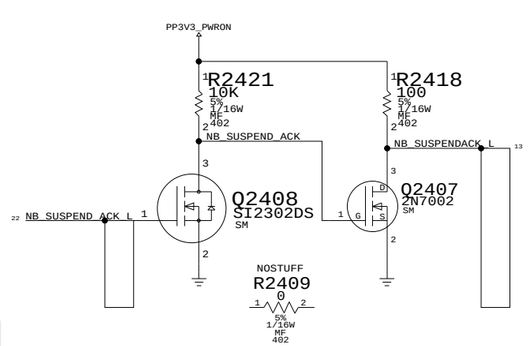
_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:04:08 2004











ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_RESET	10 MIL SPACING		SYS_COLD_RESET_L 13 22 51
SMU_RESET	10 MIL SPACING		SYS_WARM_RESET_L 5 23 45 48

MASTER: GILA

U3LITE MISC

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 24 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
I2S0_TO_SB			I2S0_DEV_TO_SB_DTI	23 61
I2S0_TO_DEV			I2S0_SB_TO_DEV_DTO	23 61
I2S0_TO_DEV	10_MIL_SPACING		I2S0_MCLK	23 61
I2S0_BIDIR			I2S0_BITCLK	23 61
I2S0_BIDIR			I2S0_SYNC	23 61
I2S1_TO_SB			I2S1_DEV_TO_SB_DTI	6 16 23 60
I2S1_TO_DEV			I2S1_SB_TO_DEV_DTO	6 16 23 60
I2S1_TO_DEV	10_MIL_SPACING		I2S1_MCLK	6 16 23 60
I2S1_BIDIR			I2S1_BITCLK	6 16 23 60
I2S1_BIDIR			I2S1_SYNC	6 16 23 60
I2S2_TO_SB			I2S2_DEV_TO_SB_DTI	23 61
I2S2_TO_DEV			I2S2_SB_TO_DEV_DTO	23
I2S2_TO_DEV	10_MIL_SPACING		I2S2_MCLK	23
I2S2_BIDIR			I2S2_BITCLK	23 61
I2S2_BIDIR			I2S2_SYNC	23 61
SB_CLK18M_XTAL	15_MIL_SPACING		SB_CLK18M_XTALI	23
	15_MIL_SPACING		SB_CLK18M_XTALO	23
	15_MIL_SPACING		SB_CLK18M_XTALO_R	23
SB_CLK25M_ATA	15_MIL_SPACING		SB_CLK25M_ATA	23 25

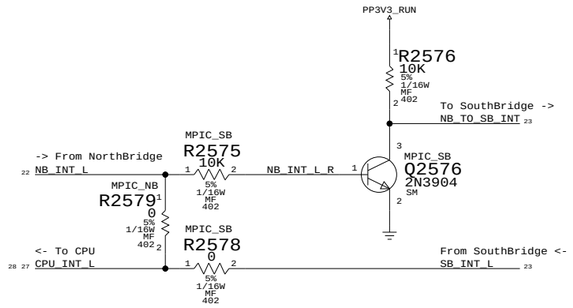
Page Notes

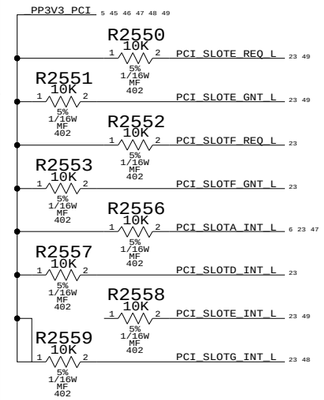
Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page:
(NONE)

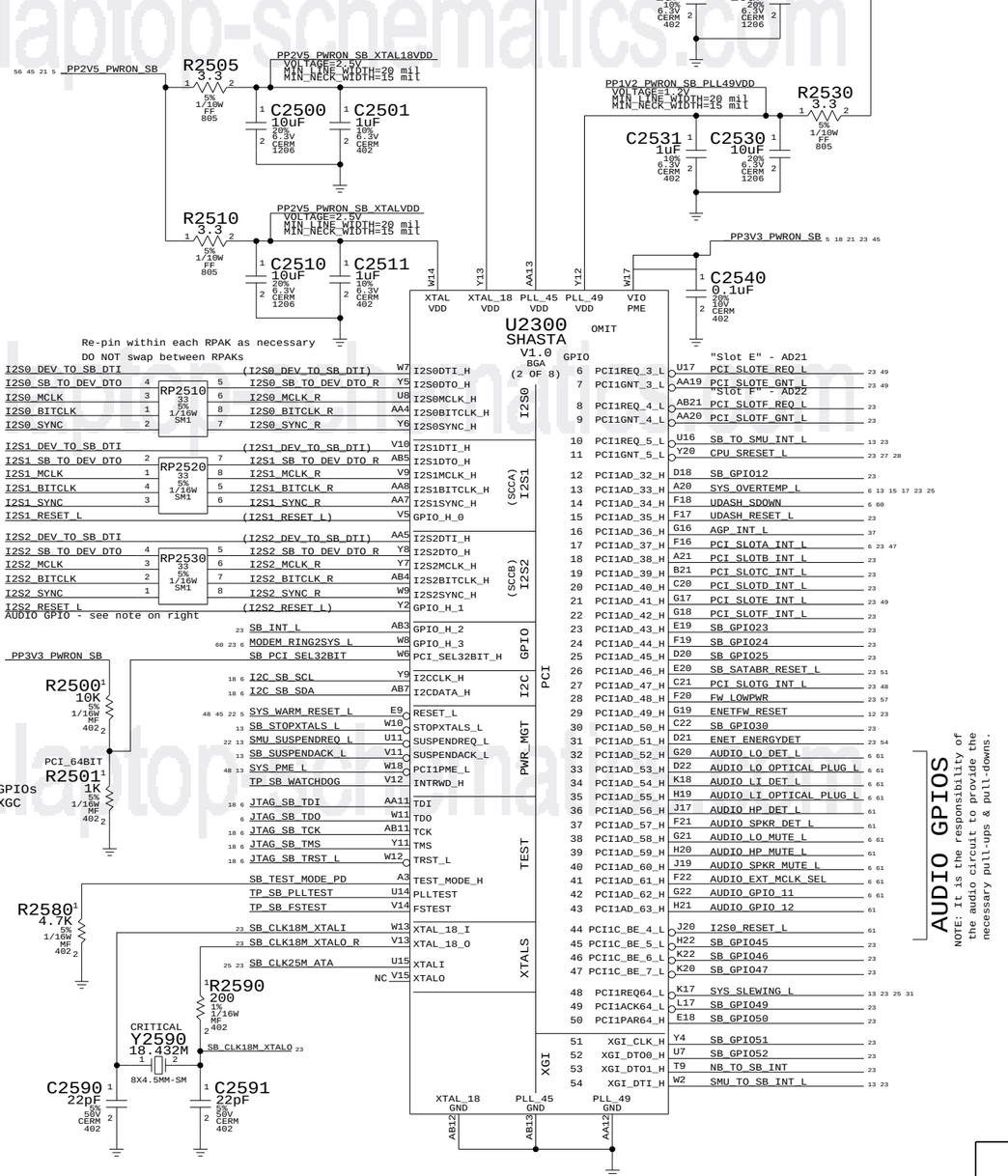
BOM options provided by this page:
- PCI_64BIT
  Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB
  Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

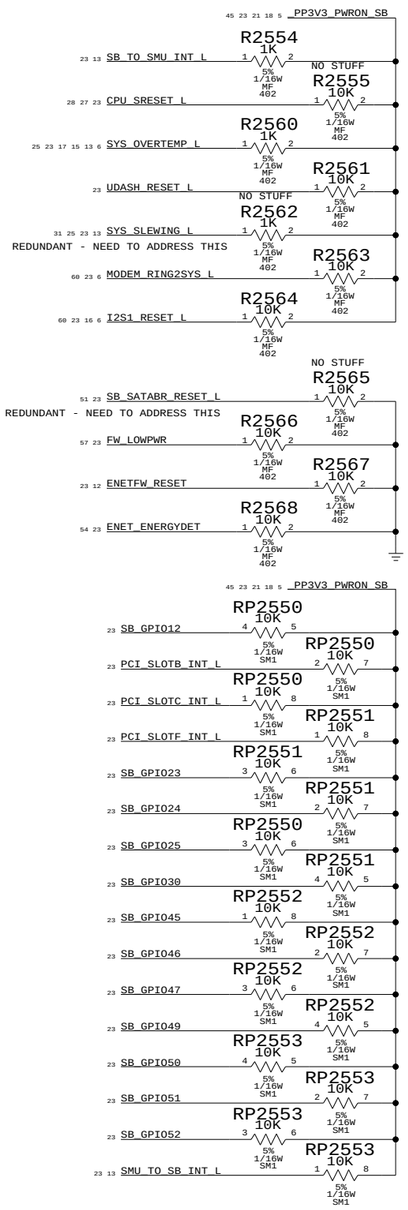
NorthBridge / SouthBridge MPIC Routing





DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:04:13 2004



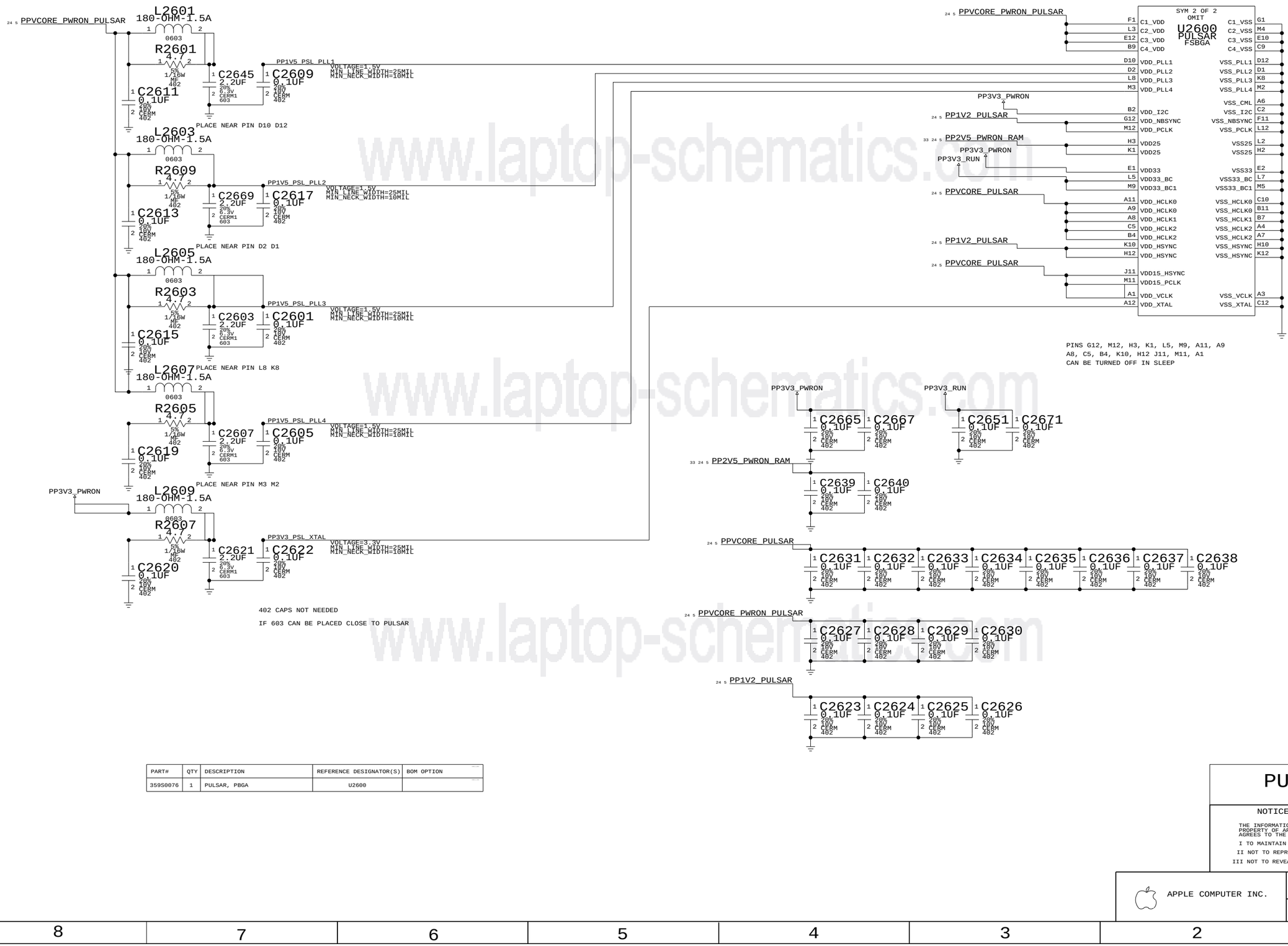


Master: Link

Shasta Serial / Misc

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 25 OF 103	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, PBGA	U2600	

MASTER: GILA

PULSAR POWER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 26 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
EI_CPU_CLK_P	EI_CPU_CLK	CLOCKS	EI_CPU_CLK
EI_CPU_CLK_N	EI_CPU_CLK	CLOCKS	EI_CPU_CLK
EI_CPU1_CLK_P	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK
EI_CPU1_CLK_N	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK
EI_NB_CLK_P	EI_NB_CLK	CLOCKS	EI_NB_CLK
EI_NB_CLK_N	EI_NB_CLK	CLOCKS	EI_NB_CLK
EI_CPU_SYNC	EI_SYNC	CLOCKS	
EI_NB_SYNC		CLOCKS	
EI_CPU1_SYNC	EI_CPU1_SYNC	CLOCKS	
VSP_NB_CLK_P	VSP_NB_CLK	CLOCKS	VSP_NB_CLK
VSP_NB_CLK_N	VSP_NB_CLK	CLOCKS	VSP_NB_CLK
AGP_CLK66M_NB	AGP_NB_CLK	CLOCKS	
AGP_CLK66M_GPU	AGP_GPU_CLK	CLOCKS	
HT_CLK66M_NB	HT_NB_CLK	CLOCKS	
HT_CLK66M_SB	HT_SB_CLK	CLOCKS	
PCI_CLK66M_SB_INT	CLOCKS_PCI	CLOCKS	
PCI_CLK33M_SB_EXT	CLOCKS_PCI	CLOCKS	
PLS_EXTCLK	PLS_XTAL	CLOCKS	

DIFFERENTIAL SIGNALS SHOULD HAVE 5 MIL SPACING TO EACH OTHER
ALL SPACING GROUPS SHOULD HAVE 15 MIL SPACING TO SIGNALS NOT IN THEIR GROUP

EI_NB_SYNC IS PART OF EI_CPU_SYNC TOPOLOGY

SYM 1 OF 2

OMIT
U2600
PULSAR
FSBGA

			NET SPACING TYPE
GPCLK33_0	L4	PCI_CLK_GP0_R	CLOCKS
GPCLK33_1	K4	PCI_CLK_GP1_R	CLOCKS
VCLKN	A2	VSP_NB_CLK_N_C	CLOCKS
VCLKP	B3	VSP_NB_CLK_P_C	CLOCKS
HCLKN_0	B10	EI_CPU_CLK_N_C	CLOCKS
HCLKN_1	C8	EI_CPU1_CLK_N_R	CLOCKS 5
HCLKN_2	C4	EI_NB_CLK_N_C	CLOCKS
HCLKP_0	A10	EI_CPU_CLK_P_C	CLOCKS
HCLKP_1	B8	EI_CPU1_CLK_P_R	CLOCKS 5
HCLKP_2	B5	EI_NB_CLK_P_C	CLOCKS
GPCLK25_0	J3	PLS_CLK_66M_0_R	CLOCKS
GPCLK25_1	J1	PLS_CLK_66M_1_R	CLOCKS
PCLK25_0	K2	HT_CLK66M_NB_R	CLOCKS
PCLK25_1	L1	RAM_CLK66M_NB_R	CLOCKS
PCLK33_0	K5	PCI_CLK66M_SB_INT_R	CLOCKS
PCLK33_1	L6	PCI_CLK_P1_R	CLOCKS
PCLK33_2	M7	AGP_CLK66M_GPU_R	CLOCKS
PCLK33_3	L9	PCI_CLK_P3_R	CLOCKS
PCLK33_4	M10	PCI_CLK_P4_R	CLOCKS
HTBEN_0	K11	CPU_HTBEN_R	CLOCKS
HTBEN_1	J12	CPU1_HTBEN_R	CLOCKS 5
NBSYNC	F12	EI_NB_SYNC_R	CLOCKS
HSYNC_0	J10	EI_CPU_SYNC_R	CLOCKS
HSYNC_1	H11	EI_CPU1_SYNC_R	CLOCKS 5
REFCLK_0	G2	SB_CLK25M_ATA_R	CLOCKS
REFCLK_1	H1	SATA_CLK25M_R	CLOCKS
SLEWING*	K9	SLEWING_L_R	CLOCKS
ERROR*	M8	CLOCK_ERROR_L	
PCLK12	L11	HT_CLK66M_SB_R	CLOCKS
PCLK15	L10	AGP_CLK66M_NB_R	CLOCKS

18 I2C_CLOCK_SCL	C1	SCLK	
18 I2C_CLOCK_SDA	B1	SDATA	
13 CLOCK_RESET_L	D3	RESET*	
PLS_X_IN	C11	XIN	
PLS_X_OUT	B12	XOUT	
PLS_X_ADDRSEL	E3	ADDRSEL	
TP_PLS_TEST1	K3	TEST1	
TP_PLS_TEST2	E11	TEST2	
TP_PLS_TEST3	D11	TEST3	
PLS_SCAN_MODE	M1	SCAN_MODE	
PLS_REF15	G11	REF15	
PLS_REF25	J2	REF25	
PLS_REF33	M6	REF33	
TP_PLS_REF_CML	A5	REF_CML	
PLS_PRES_CML	B6	PRES_CML	
PLS_FORCE_P0_L_R	F2	FORCESPO*	
	C3	PD	

R2704 0 5% 402 — CLOCK_RESET_L → PLS_RESET_L

0=IIC ADDR D2/D3
1=IIC ADDR D4/D5

R2738 1K 5% 402 NOSTUFF — PLS_X_ADDRSEL

R2706 249 1% 402 — PLS_SCAN_MODE

R2744 681 1% 402 — PLS_REF15
R2740 1K 1% 402 — PLS_REF25
R2746 1K 1% 402 — PLS_REF33

R2742 806 1% 402 — PLS_PRES_CML

17 6 PP3V3_PWRON → R2722 1K 5% 1/16W MF 402

R2748 0 5% 1/16W MF 402 NOSTUFF — 23 17 15 13 6 SYS_OVERTEMP_L → PLS_FORCE_P0_L_R

11 10 5 SYS_SLEEP (SLEEP) → R2750 0 5% 402 — PLS_POWER_DOWN

R2724 1K 5% 402 NOSTUFF

J2700 U.FL-R_SMT F-ST-SM

25 PLS_EXTCLK → R2752 0 5% 1/16W MF 402 NO STUFF

R2762 24 5% 1/16W MF 402 NOSTUFF — PLS_INTERM

R2764 24 5% 1/16W MF 402 NOSTUFF

R2754 0 5% 1/16W MF 402

R2758 330K 5% 1/16W MF 402 NO STUFF

R2756 0 5% 1/16W MF 402

CRITICAL
Y2701 25.0000M 8X4.5MM-SM — PLS_X_IN_B, PLS_X_OUT_B

C2707 33PF 5% 50V CERM 402

C2705 33PF 5% 50V CERM 402

R2701 0 5% 3.3V 33MHZ — PCI_CLK_GP0 5
R2761 0 5% 402 3.3V 33MHZ — PCI_CLK_GP1 5

C2708 0.001UF 50V 10% 2CERM 402
C2710 0.001UF 50V 10% 2CERM 402
C2713 0.001UF 50V 10% 2CERM 402
C2715 0.001UF 50V 10% 2CERM 402

VSP_NB_CLK_P 22 25
VSP_NB_CLK_N 22 25

EI_CPU_CLK_P 25 27
EI_CPU_CLK_N 25 27

C2700 0.001UF 50V 10% 2CERM 402
C2702 0.001UF 50V 10% 2CERM 402

EI_NB_CLK_P 25 26
EI_NB_CLK_N 25 26

R2775 0 5% 402	2.5V	66MHZ	TP_PLS_CLK_66M_0	
R2776 0 5% 402	2.5V	66MHZ	TP_PLS_CLK_66M_1	
R2703 20 5% 402	2.5V	66MHZ	HT_CLK66M_NB	25 43
R2709 20 5% 402	2.5V	66MHZ	RAM_CLK66M_NB	33
R2705 0 5% 402	3.3V	66MHZ	PCI_CLK66M_SB_INT	25 45
R2711 0 5% 402	3.3V	33MHZ	PCI_CLK_P1	5
R2707 0 5% 402	3.3V	66MHZ	AGP_CLK66M_GPU	25 37
R2702 0 5% 402	3.3V	33MHZ	PCI_CLK_P3	5
R2779 0 5% 402			PCI_CLK_P4	5
R2715 0 5% 402	1.2V	33MHZ	CPU_HTBEN	27 28
R2768 0 5% 402	1.2V		EI_NB_SYNC	25 26
R2772 0 5% 402	1.2V		EI_CPU_SYNC	25 27
R2770 20 5% 402	2.5V	25MHZ	SB_CLK25M_ATA	23
R2700 22 5% 402	2.5V	25MHZ	TP_SATA_CLK25M	
R2720 0 5% 402 — SYS_SLEWING_L	13 23 31			
R2717 0 5% 402	1.2V	66MHZ	HT_CLK66M_SB	25 44
R2719 0 5% 402	1.5V	66MHZ	AGP_CLK66M_NB	25 36

MASTER: GILA

PULSAR CLOCKS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 27 OF 103	

43 36 33 5 PP1V5_PWRON_NB_AVDD

R2890 2.2 5% 1/16W MF 603

PP1V5_PWRON_EI_NB_AVDD VOLTAGE=1.5V

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

C2818 1UF 10% 6.3V CERM 402

C2819 0.1UF 20% 10V CERM 402

PP1V2_EI_NB 5 18 26

F21 K4 K8 J3 H13 H16 G2 F7 F10 D4 D13 D16 B7 B10 B19

API APCLK_AVDD

VDD_API

U3 U3LITE V1.0-300MM PBGA (SYM 1 OF 7)

OMIT

APPLE PI INTERFACE

62 27 26 EI_NB_TO_CPU_CLK_P	F15	API0_BCLKIP	API0_BCLKOP	D6	EI_CPU_TO_NB_CLK_P 26 27 62
62 27 26 EI_NB_TO_CPU_CLK_N	E15	API0_BCLKIN	API0_BCLKON	E6	EI_CPU_TO_NB_CLK_N 26 27 62
62 27 26 EI_NB_TO_CPU_AD<0>	F11	API0_ADI0	API0_AD0	J2	EI_CPU_TO_NB_AD<0> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<1>	F12	API0_ADI1	API0_AD1	H1	EI_CPU_TO_NB_AD<1> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<2>	G11	API0_ADI2	API0_AD2	J1	EI_CPU_TO_NB_AD<2> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<3>	H11	API0_ADI3	API0_AD3	K1	EI_CPU_TO_NB_AD<3> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<4>	G12	API0_ADI4	API0_AD4	E1	EI_CPU_TO_NB_AD<4> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<5>	H12	API0_ADI5	API0_AD5	F2	EI_CPU_TO_NB_AD<5> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<6>	H14	API0_ADI6	API0_AD6	J4	EI_CPU_TO_NB_AD<6> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<7>	G14	API0_ADI7	API0_AD7	H4	EI_CPU_TO_NB_AD<7> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<8>	D9	API0_ADI8	API0_AD8	G1	EI_CPU_TO_NB_AD<8> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<9>	C9	API0_ADI9	API0_AD9	H2	EI_CPU_TO_NB_AD<9> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<10>	D11	API0_ADI10	API0_AD10	F1	EI_CPU_TO_NB_AD<10> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<11>	E11	API0_ADI11	API0_AD11	H5	EI_CPU_TO_NB_AD<11> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<12>	A10	API0_ADI12	API0_AD12	H3	EI_CPU_TO_NB_AD<12> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<13>	A9	API0_ADI13	API0_AD13	J3	EI_CPU_TO_NB_AD<13> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<14>	A8	API0_ADI14	API0_AD14	J5	EI_CPU_TO_NB_AD<14> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<15>	B9	API0_ADI15	API0_AD15	J6	EI_CPU_TO_NB_AD<15> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<16>	C11	API0_ADI16	API0_AD16	E3	EI_CPU_TO_NB_AD<16> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<17>	B11	API0_ADI17	API0_AD17	F4	EI_CPU_TO_NB_AD<17> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<18>	A11	API0_ADI18	API0_AD18	E2	EI_CPU_TO_NB_AD<18> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<19>	A12	API0_ADI19	API0_AD19	F5	EI_CPU_TO_NB_AD<19> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<20>	B12	API0_ADI20	API0_AD20	H6	EI_CPU_TO_NB_AD<20> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<21>	C12	API0_ADI21	API0_AD21	J7	EI_CPU_TO_NB_AD<21> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<22>	D12	API0_ADI22	API0_AD22	F3	EI_CPU_TO_NB_AD<22> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<23>	E12	API0_ADI23	API0_AD23	J8	EI_CPU_TO_NB_AD<23> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<24>	A13	API0_ADI24	API0_AD24	F6	EI_CPU_TO_NB_AD<24> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<25>	A14	API0_ADI25	API0_AD25	E5	EI_CPU_TO_NB_AD<25> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<26>	B14	API0_ADI26	API0_AD26	D5	EI_CPU_TO_NB_AD<26> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<27>	C14	API0_ADI27	API0_AD27	E4	EI_CPU_TO_NB_AD<27> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<28>	A16	API0_ADI28	API0_AD28	D8	EI_CPU_TO_NB_AD<28> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<29>	A15	API0_ADI29	API0_AD29	A5	EI_CPU_TO_NB_AD<29> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<30>	B15	API0_ADI30	API0_AD30	C2	EI_CPU_TO_NB_AD<30> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<31>	C15	API0_ADI31	API0_AD31	C3	EI_CPU_TO_NB_AD<31> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<32>	H15	API0_ADI32	API0_AD32	C5	EI_CPU_TO_NB_AD<32> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<33>	G15	API0_ADI33	API0_AD33	C6	EI_CPU_TO_NB_AD<33> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<34>	F17	API0_ADI34	API0_AD34	B2	EI_CPU_TO_NB_AD<34> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<35>	G17	API0_ADI35	API0_AD35	D1	EI_CPU_TO_NB_AD<35> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<36>	G18	API0_ADI36	API0_AD36	B1	EI_CPU_TO_NB_AD<36> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<37>	H18	API0_ADI37	API0_AD37	C1	EI_CPU_TO_NB_AD<37> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<38>	F18	API0_ADI38	API0_AD38	A6	EI_CPU_TO_NB_AD<38> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<39>	E18	API0_ADI39	API0_AD39	C8	EI_CPU_TO_NB_AD<39> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<40>	A17	API0_ADI40	API0_AD40	A2	EI_CPU_TO_NB_AD<40> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<41>	A18	API0_ADI41	API0_AD41	B3	EI_CPU_TO_NB_AD<41> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<42>	B17	API0_ADI42	API0_AD42	A7	EI_CPU_TO_NB_AD<42> 26 27 62
62 27 26 EI_NB_TO_CPU_AD<43>	C17	API0_ADI43	API0_AD43	B8	EI_CPU_TO_NB_AD<43> 26 27 62
62 27 26 EI_NB_TO_CPU_SR_P<0>	D17	API0_SRIP0	API0_SROP0	A3	EI_CPU_TO_NB_SR_P<0> 26 27 62
62 27 26 EI_NB_TO_CPU_SR_N<0>	A19	API0_SRIN0	API0_SRON0	A4	EI_CPU_TO_NB_SR_N<0> 26 27 62
62 27 26 EI_NB_TO_CPU_SR_P<1>	E17	API0_SRIP1	API0_SROP1	B5	EI_CPU_TO_NB_SR_P<1> 26 27 62
62 27 26 EI_NB_TO_CPU_SR_N<1>	B18	API0_SRIN1	API0_SRON1	B6	EI_CPU_TO_NB_SR_N<1> 26 27 62
27 EI_QACK_L	D14	API_QACK0	API_QREQ0	E14	EI_QREQ_L 27 28
	E8	API0_APSYNC	API_APCLKP	D18	EI_NB_CLK_P
	H17	API0_SE	API_APCLKN	C18	EI_NB_CLK_N
			API_CSTP	F14	CPU_CHKSTOP_L 27

PLACE R2805 AND R2806 NEAR U3LITE

R2805 0 5% 1/16W MF 402

25 EI_NB_SYNC — NB_APSYNC

NOSTUFF R2806 0 5% 1/16W MF 402

27 EI_SYNC_FROM_NB

28 27 EI_SE

API_APCLK_AVSS

C28

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
62 27 26 EI_CPU_TO_NB_CLK_P	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	P42
62 27 26 EI_CPU_TO_NB_CLK_N	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	P43
62 27 26 EI_NB_TO_CPU_CLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	P44
62 27 26 EI_NB_TO_CPU_CLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	P45
62 27 26 EI_CPU_TO_NB_AD<0..43>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_AD		P46
62 27 26 EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_AD		P47
62 27 26 EI_CPU_TO_NB_SR_P<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0	P48
62 27 26 EI_CPU_TO_NB_SR_N<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0	P49
62 27 26 EI_CPU_TO_NB_SR_P<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1	P50
62 27 26 EI_CPU_TO_NB_SR_N<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1	P51
62 27 26 EI_NB_TO_CPU_SR_P<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR0	P52
62 27 26 EI_NB_TO_CPU_SR_N<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR0	P53
62 27 26 EI_NB_TO_CPU_SR_P<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR1	P54
62 27 26 EI_NB_TO_CPU_SR_N<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR1	P55

PP1V2_EI_NB 5 18 26

NOSTUFF R2802 100 1% 1/16W MF 402

NOSTUFF C2821 0.001UF 10% 50V CERM 402

NOSTUFF R2801 100 1% 1/16W MF 402

EI_APCLK_VREF VOLTAGE=0.6V

NOSTUFF C2820 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=28MIL MIN_NECK_WIDTH=10MIL

NOSTUFF R2803 121 1% 1/16W MF 402

NOSTUFF R2804 121 1% 1/16W MF 402

EI_NB_CLK_P 25

EI_NB_CLK_N 25

C2820, R2803, R2804 CHANGED TO 603 FOR FMAX

ZT2847 ZT2857 ZT2867 ZT2807 ZT2817 ZT2827 ZT2837
ZT2848 ZT2858 ZT2868 ZT2808 ZT2818 ZT2828 ZT2838
ZT2849 ZT2859 ZT2869 ZT2809 ZT2819 ZT2829 ZT2839
ZT2850 ZT2860 ZT2800 ZT2810 ZT2820 ZT2830 ZT2840
ZT2851 ZT2861 ZT2801 ZT2811 ZT2821 ZT2831 ZT2841
ZT2852 ZT2862 ZT2802 ZT2812 ZT2822 ZT2832 ZT2842
ZT2853 ZT2863 ZT2803 ZT2813 ZT2823 ZT2833 ZT2843
ZT2854 ZT2864 ZT2804 ZT2814 ZT2824 ZT2834 ZT2844
ZT2855 ZT2865 ZT2805 ZT2815 ZT2825 ZT2835 ZT2845
ZT2806 ZT2816 ZT2826 ZT2836
ZT2846 ZT2856 ZT2866

All: OMIT HOLE-VIA-20R10

PP1V2_EI_NB 5 18 26

C2800 C2801 C2802 C2803 C2804 C2805 C2806 C2807 C2808 C2809 C2810 C2811 C2812 C2813 C2814 C2815 C2816 C2817
0.1UF 20% 10V CERM 402

MASTER: GILA

U3LITE APPLE PI

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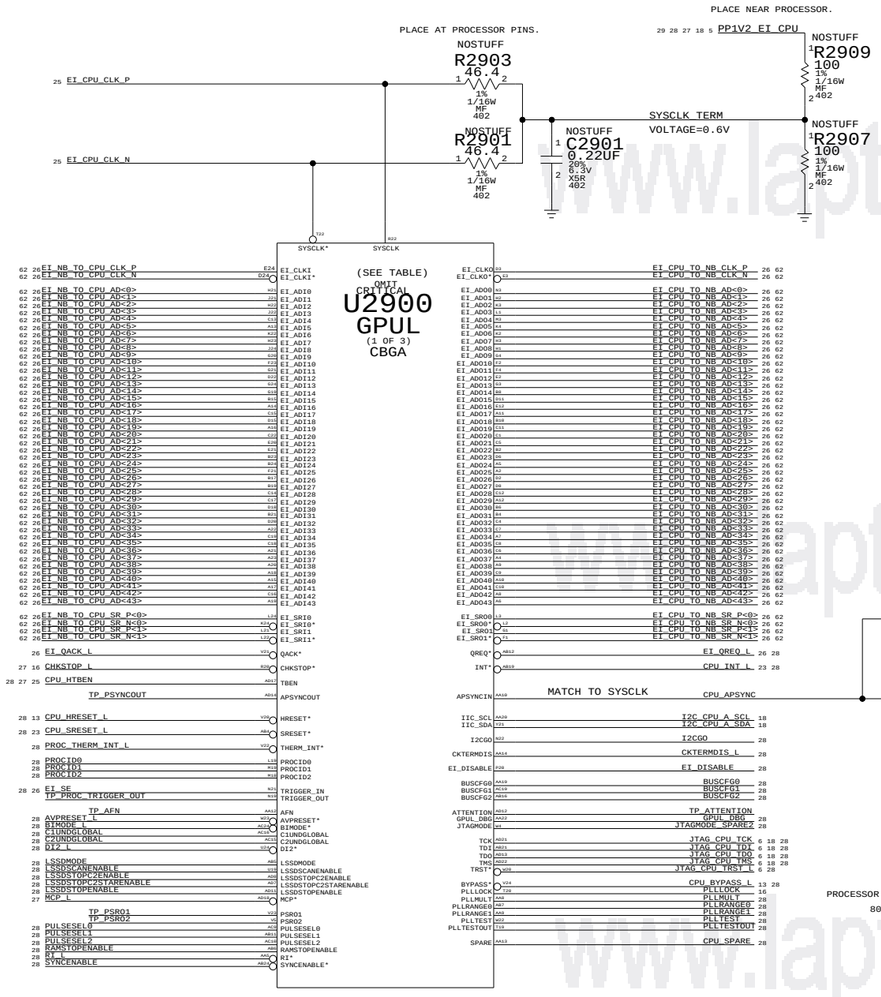
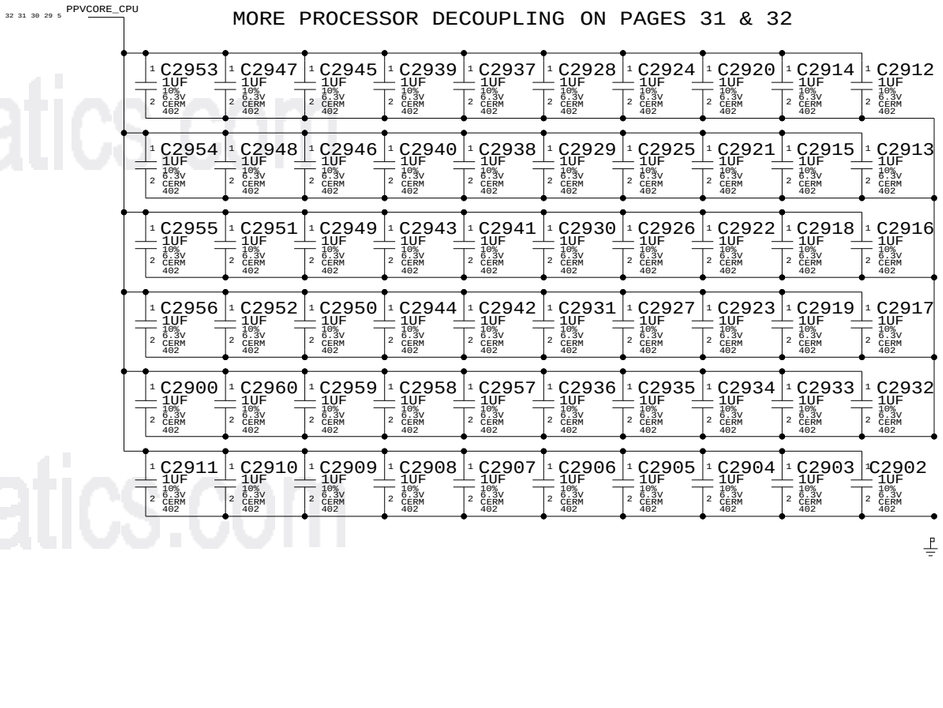
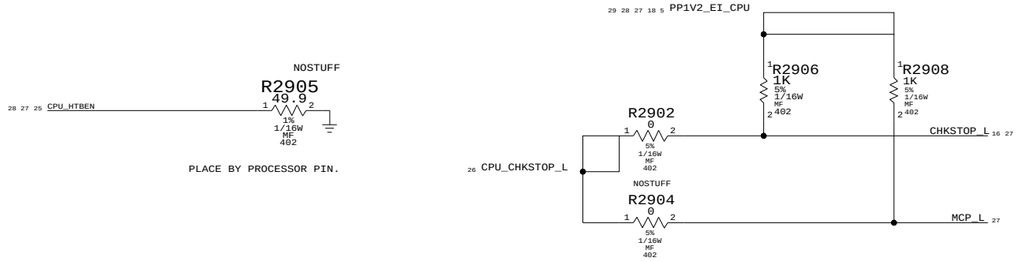
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 28 OF 103	







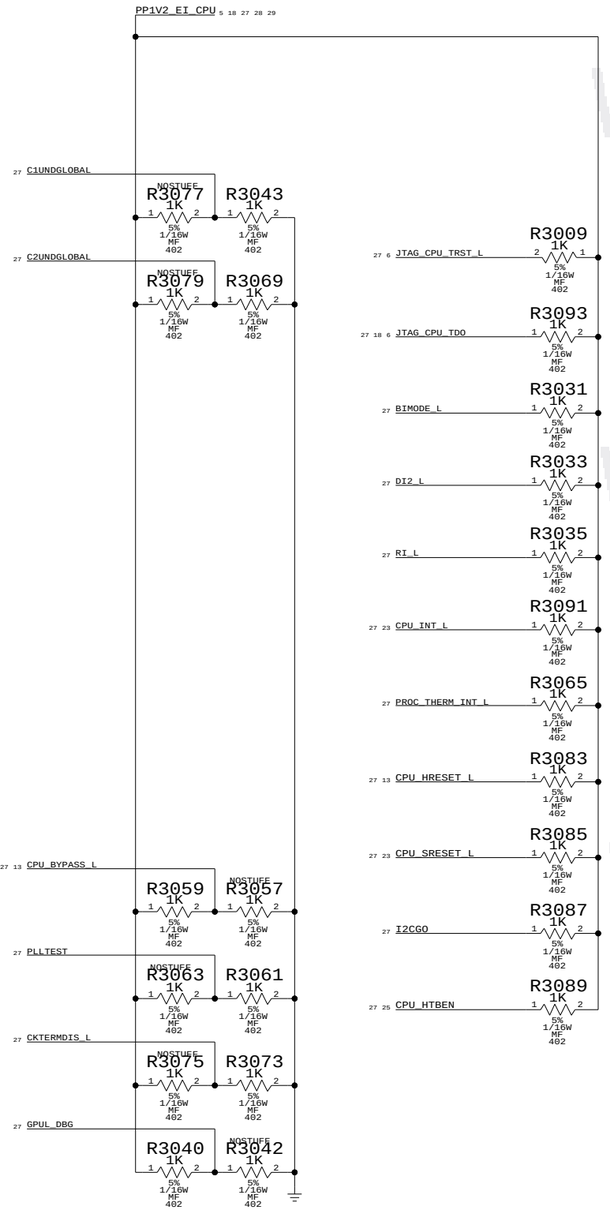
PROCESSOR LOGIC I/O

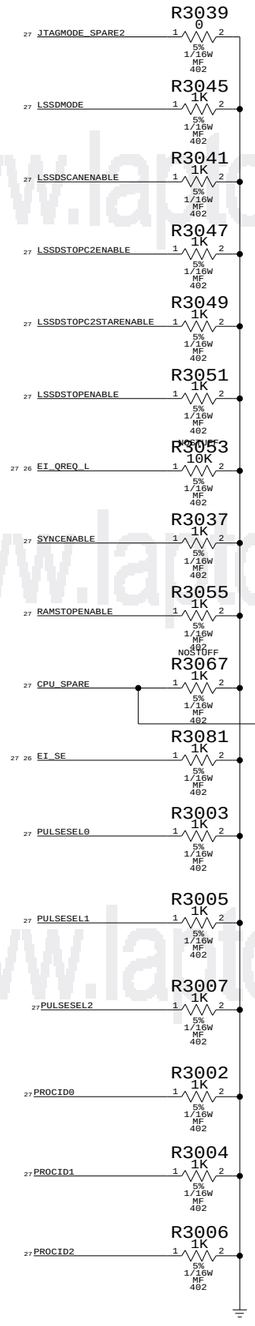
MASTER: GILA

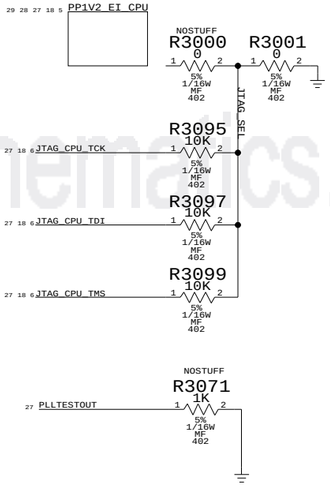
NEO APPLE PI

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 29 OF 103	







SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3034	EI_3TO1	SYSCLK * 12
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3018	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028	EI_2TO1	PROC / 2
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	EI_3TO1	PROC / 3
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF	PROC / 4
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3012	NOSTUFF	PROC / 6
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF	PROC / 8
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3012	NOSTUFF	PROC / 12
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3028	NOSTUFF	PROC / 16
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3036		
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF	BYPASS MODE

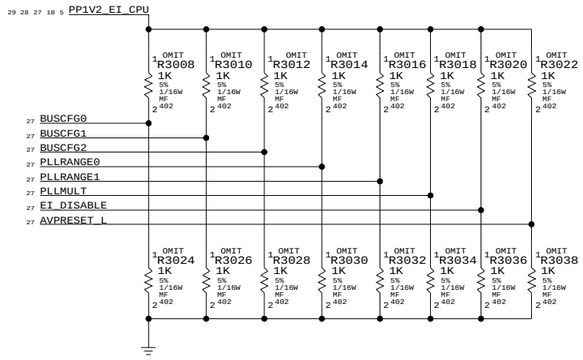
SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	CPU_PLL_LOW	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	CPU_PLL_HIGH	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032	CPU_PLL_MEDIUM	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3022		AVPRESET OFF
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3038	NOSTUFF	AVPRESET ON

* STUFF THESE ON Q45.

SYSTEM CONFIGURATION



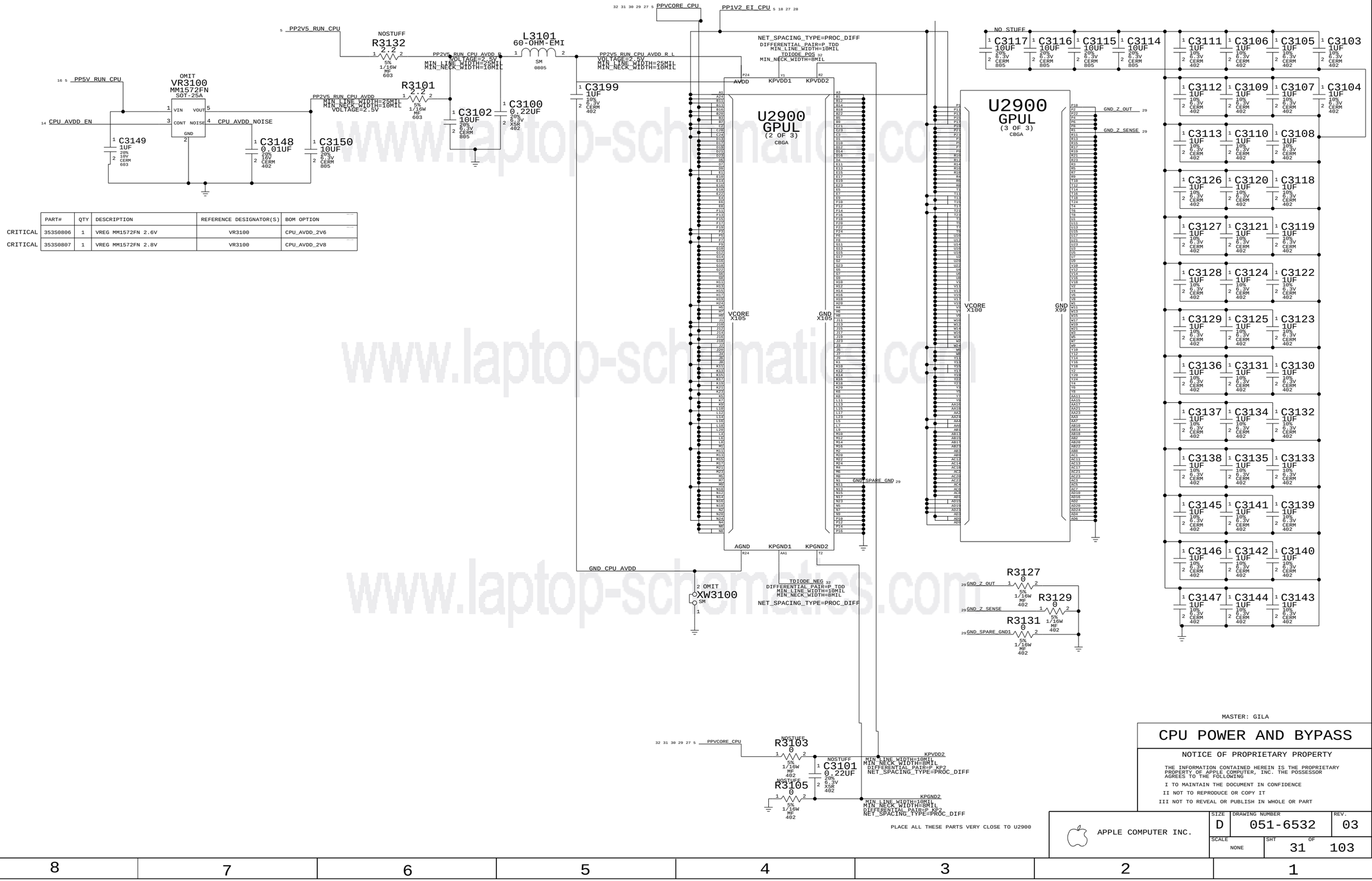
MASTER: GILA

CPU STRAPS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	30	103



	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL	353S0806	1	VREG MM1572FN 2.6V	VR3100	CPU_AVDD_2V6
CRITICAL	353S0807	1	VREG MM1572FN 2.8V	VR3100	CPU_AVDD_2V8

MASTER: GILA

CPU POWER AND BYPASS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	31	103

32 31 29 27 5 PPVCORE_CPU

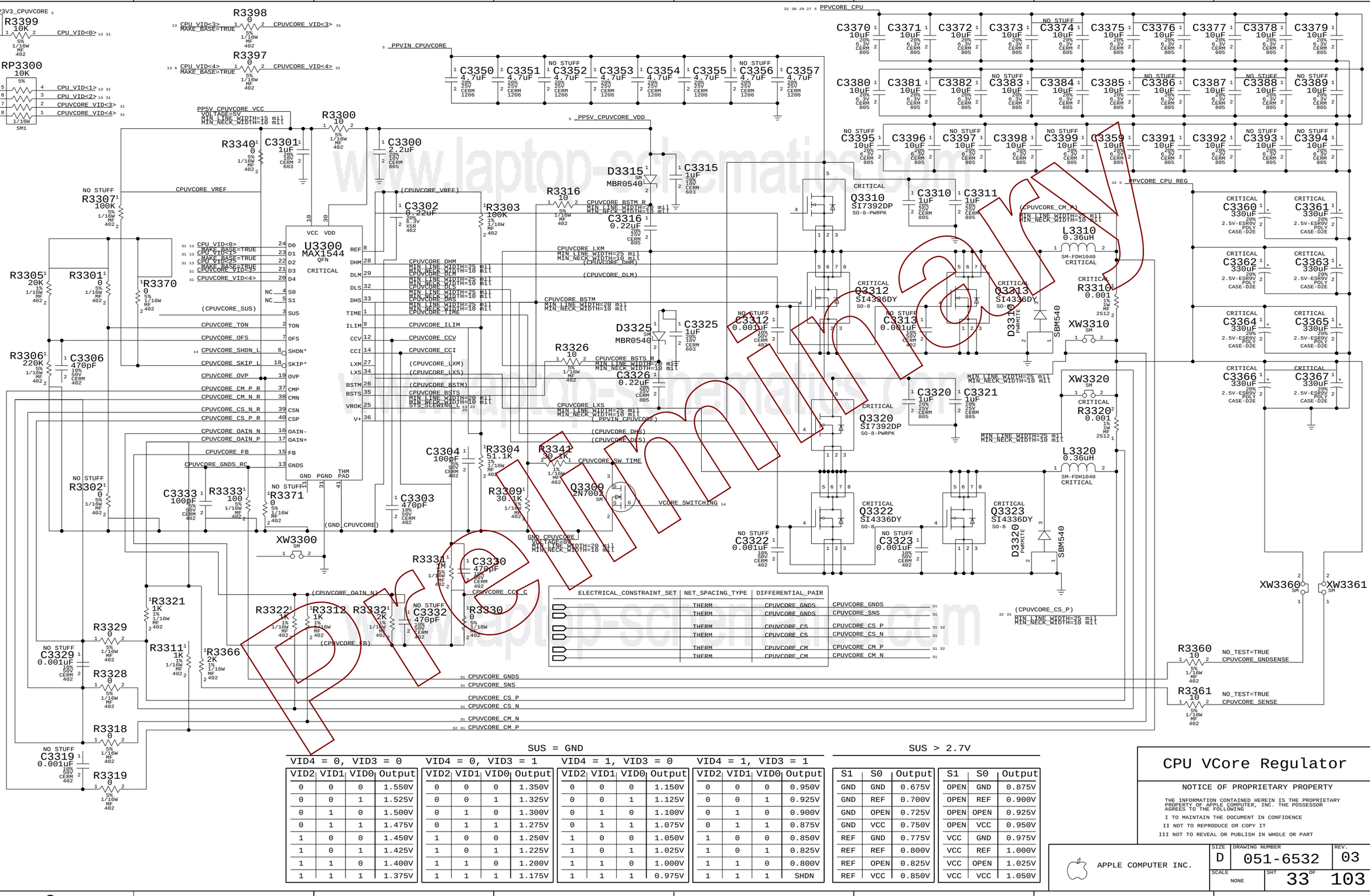
C3222 1UF 10% 6.3V CERM 402	C3221 1UF 10% 6.3V CERM 402	C3220 1UF 10% 6.3V CERM 402	C3219 1UF 10% 6.3V CERM 402	C3218 1UF 10% 6.3V CERM 402	C3217 1UF 10% 6.3V CERM 402	C3216 1UF 10% 6.3V CERM 402	C3215 1UF 10% 6.3V CERM 402	C3212 1UF 10% 6.3V CERM 402	C3200 1UF 10% 6.3V CERM 402
C3293 1UF 10% 6.3V CERM 402	C3268 1UF 10% 6.3V CERM 402	C3261 1UF 10% 6.3V CERM 402	C3259 1UF 10% 6.3V CERM 402	C3235 1UF 10% 6.3V CERM 402	C3232 1UF 10% 6.3V CERM 402	C3226 1UF 10% 6.3V CERM 402	C3224 1UF 10% 6.3V CERM 402	C3245 1UF 10% 6.3V CERM 402	C3223 1UF 10% 6.3V CERM 402
C3294 1UF 10% 6.3V CERM 402	C3269 1UF 10% 6.3V CERM 402	C3264 1UF 10% 6.3V CERM 402	C3260 1UF 10% 6.3V CERM 402	C3236 1UF 10% 6.3V CERM 402	C3233 1UF 10% 6.3V CERM 402	C3227 1UF 10% 6.3V CERM 402	C3225 1UF 10% 6.3V CERM 402	C3256 1UF 10% 6.3V CERM 402	C3234 1UF 10% 6.3V CERM 402
C3295 1UF 10% 6.3V CERM 402	C3271 1UF 10% 6.3V CERM 402	C3265 1UF 10% 6.3V CERM 402	C3262 1UF 10% 6.3V CERM 402	C3239 1UF 10% 6.3V CERM 402	C3237 1UF 10% 6.3V CERM 402	C3230 1UF 10% 6.3V CERM 402	C3228 1UF 10% 6.3V CERM 402	C3289 1UF 10% 6.3V CERM 402	C3267 1UF 10% 6.3V CERM 402
C3296 1UF 10% 6.3V CERM 402	C3270 1UF 10% 6.3V CERM 402	C3266 1UF 10% 6.3V CERM 402	C3263 1UF 10% 6.3V CERM 402	C3240 1UF 10% 6.3V CERM 402	C3238 1UF 10% 6.3V CERM 402	C3231 1UF 10% 6.3V CERM 402	C3229 1UF 10% 6.3V CERM 402	C3201 1UF 10% 6.3V CERM 402	C3278 1UF 10% 6.3V CERM 402
C3297 1UF 10% 6.3V CERM 402	C3282 1UF 10% 6.3V CERM 402	C3276 1UF 10% 6.3V CERM 402	C3272 1UF 10% 6.3V CERM 402	C3252 1UF 10% 6.3V CERM 402	C3250 1UF 10% 6.3V CERM 402	C3243 1UF 10% 6.3V CERM 402	C3241 1UF 10% 6.3V CERM 402	C3206 1UF 10% 6.3V CERM 402	C3204 1UF 10% 6.3V CERM 402
C3298 1UF 10% 6.3V CERM 402	C3281 1UF 10% 6.3V CERM 402	C3277 1UF 10% 6.3V CERM 402	C3273 1UF 10% 6.3V CERM 402	C3253 1UF 10% 6.3V CERM 402	C3251 1UF 10% 6.3V CERM 402	C3244 1UF 10% 6.3V CERM 402	C3242 1UF 10% 6.3V CERM 402	C3207 1UF 10% 6.3V CERM 402	C3205 1UF 10% 6.3V CERM 402
C3299 1UF 10% 6.3V CERM 402	C3284 1UF 10% 6.3V CERM 402	C3279 1UF 10% 6.3V CERM 402	C3274 1UF 10% 6.3V CERM 402	C3257 1UF 10% 6.3V CERM 402	C3254 1UF 10% 6.3V CERM 402	C3248 1UF 10% 6.3V CERM 402	C3246 1UF 10% 6.3V CERM 402	C3210 1UF 10% 6.3V CERM 402	C3208 1UF 10% 6.3V CERM 402
C3202 1UF 10% 6.3V CERM 402	C3283 1UF 10% 6.3V CERM 402	C3280 1UF 10% 6.3V CERM 402	C3275 1UF 10% 6.3V CERM 402	C3258 1UF 10% 6.3V CERM 402	C3255 1UF 10% 6.3V CERM 402	C3249 1UF 10% 6.3V CERM 402	C3247 1UF 10% 6.3V CERM 402	C3211 1UF 10% 6.3V CERM 402	C3209 1UF 10% 6.3V CERM 402
C3203 1UF 10% 6.3V CERM 402	C3292 1UF 10% 6.3V CERM 402	C3291 1UF 10% 6.3V CERM 402	C3290 1UF 10% 6.3V CERM 402	C3288 1UF 10% 6.3V CERM 402	C3287 1UF 10% 6.3V CERM 402	C3286 1UF 10% 6.3V CERM 402	C3285 1UF 10% 6.3V CERM 402	C3214 1UF 10% 6.3V CERM 402	C3213 1UF 10% 6.3V CERM 402

MASTER: GILA

PROC DECOUPLING

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 32 OF 103	



SUS = GND

VID4 = 0, VID3 = 0				VID4 = 0, VID3 = 1				VID4 = 1, VID3 = 0				VID4 = 1, VID3 = 1			
VID2	VID1	VID0	Output	VID2	VID1	VID0	Output	VID2	VID1	VID0	Output	VID2	VID1	VID0	Output
0	0	0	1.550V	0	0	0	1.350V	0	0	0	1.150V	0	0	0	0.950V
0	0	1	1.525V	0	0	1	1.325V	0	0	1	1.125V	0	0	1	0.925V
0	1	0	1.500V	0	1	0	1.300V	0	1	0	1.100V	0	1	0	0.900V
0	1	1	1.475V	0	1	1	1.275V	0	1	1	1.075V	0	1	1	0.875V
1	0	0	1.450V	1	0	0	1.250V	1	0	0	1.050V	1	0	0	0.850V
1	0	1	1.425V	1	0	1	1.225V	1	0	1	1.025V	1	0	1	0.825V
1	1	0	1.400V	1	1	0	1.200V	1	1	0	1.000V	1	1	0	0.800V
1	1	1	1.375V	1	1	1	1.175V	1	1	1	0.975V	1	1	1	SHDN

SUS > 2.7V

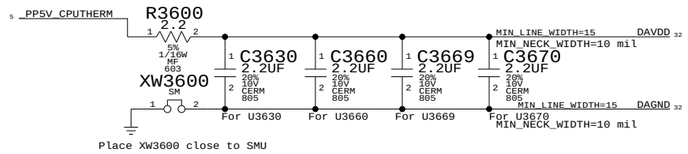
S1	S0	Output
GND	GND	0.675V
GND	REF	0.700V
GND	OPEN	0.725V
GND	VCC	0.750V
REF	GND	0.775V
REF	REF	0.800V
REF	OPEN	0.825V
REF	VCC	0.850V

S1	S0	Output
OPEN	GND	0.875V
OPEN	REF	0.900V
OPEN	OPEN	0.925V
OPEN	VCC	0.950V
VCC	GND	0.975V
VCC	REF	1.000V
VCC	OPEN	1.025V
VCC	VCC	1.050V

CPU VCore Regulator

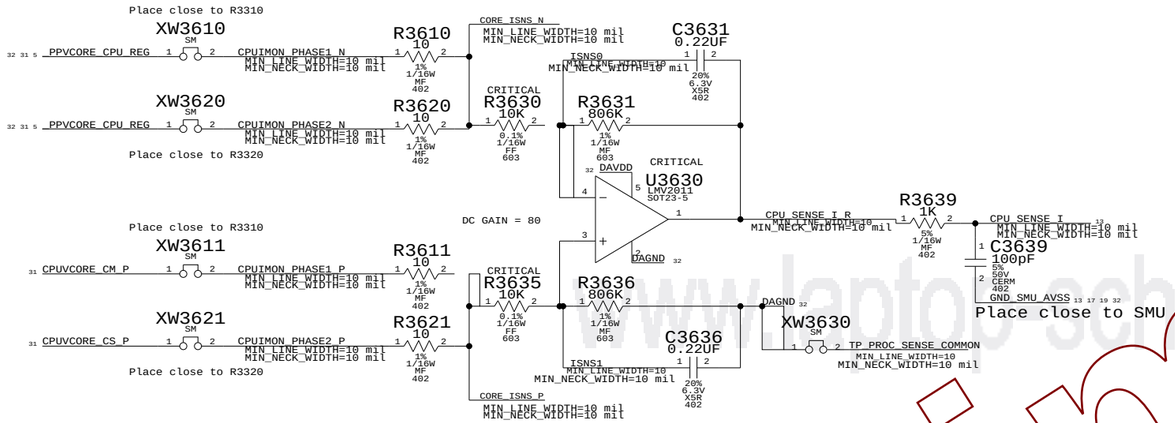
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 33 OF 103	



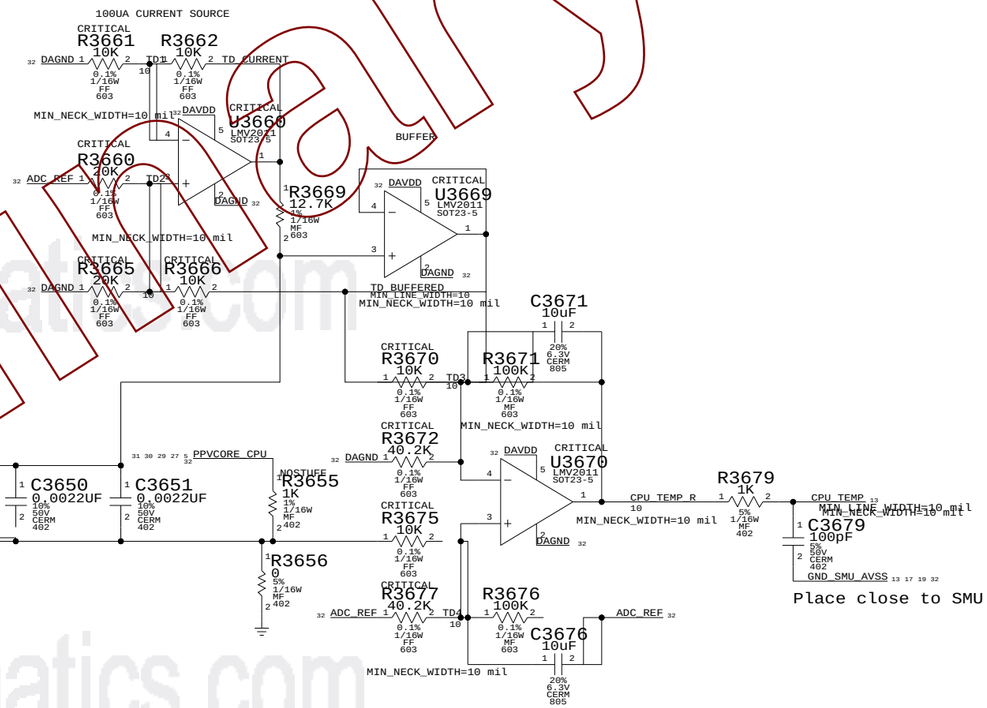
CPU Current Monitoring

Place close to CPU Power Supply

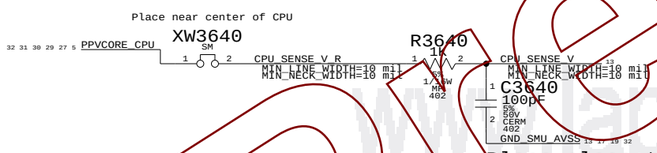


CPU Thermal Diode Circuit

Place close to CPU

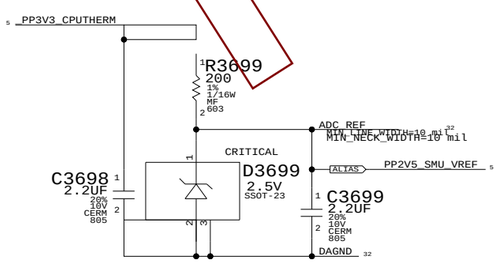


CPU Voltage Monitoring



SMU Voltage Reference

Place close to SMU



CPU Temp Monitoring

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 36 OF 103	

U3TWINS DO NOT HAVE MASKS

PP2V5_PWRON_RAM

U3 U3LITE V1.0-300MM PBGA (SYM 2 OF 7) OMIT

MEMORY DATA INTERFACE

RAM_DQ_R<0>	AF20	DDR_DQ0	DDR_DQ64	AG27	RAM_DQ_R<64>
RAM_DQ_R<1>	AH22	DDR_DQ1	DDR_DQ65	AF24	RAM_DQ_R<65>
RAM_DQ_R<2>	AH21	DDR_DQ2	DDR_DQ66	AE24	RAM_DQ_R<66>
RAM_DQ_R<3>	AG21	DDR_DQ3	DDR_DQ67	AG26	RAM_DQ_R<67>
RAM_DQ_R<4>	AB20	DDR_DQ4	DDR_DQ68	AF26	RAM_DQ_R<68>
RAM_DQ_R<5>	AC21	DDR_DQ5	DDR_DQ69	AD24	RAM_DQ_R<69>
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RAM_DQ_R<8>	AH26	DDR_DQ8	DDR_DQ72	AF28	RAM_DQ_R<72>
RAM_DQ_R<9>	AH25	DDR_DQ9	DDR_DQ73	AE28	RAM_DQ_R<73>
RAM_DQ_R<10>	AH24	DDR_DQ10	DDR_DQ74	AD26	RAM_DQ_R<74>
RAM_DQ_R<11>	AH23	DDR_DQ11	DDR_DQ75	AF27	RAM_DQ_R<75>
RAM_DQ_R<12>	AH27	DDR_DQ12	DDR_DQ76	AC26	RAM_DQ_R<76>
RAM_DQ_R<13>	AG24	DDR_DQ13	DDR_DQ77	AC25	RAM_DQ_R<77>
RAM_DQ_R<14>	AF23	DDR_DQ14	DDR_DQ78	AC27	RAM_DQ_R<78>
RAM_DQ_R<15>	AH28	DDR_DQ15	DDR_DQ79	AD27	RAM_DQ_R<79>
RAM_DQ_R<16>	U25	DDR_DQ16	DDR_DQ80	AA27	RAM_DQ_R<80>
RAM_DQ_R<17>	AA23	DDR_DQ17	DDR_DQ81	AA26	RAM_DQ_R<81>
RAM_DQ_R<18>	Y22	DDR_DQ18	DDR_DQ82	AA24	RAM_DQ_R<82>
RAM_DQ_R<19>	AA22	DDR_DQ19	DDR_DQ83	AA28	RAM_DQ_R<83>
RAM_DQ_R<20>	U24	DDR_DQ20	DDR_DQ84	Y26	RAM_DQ_R<84>
RAM_DQ_R<21>	V23	DDR_DQ21	DDR_DQ85	Y25	RAM_DQ_R<85>
RAM_DQ_R<22>	V22	DDR_DQ22	DDR_DQ86	Y28	RAM_DQ_R<86>
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RAM_DQ_R<29>	R24	DDR_DQ29	DDR_DQ93	V28	RAM_DQ_R<93>
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RAM_DQ_R<48>	B24	DDR_DQ48	DDR_DQ112	J25	RAM_DQ_R<112>
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RAM_DQ_R<61>	H21	DDR_DQ61	DDR_DQ125	C28	RAM_DQ_R<125>
RAM_DQ_R<62>	G21	DDR_DQ62	DDR_DQ126	E25	RAM_DQ_R<126>
RAM_DQ_R<63>	H22	DDR_DQ63	DDR_DQ127	E24	RAM_DQ_R<127>

PP1V5_PWRON_NB_AVDD

R3702 2.2 5% 1/16W MF 603

PP1V5_PWRON_RAM_NB_AVDD VOLTAGE=1.5V

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

C3745 1UF 10% 6.3V CERM 402

C3744 0.1UF 20% 10V CERM 402

PP2V5_PWRON_RAM

U3 U3LITE V1.0-300MM PBGA (SYM 3 OF 7) OMIT

DDR CLK_AVDD

VDD_DDR

MEMORY CONTROL INTERFACE

RAM_CLK66M_NB	AC20	DDR_CLKP	DDR_RAS	AE21	RAM_RAS_L_R
RAM_CLK_A_P_R	AA12	DDR_CK_A	DDR_CAS	AD20	RAM_CAS_L_R
RAM_CLK_A_N_R	AB12	DDR_CK_AN	DDR_WE	AC23	RAM_WE_L_R
RAM_CLK_B_P_R	AB14	DDR_CK_B	DDR_BA0	AF21	RAM_BA_R<0>
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RAM_CLK_C_N_R	AE14	DDR_CK_CN	DDR_MUXEN1	AH18	RAM_MUXEN1
RAM_CLK_D_P_R	AC14	DDR_CK_D	DDR_MAD0	AG12	RAM_A_R<0>
RAM_CLK_D_N_R	AD14	DDR_CK_DN	DDR_MAD1	AH13	RAM_A_R<1>
RAM_CLK_E_P_R	AD15	DDR_CK_E	DDR_MAD2	AH14	RAM_A_R<2>
RAM_CLK_E_N_R	AC15	DDR_CK_EN	DDR_MAD3	AH15	RAM_A_R<3>
RAM_CLK_F_P_R	AA15	DDR_CK_F	DDR_MAD4	AF12	RAM_A_R<4>
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RAM_CKE_R<0>	AC17	DDR_CKE0	DDR_MAD6	AD12	RAM_A_R<6>
RAM_CKE_R<1>	AD17	DDR_CKE1	DDR_MAD7	AC12	RAM_A_R<7>
RAM_CKE_R<2>	AE17	DDR_CKE2	DDR_MAD8	AG15	RAM_A_R<8>
RAM_CKE_R<3>	AF17	DDR_CKE3	DDR_MAD9	AF15	RAM_A_R<9>
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RAM_CKE_R<6>	AB18	DDR_CKE6	DDR_MAD12	AH17	RAM_A_R<12>
RAM_CKE_R<7>	AA18	DDR_CKE7	DDR_MAD13	AG17	RAM_A_R<13>
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	U21	DDR_VREF1	DDR_CS0	AF18	RAM_CS_L_R<0>
	L21	DDR_VREF2	DDR_CS1	AE18	RAM_CS_L_R<1>
	H20	DDR_VREF3	DDR_CS2	AG20	RAM_CS_L_R<2>
	AJ21	DDR_VREF4	DDR_CS3	AH20	RAM_CS_L_R<3>
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	J20	DDR_VREF7	DDR_CS10	AG18	RAM_CS_L_R<10>
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			DDR_DQSP1	AG23	RAM_DQS_R<1>
			DDR_DQSP2	Y23	RAM_DQS_R<2>
			DDR_DQSP3	R23	RAM_DQS_R<3>
			DDR_DQSP4	M22	RAM_DQS_R<4>
			DDR_DQSP5	B26	RAM_DQS_R<5>
			DDR_DQSP6	B27	RAM_DQS_R<6>
			DDR_DQSP7	F23	RAM_DQS_R<7>
			DDR_DQSP8	AE23	RAM_DQS_R<8>
			DDR_DQSP9	AD28	RAM_DQS_R<9>
			DDR_DQSP10	Y27	RAM_DQS_R<10>
			DDR_DQSP11	U28	RAM_DQS_R<11>
			DDR_DQSP12	M27	RAM_DQS_R<12>
			DDR_DQSP13	J28	RAM_DQS_R<13>
			DDR_DQSP14	F28	RAM_DQS_R<14>
			DDR_DQSP15	F25	RAM_DQS_R<15>

DDR_CLK_AVSS

PP2V5_PWRON_RAM

R3700 1K 1% 1/16W MF 402

R3701 1K 1% 1/16W MF 402

PP1V25_PWRON_RAM_VREF_NB VOLTAGE=1.25V

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

C3730 0.1UF 20% 10V CERM 402

C3746 0.1UF 20% 10V CERM 402

C3747 0.1UF 20% 10V CERM 402

C3748 0.1UF 20% 10V CERM 402

PP2V5_PWRON_RAM

C3700 C3701 C3702 C3703 C3704 C3705 C3706 C3707 C3708 C3709 C3710 C3711 C3712 C3713 C3714 C3731 C3732 C3733 C3734 C3735 C3736 C3737 0.1UF 20% 10V CERM 402

C3715 C3716 C3717 C3718 C3719 C3720 C3721 C3722 C3724 C3725 C3726 C3727 C3728 C3729 C3743 C3742 C3740 C3739 C3738 0.1UF 20% 10V CERM 402

MASTER: GILA

U3LITE MEMORY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 37 OF 103	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: SO-DIMMs only use 2 of the 3 clocks provided for each DIMM module. Unused clocks renamed below.

33 RAM_CLK_C_P_R — ALIAS — TP_RAM_CLK_C_P MAKE_BASE=TRUE
33 RAM_CLK_C_N_R — ALIAS — TP_RAM_CLK_C_N MAKE_BASE=TRUE
33 RAM_CLK_F_P_R — ALIAS — TP_RAM_CLK_F_P MAKE_BASE=TRUE
33 RAM_CLK_F_N_R — ALIAS — TP_RAM_CLK_F_N MAKE_BASE=TRUE

Series Termination for Clock/Control Signals

RPAKs can be swapped if the 3rd number in reference designator (RP38x0) is the same.

CLOCKS

62 33 RAM_CLK_A_P_R — RP3800 22 (1, 8) — RAM_CLK_A_P 35 62
62 33 RAM_CLK_A_N_R — RP3800 22 (2, 7) — RAM_CLK_A_N 35 62
62 33 RAM_CLK_B_P_R — RP3800 22 (4, 5) — RAM_CLK_B_P 35 62
62 33 RAM_CLK_B_N_R — RP3800 22 (3, 6) — RAM_CLK_B_N 35 62
62 33 RAM_CLK_D_P_R — RP3801 22 (3, 6) — RAM_CLK_D_P 35 62
62 33 RAM_CLK_D_N_R — RP3801 22 (4, 5) — RAM_CLK_D_N 35 62
62 33 RAM_CLK_E_P_R — RP3801 22 (1, 8) — RAM_CLK_E_P 35 62
62 33 RAM_CLK_E_N_R — RP3801 22 (2, 7) — RAM_CLK_E_N 35 62

5% 1/16W SM1

CS

62 33 RAM_CS_L_R<0> — RP3810 22 (2, 7) — RAM_CS_L<0> 35 62
62 33 RAM_CS_L_R<1> — RP3810 22 (3, 6) — RAM_CS_L<1> 35 62
62 33 RAM_CS_L_R<8> — RP3810 22 (1, 8) — RAM_CS_L<8> 35 62
62 33 RAM_CS_L_R<9> — RP3810 22 (4, 5) — RAM_CS_L<9> 35 62

CKE

62 33 RAM_CKE_R<0> — RP3820 22 (4, 5) — RAM_CKE<0> 34 35 62
62 33 RAM_CKE_R<1> — RP3820 22 (3, 6) — RAM_CKE<1> 34 35 62
62 33 RAM_CKE_R<4> — RP3820 22 (1, 8) — RAM_CKE<4> 34 35 62
62 33 RAM_CKE_R<5> — RP3820 22 (2, 7) — RAM_CKE<5> 34 35 62

ADDR

62 33 RAM_A_R<0> — RP3830 22 (2, 7) — RAM_A<0> 35 62
62 33 RAM_A_R<1> — RP3830 22 (4, 5) — RAM_A<1> 35 62
62 33 RAM_A_R<2> — RP3830 22 (1, 8) — RAM_A<2> 35 62
62 33 RAM_A_R<3> — RP3830 22 (3, 6) — RAM_A<3> 35 62
62 33 RAM_A_R<4> — RP3831 22 (2, 7) — RAM_A<4> 35 62
62 33 RAM_A_R<5> — RP3831 22 (3, 6) — RAM_A<5> 35 62
62 33 RAM_A_R<6> — RP3831 22 (1, 8) — RAM_A<6> 35 62
62 33 RAM_A_R<7> — RP3831 22 (4, 5) — RAM_A<7> 35 62
62 33 RAM_A_R<8> — RP3832 22 (3, 6) — RAM_A<8> 35 62
62 33 RAM_A_R<9> — RP3832 22 (1, 8) — RAM_A<9> 35 62
62 33 RAM_A_R<10> — RP3832 22 (4, 5) — RAM_A<10> 35 62
62 33 RAM_A_R<11> — RP3832 22 (2, 7) — RAM_A<11> 35 62
62 33 RAM_A_R<12> — RP3833 22 (4, 5) — RAM_A<12> 35 62
62 33 RAM_A_R<13> — RP3833 22 (3, 6) — RAM_A<13> 35 62

BA

62 33 RAM_BA_R<0> — RP3833 22 (1, 8) — RAM_BA<0> 35
62 33 RAM_BA_R<1> — RP3833 22 (2, 7) — RAM_BA<1> 35

CNTL

62 33 RAM_WE_L_R — R3840 22 (1, 2) — RAM_WE_L 35
62 33 RAM_CAS_L_R — RP3841 22 (1, 2) — RAM_CAS_L 35
62 33 RAM_RAS_L_R — R3842 22 (1, 2) — RAM_RAS_L 35

5% 1/16W MF 402

CKE pulldowns to put RAM into self refresh during sleep

62 35 34 RAM_CKE<0> — RP3850 10K (2, 7)
62 35 34 RAM_CKE<1> — RP3850 10K (4, 5)
62 35 34 RAM_CKE<4> — RP3850 10K (1, 8)
62 35 34 RAM_CKE<5> — RP3850 10K (3, 6)

5% 1/16W SM1

No series termination on data signals

DIMM "A"

62 33 RAM_DQ_R<0> — ALIAS — RAM_DQ<0> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<1> — ALIAS — RAM_DQ<1> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<2> — ALIAS — RAM_DQ<2> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<3> — ALIAS — RAM_DQ<3> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<4> — ALIAS — RAM_DQ<4> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<5> — ALIAS — RAM_DQ<5> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<6> — ALIAS — RAM_DQ<6> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<7> — ALIAS — RAM_DQ<7> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<8> — ALIAS — RAM_DQ<8> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<9> — ALIAS — RAM_DQ<9> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<10> — ALIAS — RAM_DQ<10> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<11> — ALIAS — RAM_DQ<11> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<12> — ALIAS — RAM_DQ<12> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<13> — ALIAS — RAM_DQ<13> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<14> — ALIAS — RAM_DQ<14> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<15> — ALIAS — RAM_DQ<15> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<16> — ALIAS — RAM_DQ<16> MAKE_BASE=TRUE 35 62
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62 33 RAM_DQ_R<18> — ALIAS — RAM_DQ<18> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<19> — ALIAS — RAM_DQ<19> MAKE_BASE=TRUE 35 62
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62 33 RAM_DQ_R<22> — ALIAS — RAM_DQ<22> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<23> — ALIAS — RAM_DQ<23> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<24> — ALIAS — RAM_DQ<24> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<25> — ALIAS — RAM_DQ<25> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<26> — ALIAS — RAM_DQ<26> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<27> — ALIAS — RAM_DQ<27> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<28> — ALIAS — RAM_DQ<28> MAKE_BASE=TRUE 35 62
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62 33 RAM_DQ_R<31> — ALIAS — RAM_DQ<31> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<32> — ALIAS — RAM_DQ<32> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<33> — ALIAS — RAM_DQ<33> MAKE_BASE=TRUE 35 62
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62 33 RAM_DQ_R<51> — ALIAS — RAM_DQ<51> MAKE_BASE=TRUE 35 62
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62 33 RAM_DQ_R<55> — ALIAS — RAM_DQ<55> MAKE_BASE=TRUE 35 62
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62 33 RAM_DQ_R<59> — ALIAS — RAM_DQ<59> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<60> — ALIAS — RAM_DQ<60> MAKE_BASE=TRUE 35 62
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62 33 RAM_DQ_R<62> — ALIAS — RAM_DQ<62> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<63> — ALIAS — RAM_DQ<63> MAKE_BASE=TRUE 35 62

DIMM "B"

62 33 RAM_DQ_R<64> — ALIAS — RAM_DQ<64> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<65> — ALIAS — RAM_DQ<65> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<66> — ALIAS — RAM_DQ<66> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<67> — ALIAS — RAM_DQ<67> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<68> — ALIAS — RAM_DQ<68> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<69> — ALIAS — RAM_DQ<69> MAKE_BASE=TRUE 35 62
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62 33 RAM_DQ_R<126> — ALIAS — RAM_DQ<126> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<127> — ALIAS — RAM_DQ<127> MAKE_BASE=TRUE 35 62

No series termination on strobe signals

62 33 RAM_DQS_R<0> — ALIAS — RAM_DQS<0> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<1> — ALIAS — RAM_DQS<1> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<2> — ALIAS — RAM_DQS<2> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<3> — ALIAS — RAM_DQS<3> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<4> — ALIAS — RAM_DQS<4> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<5> — ALIAS — RAM_DQS<5> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<6> — ALIAS — RAM_DQS<6> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<7> — ALIAS — RAM_DQS<7> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<8> — ALIAS — RAM_DQS<8> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<9> — ALIAS — RAM_DQS<9> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<10> — ALIAS — RAM_DQS<10> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<11> — ALIAS — RAM_DQS<11> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<12> — ALIAS — RAM_DQS<12> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<13> — ALIAS — RAM_DQS<13> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<14> — ALIAS — RAM_DQS<14> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<15> — ALIAS — RAM_DQS<15> MAKE_BASE=TRUE 35 62

Memory Series Term

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	38	103

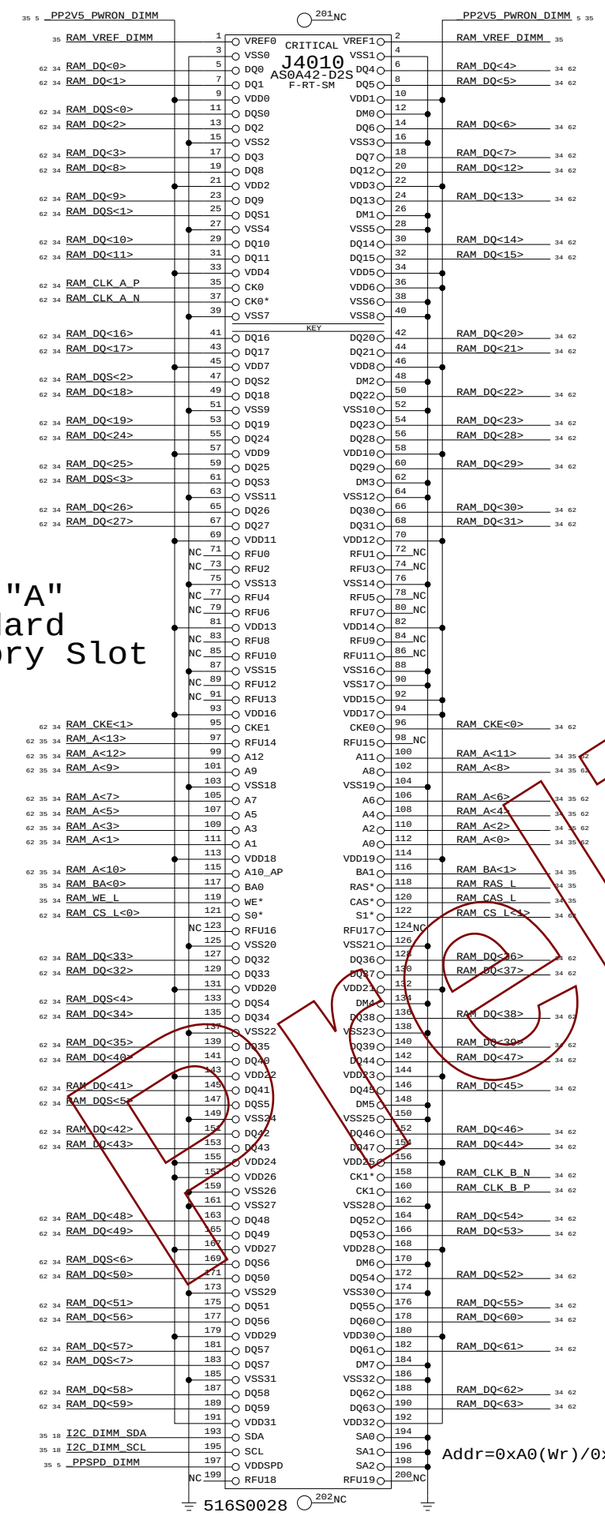
Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_DIMM
- _PPSPD_DIMM (2.5V - 3.3V)

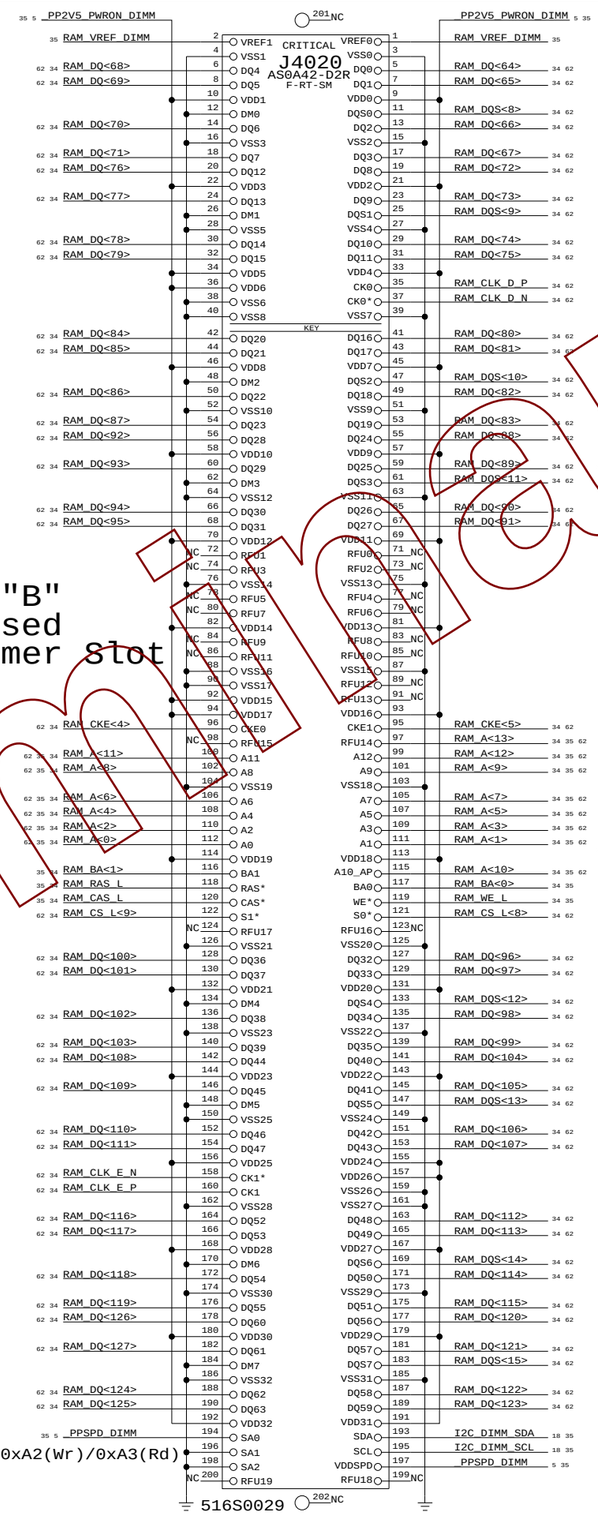
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Slot "A" Standard Factory Slot



Slot "B" Reversed Customer Slot

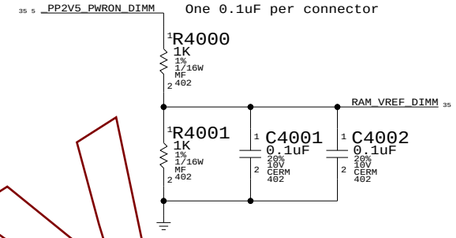


Addr=0xA0(Wr)/0xA1(Rd)

Addr=0xA2(Wr)/0xA3(Rd)

DDR VRef

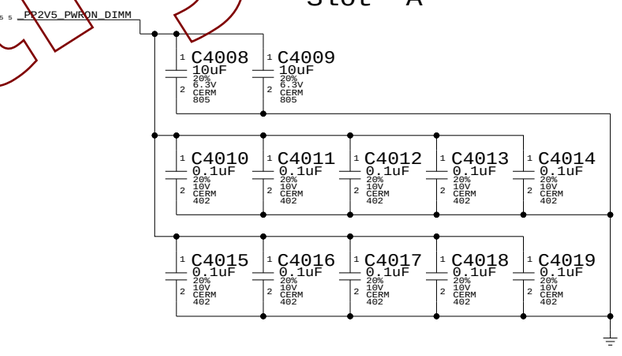
One 0.1uF per connector



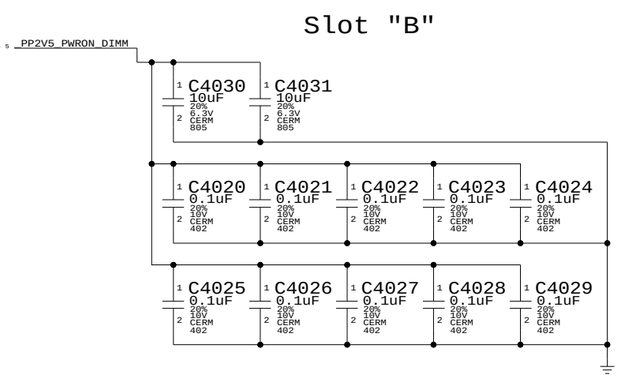
DDR Bypass Caps

(For return current)

Slot "A"



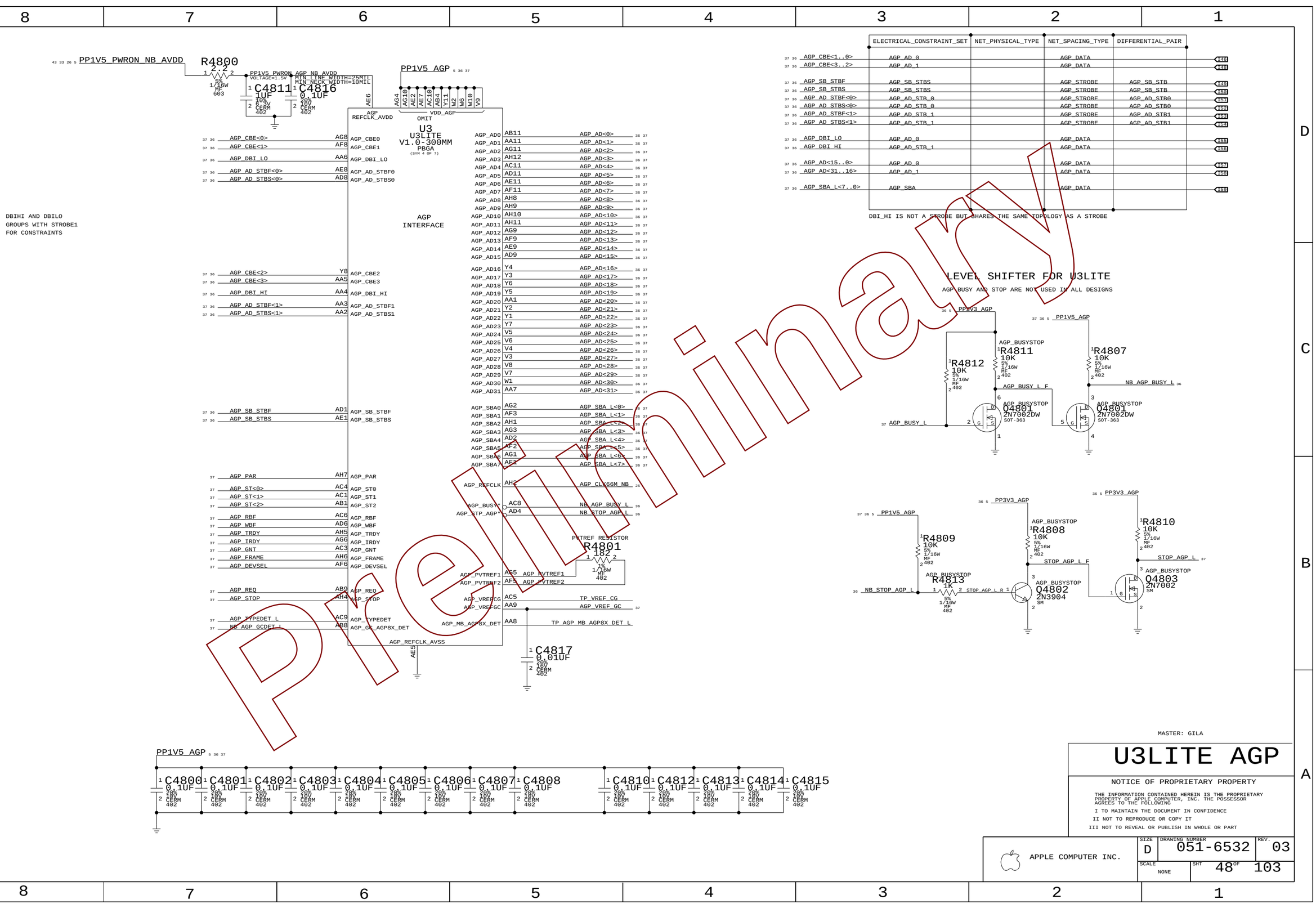
Slot "B"



DDR SODIMM CONNS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 40 OF 103	


43 33 26 5 PP1V5_PWRON_NB_AVDD
R4800
2.2
5%
1/16W
MF
603
PP1V5_PWRON_NB_AVDD
VOLTAGE=1.5V
MIN_LINE_WIDTH=25MIL
MIN_NECK_WIDTH=10MIL
C4811
1UF
10%
6.3V
CERM
402
C4816
0.1UF
20%
10V
CERM
402
PP1V5_AGP 5 36 37
AE6
AG4
AG10
AE2
AE7
AC10
AB4
Y11
W2
W6
W10
V9
AGP
REFCLK_AVDD
VDD_AGP
OMIT
U3
U3LITE
V1.0-300MM
PBGA
(SYM 4 OF 7)
37 36 AGP_CBE<0>
37 36 AGP_CBE<1>
37 36 AGP_DBI_LO
37 36 AGP_AD_STBF<0>
37 36 AGP_AD_STBS<0>
AG8 AGP_CBE0
AF8 AGP_CBE1
AA6 AGP_DBI_LO
AE8 AGP_AD_STBF0
AD8 AGP_AD_STBS0
DBIHI AND DBILO
GROUPS WITH STROBE1
FOR CONSTRAINTS
AGP
INTERFACE
AGP_AD0 AB11 AGP_AD<0> 36 37
AGP_AD1 AA11 AGP_AD<1> 36 37
AGP_AD2 AG11 AGP_AD<2> 36 37
AGP_AD3 AH12 AGP_AD<3> 36 37
AGP_AD4 AC11 AGP_AD<4> 36 37
AGP_AD5 AD11 AGP_AD<5> 36 37
AGP_AD6 AE11 AGP_AD<6> 36 37
AGP_AD7 AF11 AGP_AD<7> 36 37
AGP_AD8 AH8 AGP_AD<8> 36 37
AGP_AD9 AH9 AGP_AD<9> 36 37
AGP_AD10 AH10 AGP_AD<10> 36 37
AGP_AD11 AH11 AGP_AD<11> 36 37
AGP_AD12 AG9 AGP_AD<12> 36 37
AGP_AD13 AF9 AGP_AD<13> 36 37
AGP_AD14 AE9 AGP_AD<14> 36 37
AGP_AD15 AD9 AGP_AD<15> 36 37
AGP_AD16 Y4 AGP_AD<16> 36 37
AGP_AD17 Y3 AGP_AD<17> 36 37
AGP_AD18 Y6 AGP_AD<18> 36 37
AGP_AD19 Y5 AGP_AD<19> 36 37
AGP_AD20 AA1 AGP_AD<20> 36 37
AGP_AD21 Y2 AGP_AD<21> 36 37
AGP_AD22 Y1 AGP_AD<22> 36 37
AGP_AD23 Y7 AGP_AD<23> 36 37
AGP_AD24 V5 AGP_AD<24> 36 37
AGP_AD25 V6 AGP_AD<25> 36 37
AGP_AD26 V4 AGP_AD<26> 36 37
AGP_AD27 V3 AGP_AD<27> 36 37
AGP_AD28 V8 AGP_AD<28> 36 37
AGP_AD29 V7 AGP_AD<29> 36 37
AGP_AD30 W1 AGP_AD<30> 36 37
AGP_AD31 AA7 AGP_AD<31> 36 37
37 36 AGP_CBE<2>
37 36 AGP_CBE<3>
37 36 AGP_DBI_HI
37 36 AGP_AD_STBF<1>
37 36 AGP_AD_STBS<1>
Y8 AGP_CBE2
AA5 AGP_CBE3
AA4 AGP_DBI_HI
AA3 AGP_AD_STBF1
AA2 AGP_AD_STBS1
AGP_SBA0 AG2 AGP_SBA_L<0> 36 37
AGP_SBA1 AF3 AGP_SBA_L<1> 36 37
AGP_SBA2 AH1 AGP_SBA_L<2> 36 37
AGP_SBA3 AG3 AGP_SBA_L<3> 36 37
AGP_SBA4 AD2 AGP_SBA_L<4> 36 37
AGP_SBA5 AF2 AGP_SBA_L<5> 36 37
AGP_SBA6 AG1 AGP_SBA_L<6> 36 37
AGP_SBA7 AF1 AGP_SBA_L<7> 36 37
37 AGP_SB_STBF
37 AGP_SB_STBS
AD1 AGP_SB_STBF
AE1 AGP_SB_STBS
37 AGP_PAR
37 AGP_ST<0>
37 AGP_ST<1>
37 AGP_ST<2>
37 AGP_RBF
37 AGP_WBF
37 AGP_TRDY
37 AGP_IRDY
37 AGP_GNT
37 AGP_FRAME
37 AGP_DEVSEL
AH7 AGP_PAR
AC4 AGP_ST0
AC1 AGP_ST1
AB1 AGP_ST2
AC6 AGP_RBF
AD6 AGP_WBF
AH5 AGP_TRDY
AG6 AGP_IRDY
AC3 AGP_GNT
AH6 AGP_FRAME
AF6 AGP_DEVSEL
37 AGP_REQ
37 AGP_STOP
AB9 AGP_REQ
AH4 AGP_STOP
37 AGP_TYPEDET_L
37 NB_AGP_GCDET_L
AC9 AGP_TYPEDET
AB8 AGP_GC_AGP8X_DET
AGP_REFCLK_AVSS
AE5
AGP_REFCLK AH2 AGP_CLK66M_NB 25
AGP_BUSY* AC8 NB_AGP_BUSY_L 36
AGP_STP_AGP* AD4 NB_STOP_AGP_L 36
PVTREF RESISTOR
R4801
182
1%
1/16W
MF
402
AGP_PVTREF1 AE5 AGP_PVTREF1
AGP_PVTREF2 AF5 AGP_PVTREF2
AGP_VREFCG AC5 TP_VREF_CG
AGP_VREFGC AA9 AGP_VREF_GC 37
AGP_MB_AGP8X_DET AA8 TP_AGP_MB_AGP8X_DET_L
C4817
0.01UF
20%
16V
CERM
402
ELECTRICAL_CONSTRAINT_SET
NET_PHYSICAL_TYPE
NET_SPACING_TYPE
DIFFERENTIAL_PAIR
37 36 AGP_CBE<1..0> AGP_AD_0 AGP_DATA 146
37 36 AGP_CBE<3..2> AGP_AD_1 AGP_DATA 148
37 36 AGP_SB_STBF AGP_SB_STBS AGP_STROBE AGP_SB_STB 140
37 36 AGP_SB_STBS AGP_SB_STBS AGP_STROBE AGP_SB_STB 160
37 36 AGP_AD_STBF<0> AGP_AD_STB_0 AGP_STROBE AGP_AD_STB0 151
37 36 AGP_AD_STBS<0> AGP_AD_STB_0 AGP_STROBE AGP_AD_STB0 152
37 36 AGP_AD_STBF<1> AGP_AD_STB_1 AGP_STROBE AGP_AD_STB1 153
37 36 AGP_AD_STBS<1> AGP_AD_STB_1 AGP_STROBE AGP_AD_STB1 154
37 36 AGP_DBI_LO AGP_AD_0 AGP_DATA 155
37 36 AGP_DBI_HI AGP_AD_STB_1 AGP_DATA 156
37 36 AGP_AD<15..0> AGP_AD_0 AGP_DATA 157
37 36 AGP_AD<31..16> AGP_AD_1 AGP_DATA 158
37 36 AGP_SBA_L<7..0> AGP_SBA AGP_DATA 159
DBI_HI IS NOT A STROBE BUT SHARES THE SAME TOPOLOGY AS A STROBE
LEVEL SHIFTER FOR U3LITE
AGP BUSY AND STOP ARE NOT USED IN ALL DESIGNS
36 5 PP3V3_AGP
37 36 5 PP1V5_AGP
R4812
10K
5%
1/16W
MF
402
AGP_BUSYSTOP
R4811
10K
5%
1/16W
MF
402
R4807
10K
5%
1/16W
MF
402
AGP_BUSY_L_F
NB_AGP_BUSY_L 36
37 AGP_BUSY_L
Q4801
2N7002DW
SOT-363
AGP_BUSYSTOP
Q4801
2N7002DW
SOT-363
36 5 PP3V3_AGP
37 36 5 PP1V5_AGP
R4809
10K
5%
1/16W
MF
402
AGP_BUSYSTOP
R4808
10K
5%
1/16W
MF
402
R4810
10K
5%
1/16W
MF
402
STOP_AGP_L_F
STOP_AGP_L 37
36 NB_STOP_AGP_L
R4813
1K
5%
1/16W
MF
402
STOP_AGP_L_R
AGP_BUSYSTOP
Q4802
2N3904
SM
AGP_BUSYSTOP
Q4803
2N7002
SM
PP1V5_AGP 5 36 37
C4800 0.1UF 20% 10V CERM 402
C4801 0.1UF 20% 10V CERM 402
C4802 0.1UF 20% 10V CERM 402
C4803 0.1UF 20% 10V CERM 402
C4804 0.1UF 20% 10V CERM 402
C4805 0.1UF 20% 10V CERM 402
C4806 0.1UF 20% 10V CERM 402
C4807 0.1UF 20% 10V CERM 402
C4808 0.1UF 20% 10V CERM 402
C4810 0.1UF 20% 10V CERM 402
C4812 0.1UF 20% 10V CERM 402
C4813 0.1UF 20% 10V CERM 402
C4814 0.1UF 20% 10V CERM 402
C4815 0.1UF 20% 10V CERM 402
MASTER: GILA
U3LITE AGP
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REV. 03
SCALE NONE
SHT 48 OF 103
Preliminary

U3LITE AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALL)

PP1V5_AGP
R4802 3.32K 1% 1/16W MF 402
AGP_VREF_GC
R4803 1.02K 1% 1/16W MF 402
C4818 0.01UF 20% 16V CERM 402

CRITICAL
U4900 RAGE_MOBILITY M10-CSP64 64MB BGA (1 OF 6) OMIT

PP3V3_GPU
PP1V5_GPU_AGP
R4920 47 5% 1/16W MF 402
NO STUFF
R4906 10K 5% 1/16W MF 402 AGP 4X
R4902 10K 5% 1/16W MF 402
R4913 10K 5% 1/16W MF 402 AGP 8X
U3LITE SIGNAL
AGP_TYPEDET_L
R4914 0 5% 1/16W MF 402
C4912 0.1UF 20% 16V CERM 402
C4913 0.01UF 20% 16V CERM 402
(PLACE C4913 CLOSE TO AGPREF PIN)
AGP_VREF_GC
MIN_LINE_WIDTH=8 mil
MIN_NECK_WIDTH=8 mil

AGP_AD<31>	AB30	AD31	
AGP_AD<30>	AB27	AD30	
AGP_AD<29>	AA29	AD29	
AGP_AD<28>	AB28	AD28	
AGP_AD<27>	AA30	AD27	
AGP_AD<26>	AA27	AD26	
AGP_AD<25>	Y30	AD25	
AGP_AD<24>	AA28	AD24	
AGP_AD<23>	W30	AD23	
AGP_AD<22>	W27	AD22	
AGP_AD<21>	V30	AD21	
AGP_AD<20>	V28	AD20	
AGP_AD<19>	V29	AD19	
AGP_AD<18>	V27	AD18	
AGP_AD<17>	U30	AD17	
AGP_AD<16>	U28	AD16	
AGP_AD<15>	R27	AD15	
AGP_AD<14>	R29	AD14	
AGP_AD<13>	P28	AD13	
AGP_AD<12>	P30	AD12	
AGP_AD<11>	P27	AD11	
AGP_AD<10>	P29	AD10	
AGP_AD<9>	N28	AD9	
AGP_AD<8>	N30	AD8	
AGP_AD<7>	M30	AD7	
AGP_AD<6>	M27	AD6	
AGP_AD<5>	M29	AD5	
AGP_AD<4>	L28	AD4	
AGP_AD<3>	L30	AD3	
AGP_AD<2>	L27	AD2	
AGP_AD<1>	L29	AD1	
AGP_AD<0>	K28	AD0	

AGP_CBE<3>	W28	CBEB3	
AGP_CBE<2>	U29	CBEB2	
AGP_CBE<1>	R30	CBEB1	
AGP_CBE<0>	N27	CBEB0	
AGP_CLK66M_GPU	AG30	PCICLK	
AGP_FRAME	U27	FRAMEB	
AGP_IRDY	T30	IRDYB	
AGP_TRDY	T28	TRDYB	
AGP_STOP	T27	STOPB	
AGP_DEVSEL	T29	DEVSELB	
AGP_PAR	R28	PAR	
AGP_REQ	AF29	REQB	
AGP_GNT	AF27	GNTB	
AGP_INT_L	AH29	INTAB	
GPU_RESET_L_R	AH30	RSTB	
AGP_WBF	AE27	WBF	
AGP_ATI_VREFG	AK3	VREFG	
AGP_ATI_MVREF	D8	VREF	

AGP_AD_STBF0	N29	AD_STB0	
AGP_AD_STBF<1>	W29	AD_STB1	
AGP_AD_STBS<0>	M28	AD_STBB0	
AGP_AD_STBS<1>	Y29	AD_STBB1	
AGP_BUSY_L	AG28	AGP_BUSYB	
	K30	AGPREF	
GPU_AGP_TEST	K29	AGPTEST	
NB_AGP_GCDET_L	U25	AGP8X_DETB	
AGP_SUS_STAT_L_PU	AJ28	SUS_STAT	
AGP_ST<0>	AF30	ST0	
AGP_ST<1>	AF28	ST1	
AGP_ST<2>	AE29	ST2	
AGP_SBA_L<7>	AC28	SBA7	
AGP_SBA_L<6>	AB29	SBA6	
AGP_SBA_L<5>	AC27	SBA5	
AGP_SBA_L<4>	AC30	SBA4	
AGP_SBA_L<3>	AD27	SBA3	
AGP_SBA_L<2>	AD30	SBA2	
AGP_SBA_L<1>	AE28	SBA1	
AGP_SBA_L<0>	AD29	SBA0	
AGP_RBF	AE30	RBFB	
STOP_AGP_L	AG29	STP_AGPB	
AGP_SB_STBF	AC29	SB_STB	
AGP_SB_STBS	AD28	SB_STBS	
ATI_RSTB_MSK	AD24	RSTB_MSK	
AGP_DBI_LO	Y25	DBI_LO	
AGP_DBI_HI	Y27	DBI_HI	

R4905 0 5% 1/16W MF 402

OMIT
U4900 RAGE_MOBILITY M10-CSP64 64MB BGA (6 OF 6)
VSS
VDDCI

U4900 RAGE_MOBILITY M10-CSP64 64MB BGA (2 OF 6)
OMIT
VSS
VSS
VSS
VSS

27MHz OSC
(PLACE THE OSCILLATOR AND R4981 AND RR4982 CLOSE TO GPU PIN AJ29)

PP3V3_GPU
L4980 FERR-EMI-100-OHM SM
PP3V3_GPU_OSC
VOLTAGE=3.3V
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil
C4981 0.1UF 20% 16V CERM 402
C4980 4.7UF 20% 6.3V CERM 805
NO STUFF
R4980 100K 5% 1/16W MF 402
CRITICAL
G4980 27.0000M OSC SM-1
VCC
OE
OUT
GND
GPU_OSC_OE
GPU_CLK27M_OSC
(PLACE R4985 CLOSE TO OSC)
GPU_SS
R4985 0 5% 1/16W MF 402
GPUSS_CLK27M
R4981 287 1% 1/16W MF 402
R4982 162 1% 1/16W MF 402
GPU_CLK27M_DIV

S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT

PP3V3_GPU
L4990 FERR-EMI-100-OHM SM
PP3V3_GPUSS_VDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil
GPU_SS
C4990 10uF 20% 6.3V CERM 805
C4991 0.1UF 20% 16V CERM 402
NO STUFF
R4990 0 5% 1/16W MF 402
R4991 0 5% 1/16W MF 402
GPUSS_CLK27M
CRITICAL
VDD
U4990 CY25811 SOI
XIN/CLKIN
XOUT
SSCLK
FRSEL
S1
S0
VSS
GPU_SSCLK_UF
R4995 33 5% 1/16W MF 402
GPU_SSCLK_IN
GPUSS_S1
GPUSS_S0
NO STUFF
R4992 0 5% 1/16W MF 402
NO STUFF
R4993 0 5% 1/16W MF 402

PP3V3_GPU
R4900 47 5% 1/16W MF 402
R4901 10K 5% 1/16W MF 402
GPU_RESET_L
R4909 1K 1% 1/16W MF 402
MIN_LINE_WIDTH=8 mil
MIN_NECK_WIDTH=8 mil
R4910 1K 1% 1/16W MF 402
PPVCORE_GPUFB
R4911 1K 1% 1/16W MF 402
PLACE VREF_VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN
R4912 1K 1% 1/16W MF 402
C4906 0.1UF 20% 16V CERM 402
C4907 10UF 20% 6.3V CERM 805
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil

PP1V8_GPU
NO STUFF
R4924 4.7K 5% 1/16W MF 402
R4907 4.7K 5% 1/16W MF 402
NO STUFF
R4908 4.7K 5% 1/16W MF 402
R4923 4.7K 5% 1/16W MF 402
GPU_MEMVMODE0
GPU_MEMVMODE1

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

	B7	MEMVMODE0	
	B6	MEMVMODE1	
	E8	TEST_YCLK	
	J6	TEST_MLCK	
	C8	MEMTEST	
	AC22	PLLTEST	NC

(PULL-UP to GPU_MEM_IO)
GPU_MEMTEST
R4904 45.3 1% 1/16W MF 402

	A10		
	C5		
	A3		
	G4		
	B2		
	U2		
	V4		
	AB2		
	AC4		
	B23		
	K2		
	A23		
	K1		
	B22		
	L2		
	A22		
	L1		

	P2		
	B18		
	P4		
	A19		
	R3		
	A18		
	R4		
	D19		
VSS	P1		
	G29		
	G27		
	B29		
	C20		
	C16		
	A15		
	C11		

	C19		
	D18		
	C10		
	B19		
	M15		
	N15		
	R15		
VSS	T15		
	T12		
	T13		
	T14		
	W16		
	V16		
	U16		
	T16		
	R16		
	R17		
	R18		
	R19		

	M2		
	R3		
	A21		
	B19		
	M15		
	N15		
	R15		
VSS	T15		
	T12		
	T13		
	T14		
	W16		
	V16		
	U16		
	T16		
	R16		
	R17		
	R18		
	R19		
	U6		
VDDCI	AE15		
	F18		
	P25		

	AC10	D+	GPU_THMDIODE_P
	AC11	D-	GPU_THMDIODE_N

PPVCORE_GPUFB

PPVCORE_GPU_VDDCI
VOLTAGE=1.2V
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil
PPVCORE_GPU
L4900 60-OHM-EMI SM
C4900 0.01UF 20% 16V CERM 402
C4902 10UF 20% 6.3V CERM 805
C4903 0.01UF 20% 16V CERM 402
C4901 0.01UF 20% 16V CERM 402
C4904 0.01UF 20% 16V CERM 402

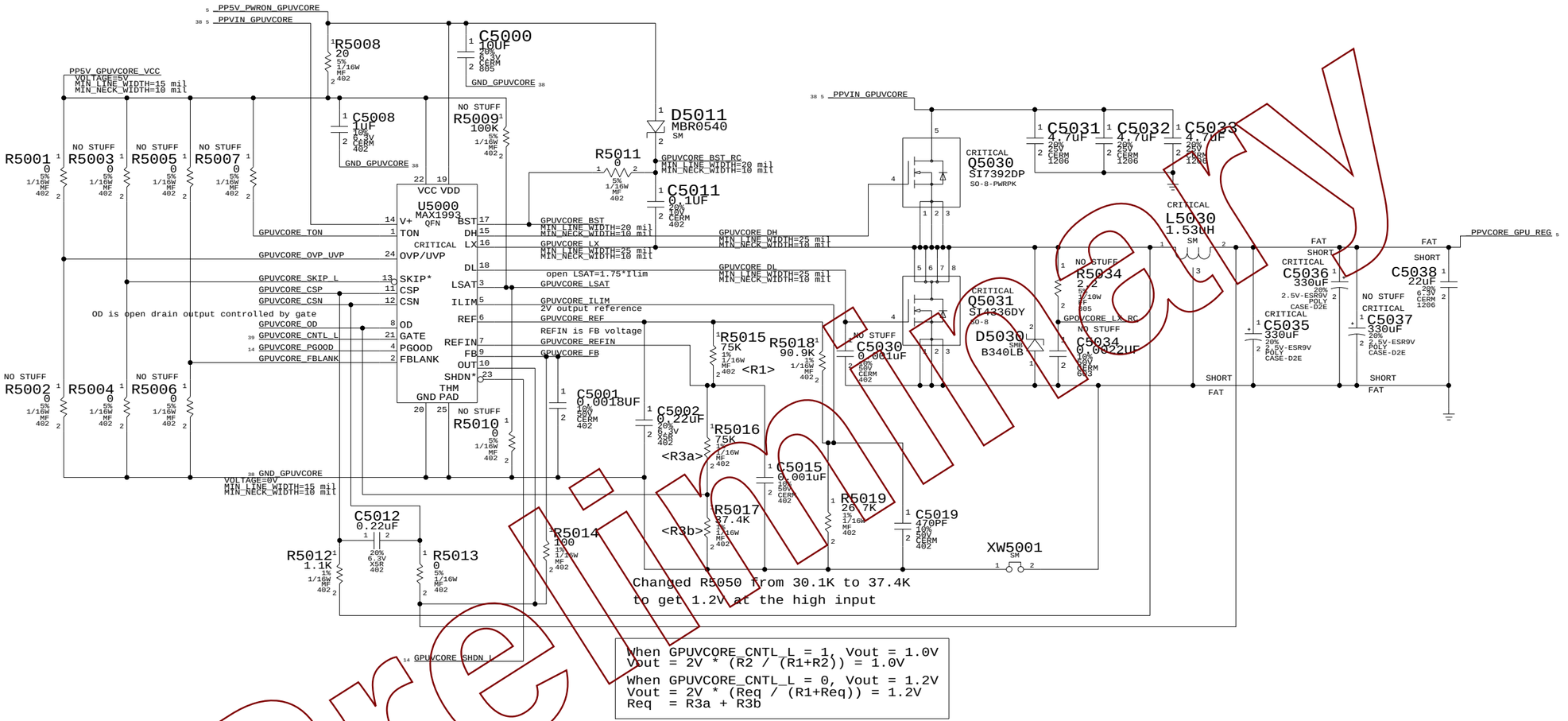
	B26		
	A26		
	B25		
	A25		
	C22		
	D21		
	C21		
	D20		
	C20		
	D22		
	C23		
	D23		
	A27		
	B27		
	H2		
	H1		
	J2		
	J1		
	K4		
	K3		
	L4		
	M3		
VSS	L3		
	M4		
	N2		
	N1		
	N4		
	N3		
	G30		
	G28		
	B30		
	D26		
	D16		
	B15		
	D11		
	B10		
	D9		
	B3		
	G3		
	E1		
	U1		
	V3		
	AB1		
	AC3		
	J30		
	J29		
	H30		
	H29		
	F30		
	F29		
	E30		
	E29		
	J28		
	J27		
	H28		
	H27		
	F28		
	F27		
	E28		
	E27		
	D30		
VSS	D29		
	C30		
	C29		
	A30		
	A29		
	A28		
	B28		
	D28		
	C28		
	D27		
	C27		
	D25		
	C25		
	D24		
	C24		
	D18		
	C18		
	D17		
	C17		
	D15		
	C15		
	D14		
	C14		
	B17		

	A17		
	B16		
	A16		
	B14		
	A14		
	B13		
	A13		
	D13		
	C13		
	D12		
	C12		
	D10		
	C10		
	D9		
	C9		
	B12		
	A12		
	B11		
	A11		
	B9		
	A9		
	B8		
	A8		
	C7		
	D7		
	C6		
	D6		
	C4		
	D4		
	C3		
	D3		
	A5		
	B5		
	A4		
	B4		
	A2		
	B2		
	A1		
	B1		
	E4		
	E3		
	F3		
	F4		
	H3		
	H4		
	J3		
	J4		
	C1		
	C2		
	D1		
	D2		
	F1		
	F2		
	G1		
	G2		
	R1		
	R2		
	T1		
	T2		
	V1		
	V2		
	W1		
	W2		
	T3		
	T4		
	U3		
	U4		
	W3		
	W4		
	Y3		
	Y4		
	Y1		
	Y2		
	AA1		
	AA2		
	AC1		
	AC2		
	AD1		
	AD2		
	AA3		
	AA4		
	AB3		
	AB4		
	AD3		
	AD4		
	AE3		
	AE4		

M11 AGP INTERFACE

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 49 OF 103	



GPU VCore Regulator

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE: NONE

SHT 50 OF 103

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
	LVDS	LVDS_L0	LVDS_L0P	6 39 42
	LVDS	LVDS_L0	LVDS_L0N	6 39 42
	LVDS	LVDS_L1	LVDS_L1P	6 39 42
	LVDS	LVDS_L1	LVDS_L1N	6 39 42
	LVDS	LVDS_L2	LVDS_L2P	6 39 42
	LVDS	LVDS_L2	LVDS_L2N	6 39 42
	LVDS	LVDS_LCLK	CLKLVDS_LP	6 39 42
	LVDS	LVDS_LCLK	CLKLVDS_LN	6 39 42
	LVDS	LVDS_U0	LVDS_U0P	6 39 42
	LVDS	LVDS_U0	LVDS_U0N	6 39 42
	LVDS	LVDS_U1	LVDS_U1P	6 39 42
	LVDS	LVDS_U1	LVDS_U1N	6 39 42
	LVDS	LVDS_U2	LVDS_U2P	6 39 42
	LVDS	LVDS_U2	LVDS_U2N	6 39 42
	LVDS	LVDS_UCLK	CLKLVDS_UP	6 39 42
	LVDS	LVDS_UCLK	CLKLVDS_UN	6 39 42
GPU_DVO_DATA	8 MIL SPACING		GPU_DVO0<0..19>	39 41
GPU_DVO_DATA20	8 MIL SPACING		GPU_DVO0<20>	39 41
GPU_DVO_DATA	8 MIL SPACING		GPU_DVO0<21..23>	39 41
GPU_DVO_DATA	8 MIL SPACING		GPU_DVO_HSYNC	39 41
GPU_DVO_CTL	8 MIL SPACING		GPU_DVO_VSYNC	39 41
GPU_DVO_CTL	8 MIL SPACING		GPU_DVO_DE	39 41
GPU_DVO_CTL	8 MIL SPACING		GPU_DVO_CLKP	39 41

Page Notes

Power aliases required by this page:
_PP1V5_GPU_AGP, _PP3V3_GPU, PPVCORE_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: LVDS

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils
Secondary Max Sep:	100 mils
Secondary Length:	250 mils

NOTE: Target differential impedance for LVDS data pairs is 100 ohms.

GPU VCORE - 1.2V

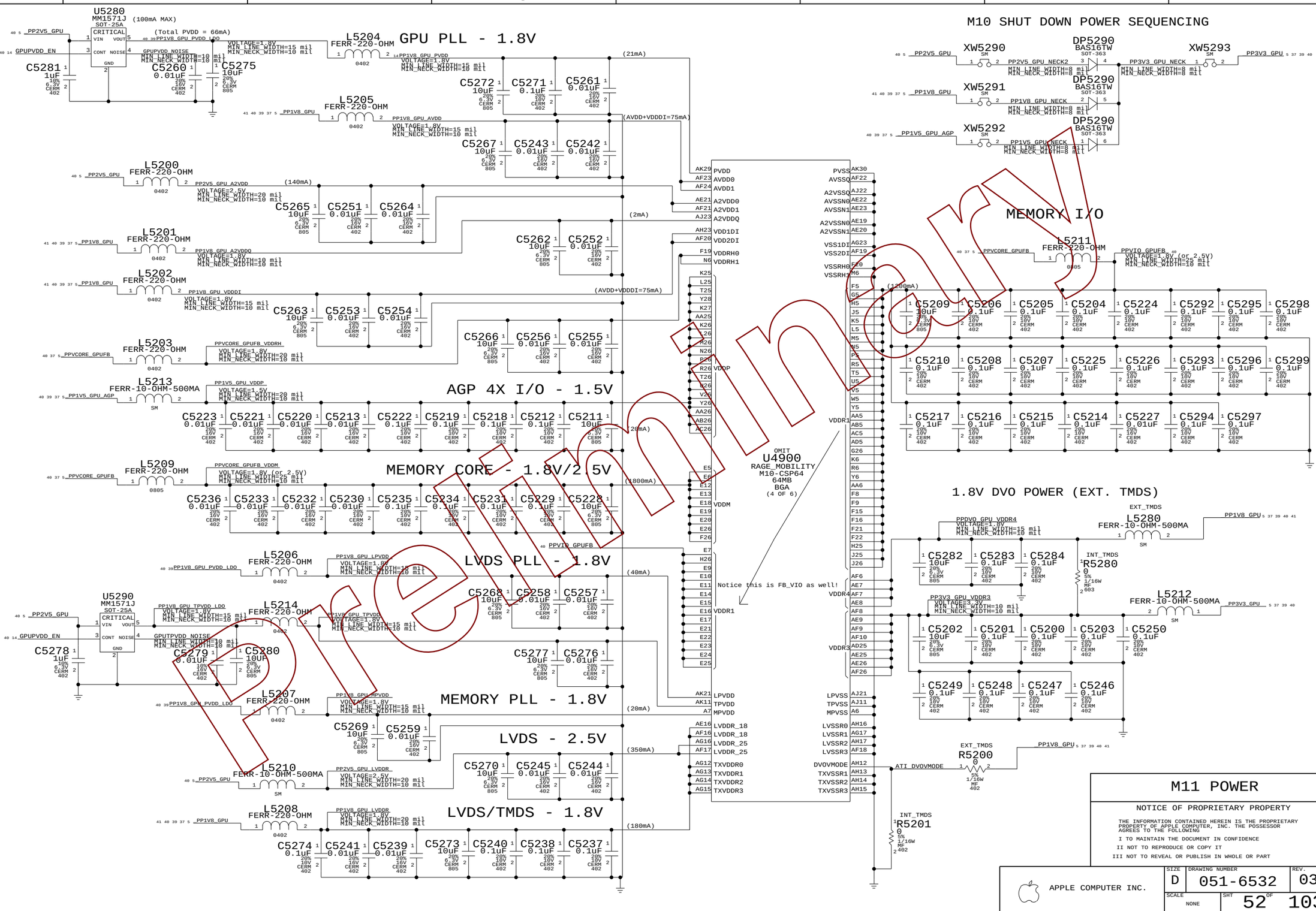
(PUT ALL CAPs BELOW ATI ASIC)

M10 Power Shut down Sequencing

M11 CORE PWR/LVDS/TMDS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 51 OF 103	


M10 SHUT DOWN POWER SEQUENCING
GPU PLL - 1.8V
AGP 4X I/O - 1.5V
MEMORY CORE - 1.8V/2.5V
LVDS PLL - 1.8V
MEMORY PLL - 1.8V
LVDS - 2.5V
LVDS/TMDS - 1.8V
MEMORY I/O
1.8V DVO POWER (EXT. TMDS)
U4900
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(4 OF 6)
Notice this is FB_VIO as well!
M11 POWER
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6532
REV. 03
SCALE NONE
SHT 52 OF 103

Page Notes

Power aliases required by this page:
(None)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: TMDS

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils
Secondary Max Sep:	100 mils
Secondary Length:	250 mils

NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ATI TMDS

SILICON IMAGE TMDS

INTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

EXTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

APPLE COMPUTER INC.

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EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL5910 CRITICAL LCFILTER SM-220MHZ — GPU_B → VGA_B
FL5911 CRITICAL LCFILTER SM-220MHZ — GPU_G → VGA_G
FL5912 CRITICAL LCFILTER SM-220MHZ — GPU_R → VGA_R
C5910 3.3PF 0.25% 50V CERM 402
C5911 3.3PF 0.25% 50V CERM 402
C5912 3.3PF 0.25% 50V CERM 402

VGA VSYNC BUFFERS

PP3V3_PWRON
CRITICAL U5913 74AHC1G32 SM
GPU_HSYNC → R5913 33 5% 1/16W MF 402 → VGA_HSYNC
CRITICAL U5914 74AHC1G32 SM
GPU_VSYNC → R5914 33 5% 1/16W MF 402 → VGA_VSYNC

TMDS FILTERING PLACE CLOSE TO CONNECTOR

CRITICAL L5916 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DN<0> / TMDS_DP<0>
CRITICAL L5917 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DN<1> / TMDS_DP<1>
CRITICAL L5918 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DN<2> / TMDS_DP<2>
CRITICAL L5919 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DN<3> / TMDS_DP<3>
CRITICAL L5920 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DN<4> / TMDS_DP<4>
CRITICAL L5921 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DN<5> / TMDS_DP<5>

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

PP5V_RUN → F5900 0.5AMP-13.2V SM → PP5V_RUN_DDC_F (MIN_LINE_WIDTH=10 MIL, MIN_NECK_WIDTH=10 MIL)
L5900 400-OHM-EMI SM-1 — Isolation required for DVI power switch
PP5V_RUN_DDC → D5900 MBR0530 SM
DDC_CLK_ISO (MIN_LINE_WIDTH=10 MIL, MIN_NECK_WIDTH=10 MIL)
R5902 4.7K 5% 1/16W MF 402
R5903 4.7K 5% 1/16W MF 402
R5904 100 5% 1/16W MF 402
R5905 100 5% 1/16W MF 402
R5906 100 5% 1/16W MF 402
C5904 100pF 5% 50V CERM 402
C5905 100pF 5% 50V CERM 402
C5906 100pF 5% 50V CERM 402
C5900 0.01UF 20% 50V CERM 603

J5900 CRITICAL QH1112 F-RT-TH 36-pin

TMDS_CONN_DN<0>	TMDS_CONN_DN<2>
TMDS_CONN_DP<0>	TMDS_CONN_DP<2>
TMDS_CONN_DN<5>	TMDS_CONN_DN<4>
TMDS_CONN_DP<5>	TMDS_CONN_DP<4>
TMDS_CONN_CLKP	TMDS_CONN_DN<1>
TMDS_CONN_CLKN	TMDS_CONN_DP<1>
	TMDS_CONN_DN<3>
	TMDS_CONN_DP<3>
	DVI_DDC_CLK_UF (+5V_DDC_SLEEP)
	DVI_DDC_DATA_UF
	VGA_VSYNC
	DVI_HPD_UF
VGA_B	VGA_R
VGA_HSYNC	VGA_G
GND_CHASSIS_DVI_TOP	
GND_CHASSIS_DVI_BOTTOM	

R5900 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R5901 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B

3V LEVEL SHIFTERS

PP3V3_RUN
Q5907 2N7002DW SOT-363 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
Q5907 2N7002DW SOT-363 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
Q5909 2N7002DW SOT-363 — DVI_HPD → GPU_HPD
R5907 10K 5% 1/16W MF 402
R5908 10K 5% 1/16W MF 402
R5909 100K 5% 1/16W MF 402
Q5909 shares with ALS sensor to save space
NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from GPU DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. Once host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q5933 TP0610 SM — DVI_DDC_CLK_UF → DVI_DDC_CLK
R5933 680 5% 1/16W MF 402 — DVI_TURN_ON → DVI_TRUN_ON_ILIM
R5935 10K 5% 1/16W MF 402 — DVI_TURN_ON_BASE
Q5935 2N3904 SM — SYS_POWER_BUTTON_L
R5934 330 5% 1/10W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
PP5V_RUN_DDC

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY GPU's GPIO.

R5920 68.1K 1% 1/16W MF 402
C5920 0.1UF 20% 10V CERM 402
U5920 LMC7211 SM — CRITICAL
HPD_4V_REF
R5922 10K 1% 1/16W MF 402 — DVI_HPD_UF
R5923 10K 1% 1/16W MF 402
R5921 100K 1% 1/16W MF 402 — DVI_HPD_DIV
HPD_PWR_SW
Q5925 2N7002DW SOT-363 — HPD_ON
Q5926 TP0610 SM
R5928 330 5% 1/16W MF 402
R5930 20K 5% 1/16W MF 402 — HPD_BASE
Q5930 2N3904 SM — HPD_ON_RC
PPBUS_ALL_A
COMP_ENABLE
COMP_DISABLE
R5926 100K 5% 1/16W MF 402
R5927 100K 5% 1/16W MF 402
C5929 47UF 20% 6.3V CERM 1210
R5929 68K 5% 1/16W MF 402
Q5925 2N7002DW SOT-363 — NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
HPD_PWR_SNS_EN
R5925 100K 5% 1/16W MF 402

LCD INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups
C5970 0.001uF 20% 50V CERM 402 — GND_CHASSIS_LVDS
CRITICAL J5970 G-501973 F-RT-SM 34-pin
PP3V3_RUN
R5972 100K 5% 1/16W MF 402
R5973 100K 5% 1/16W MF 402
PP3V3_LCD (MIN_LINE_WIDTH=20 MIL, MIN_NECK_WIDTH=10 MIL) (LVDS DDC POWER)
LVDS_DDC_CLK
LVDS_DDC_DATA
NO STUFF
C5972 0.001uF 20% 50V CERM 402
C5973 0.001uF 20% 50V CERM 402
GND_CHASSIS_LVDS

NC	
LVDS_L0N	
LVDS_L0P	
LVDS_L1N	
LVDS_L1P	
LVDS_L2N	
LVDS_L2P	
CLKLVDS_LN	
CLKLVDS_LP	
LVDS_U0N	
LVDS_U0P	
LVDS_U1N	
LVDS_U1P	
LVDS_U2N	
LVDS_U2P	
CLKLVDS_UN	
CLKLVDS_UP	

INVERTER INTERFACE

PPBUS_INV → L5980 FERR-1K-OHM-EMI SM (PPBUS_INVERTER MIN_LINE_WIDTH=20 MIL, MIN_NECK_WIDTH=10 MIL)
PP5V_PWRON
Q5984 FDG6324L SC70-6
R5984 100K 5% 1/16W MF 402
FP_PWR_EN_L
PP5V_INVERTER_F (MIN_LINE_WIDTH=10 MIL, MIN_NECK_WIDTH=10 MIL)
L5981 400-OHM-EMI SM-1
C5984 10UF 20% 6.3V CERM 805
PP5V_INVERTER
Q5984 FDG6324L SC70-6
FP_PWR_EN
L5982 400-OHM-EMI SM-1
BRIGHT_PWM
PP3V3_ALL
C5983 0.1UF 20% 10V CERM 402
INV_ON_PWM
CRITICAL U5983 74AHC1G32 SM
BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
C5980 0.001UF 20% 50V CERM 402
C5981 0.001UF 20% 50V CERM 402
C5982 0.001UF 20% 50V CERM 402
CRITICAL J5980 SM-2MT
GND_CHASSIS_INV

S-VIDEO/COMP OUT INTERFACE

XW5960 SM — GPU_TV_GND1 → L5960 FERR-10-OHM-500MA SM (MIN_LINE_WIDTH=15 MIL, MIN_NECK_WIDTH=10 MIL) → TV_GND1
C5960 0.01UF 20% 50V CERM 603
Place GND shorts at graphics controller
L5962 3.3UH 0603 — GPU_Y → TV_C
C5967 560PF 10% 50V CERM 402
C5962 560PF 10% 50V CERM 402
L5963 3.3UH 0603 — GPU_C → TV_Y
C5968 560PF 10% 50V CERM 402
C5963 560PF 10% 50V CERM 402
CRITICAL J5960 MINIDIN RT-TH MH1177
L5964 3.3UH 0603 — GPU_COMP → TV_COMP
C5969 560PF 10% 50V CERM 402
C5964 560PF 10% 50V CERM 402
XW5961 SM — GPU_TV_GND2 → L5961 FERR-10-OHM-500MA SM (MIN_LINE_WIDTH=15 MIL, MIN_NECK_WIDTH=10 MIL) → TV_GND2
C5961 0.01UF 20% 50V CERM 603
Place GND shorts at graphics controller
GND_CHASSIS_SVIDEO

LCD POWER SWITCH

PP3V3_PWRON
R5977 100K 5% 1/16W MF 402
C5976 0.0022uF 10% 50V CERM 402
R5976 100K 5% 1/16W MF 402 — LCD_PWREN_L
LCD_DIGON_L
Q5977 2N7002 SM — FP_PWR_EN
PP3V3_LCD_FET (MIN_LINE_WIDTH=20 MIL, MIN_NECK_WIDTH=10 MIL)
L5975 FERR-250-OHM SM
Q5975 SI3443DV TSOP
C5975 0.001uF 20% 50V CERM 402
C5971 0.001uF 20% 50V CERM 402
R5999 0 5% 1/16W MF 402
C5999 0.01uF 20% 50V CERM 603
GND_CHASSIS_INV

VIDEO CONNECTORS

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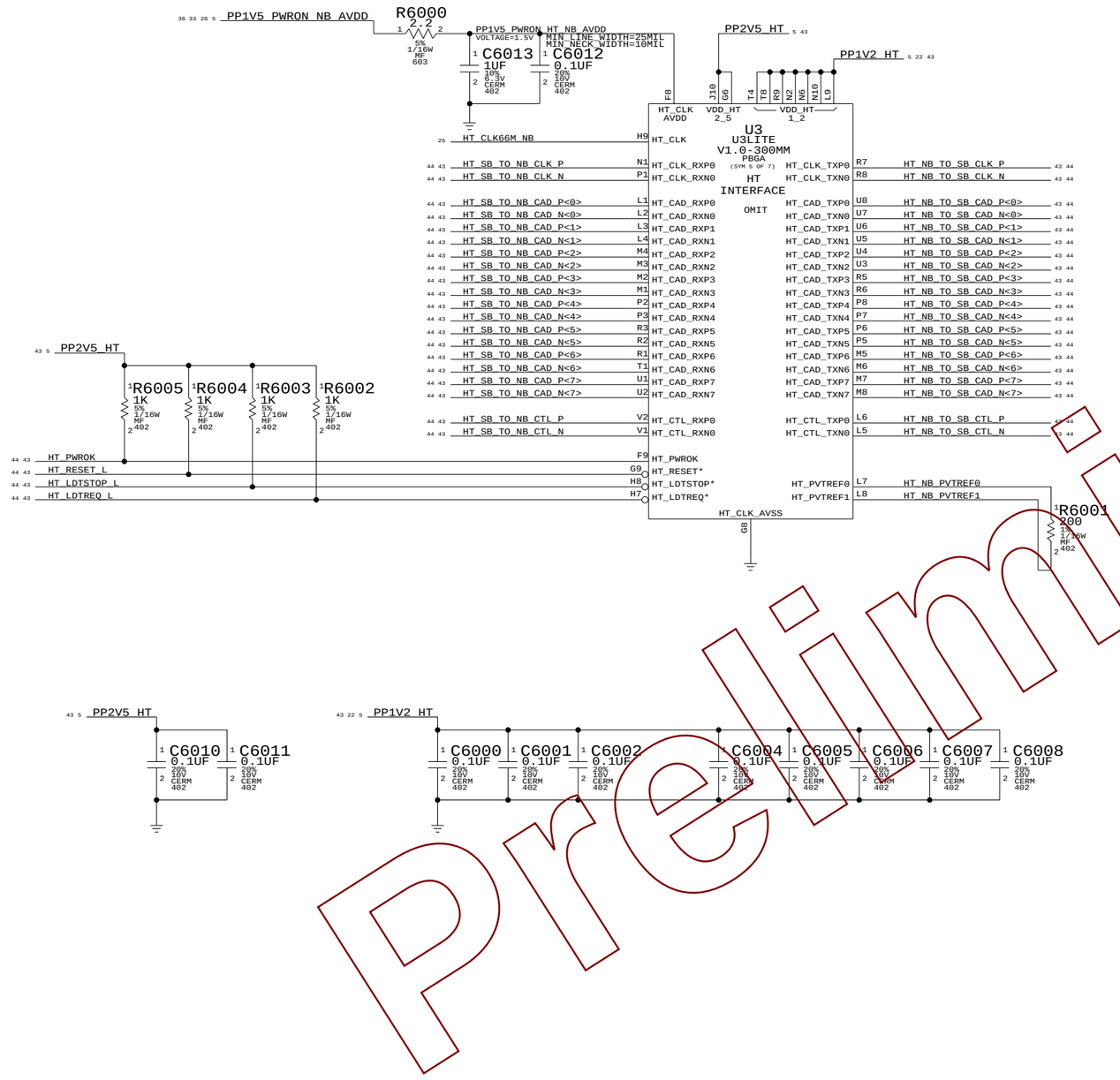

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
HT_NB_TO_SB_CLK_P	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CLK	146
HT_NB_TO_SB_CLK_N	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CLK	147
HT_NB_TO_SB_CTL_P	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CTL	183
HT_NB_TO_SB_CTL_N	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CTL	182
HT_NB_TO_SB_CAD_P<0>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	151
HT_NB_TO_SB_CAD_N<0>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	150
HT_NB_TO_SB_CAD_P<1>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	152
HT_NB_TO_SB_CAD_N<1>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	153
HT_NB_TO_SB_CAD_P<2>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	154
HT_NB_TO_SB_CAD_N<2>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	155
HT_NB_TO_SB_CAD_P<3>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	156
HT_NB_TO_SB_CAD_N<3>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	157
HT_NB_TO_SB_CAD_P<4>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	158
HT_NB_TO_SB_CAD_N<4>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	159
HT_NB_TO_SB_CAD_P<5>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	160
HT_NB_TO_SB_CAD_N<5>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	161
HT_NB_TO_SB_CAD_P<6>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	162
HT_NB_TO_SB_CAD_N<6>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	163
HT_NB_TO_SB_CAD_P<7>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	164
HT_NB_TO_SB_CAD_N<7>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	165
HT_SB_TO_NB_CLK_P	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CLK	148
HT_SB_TO_NB_CLK_N	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CLK	149
HT_SB_TO_NB_CTL_P	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CTL	184
HT_SB_TO_NB_CTL_N	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CTL	185
HT_SB_TO_NB_CAD_P<0>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	166
HT_SB_TO_NB_CAD_N<0>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	167
HT_SB_TO_NB_CAD_P<1>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	168
HT_SB_TO_NB_CAD_N<1>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	169
HT_SB_TO_NB_CAD_P<2>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	170
HT_SB_TO_NB_CAD_N<2>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	171
HT_SB_TO_NB_CAD_P<3>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	172
HT_SB_TO_NB_CAD_N<3>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	173
HT_SB_TO_NB_CAD_P<4>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	174
HT_SB_TO_NB_CAD_N<4>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	175
HT_SB_TO_NB_CAD_P<5>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	176
HT_SB_TO_NB_CAD_N<5>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	177
HT_SB_TO_NB_CAD_P<6>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	178
HT_SB_TO_NB_CAD_N<6>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	179
HT_SB_TO_NB_CAD_P<7>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	180
HT_SB_TO_NB_CAD_N<7>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	181
HT_PWROK	HT_PWROK	HT_2V5		186
HT_RESET_L	HT_CTL	HT_2V5		187
HT_LDTSTOP_L	HT_CTL	HT_2V5		188
HT_LDTREQ_L	HT_CTL	HT_2V5		189

HT_1V2

5 MIL SPACING FOR DIFF PAIR
10 MIL SPACING TO ANYTHING ELSE

HT_2V5

4 MIL SPACING IN GROUP
8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERENCE DOES NOT NEED TO BE SPECIFIED
MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH

MASTER: GILA

U3LITE HT

APPLE COMPUTER INC.

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	15 MIL SPACING	

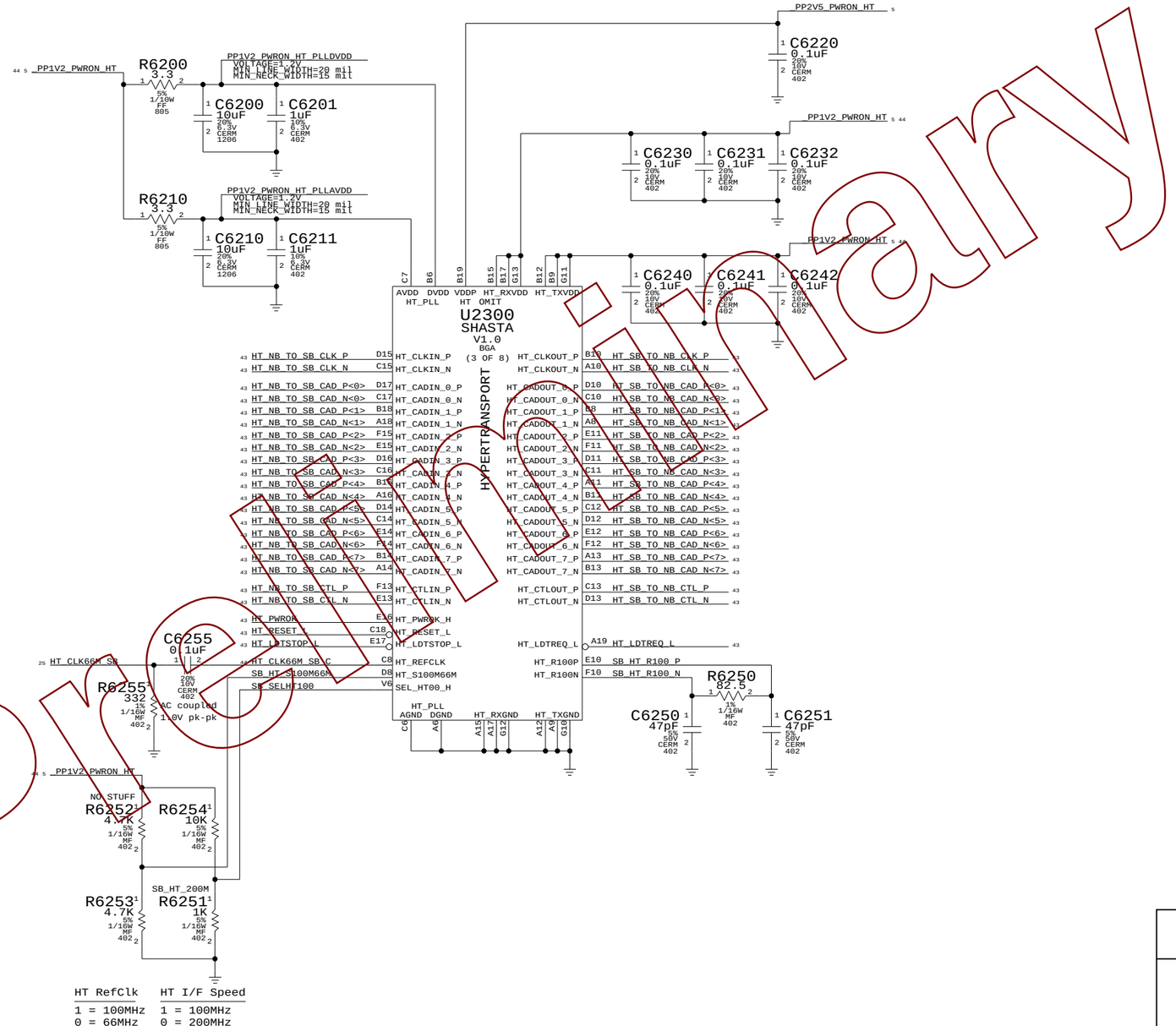
HT_CLK66M_SB_C 44

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_HT
- _PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.



Master: Fizzy

Shasta HyperTransport

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:06:27 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_AD		PCI_AD<31..28> 6 46 47 48 49 62
PCI_AD27		PCI_AD<27> 6 46 47 48 49 62
PCI_AD		PCI_AD<26..24> 6 46 47 48 49 62
PCI_AD23		PCI_AD<23> 6 47 48 49 62
PCI_AD22		PCI_AD<22> 6 47 48 49 62
PCI_AD21		PCI_AD<21> 6 47 48 49 62
PCI_AD20		PCI_AD<20> 6 46 47 48 49 62
PCI_AD		PCI_AD<19..18> 6 46 47 48 49 62
PCI_AD17		PCI_AD<17> 6 46 47 48 49 62
PCI_AD		PCI_AD<16..0> 6 46 47 48 49 62
PCI		PCI_CBE_L<3..0> 6 47 48 49 62
PCI		PCI_PAR 6 47 48 49 62
PCI_CTL		PCI_DEVSEL_L 6 45 47 48 49 62
PCI_CTL		PCI_FRAME_L 6 45 47 48 49 62
PCI_CTL		PCI_IRDY_L 6 45 47 48 49 62
PCI_CTL		PCI_TRDY_L 6 45 47 48 49 62
PCI_CTL		PCI_STOP_L 6 45 47 48 49 62

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_SB_PCI (can be _PP3V3_PCI)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

5 _PP3V3_SB_PCI

NO_STUFF C7410 10uF 20% 6.3V CERM 805
C7400 0.1uF 20% 10V CERM 402
C7401 0.1uF 20% 10V CERM 402
C7402 0.1uF 20% 10V CERM 402
C7403 0.1uF 20% 10V CERM 402
C7404 0.1uF 20% 10V CERM 402

NO_STUFF C7411 10uF 20% 6.3V CERM 805
C7405 0.1uF 20% 10V CERM 402
C7406 0.1uF 20% 10V CERM 402
C7407 0.1uF 20% 10V CERM 402
C7408 0.1uF 20% 10V CERM 402
C7409 0.1uF 20% 10V CERM 402

PP2V5_PWRON_SB 5 6 21 23 56

C7420 0.1uF 20% 10V CERM 402
C7421 0.1uF 20% 10V CERM 402
C7422 0.1uF 20% 10V CERM 402
C7423 0.1uF 20% 10V CERM 402

U2300 SHASTA V1.0 BGA (1 OF 8)

VDDOPC: AA22, B22, E21, H16, J21, M16, N21, R20, U21, V19
PCIVDDP: B20, J18, N20, U20
OMIT

25 PCI_CLK66M_SB_INT	AB9	PCIBR_CLK_H	
25 5 PCI_CLK33M_SB_EXT	U19	PCIICLK_H	
"Slot A" - AD17			
47 46 6 PCI_SLOTA_REQ_L	AB18	PCI1REQ_0_L	
47 48 PCI_SLOTA_GNT_L	AA18	PCI1GNT_0_L	
"Slot G" - AD27			
48 45 PCI_SLOTG_REQ_L	AB20	PCI1REQ_1_L	
48 45 PCI_SLOTG_GNT_L	AB19	PCI1GNT_1_L	
"Slot D" - AD26			
45 PCI_SLOTD_REQ_L	V17	PCI1REQ_2_L	
45 PCI_SLOTD_GNT_L	V18	PCI1GNT_2_L	
47 46 6 ROM_CS_L	AB8	ROMCS_L	
47 46 6 ROM_OE_L	AA9	ROMOE_L	
47 46 6 ROM_WE_L	Y10	ROMRW_L	

PCI1AD_0_H	L18	PCI_SB_AD<0>	62
PCI1AD_1_H	K19	PCI_SB_AD<1>	62
PCI1AD_2_H	L22	PCI_SB_AD<2>	62
PCI1AD_3_H	M22	PCI_SB_AD<3>	62
PCI1AD_4_H	M18	PCI_SB_AD<4>	62
PCI1AD_5_H	L20	PCI_SB_AD<5>	62
PCI1AD_6_H	M21	PCI_SB_AD<6>	62
PCI1AD_7_H	N16	PCI_SB_AD<7>	62
PCI1AD_8_H	M20	PCI_SB_AD<8>	62
PCI1AD_9_H	P22	PCI_SB_AD<9>	62
PCI1AD_10_H	M17	PCI_SB_AD<10>	62
PCI1AD_11_H	N18	PCI_SB_AD<11>	62
PCI1AD_12_H	M19	PCI_SB_AD<12>	62
PCI1AD_13_H	N19	PCI_SB_AD<13>	62
PCI1AD_14_H	P21	PCI_SB_AD<14>	62
PCI1AD_15_H	R22	PCI_SB_AD<15>	62
PCI1AD_16_H	P20	PCI_SB_AD<16>	62
PCI1AD_17_H	V21	PCI_SB_AD<17>	62
PCI1AD_18_H	P18	PCI_SB_AD<18>	62
PCI1AD_19_H	T20	PCI_SB_AD<19>	62
PCI1AD_20_H	R16	PCI_SB_AD<20>	62
PCI1AD_21_H	R17	PCI_SB_AD<21>	62
PCI1AD_22_H	W21	PCI_SB_AD<22>	62
PCI1AD_23_H	Y22	PCI_SB_AD<23>	62
PCI1AD_24_H	R18	PCI_SB_AD<24>	62
PCI1AD_25_H	T19	PCI_SB_AD<25>	62
PCI1AD_26_H	T18	PCI_SB_AD<26>	62
PCI1AD_27_H	Y21	PCI_SB_AD<27>	48 62
PCI1AD_28_H	W20	PCI_SB_AD<28>	62
PCI1AD_29_H	T16	PCI_SB_AD<29>	62
PCI1AD_30_H	AA21	PCI_SB_AD<30>	62
PCI1AD_31_H	T17	PCI_SB_AD<31>	62
PCI1C_BE_0_L	L19	PCI_SB_CBE_L<0>	62
PCI1C_BE_1_L	P16	PCI_SB_CBE_L<1>	62
PCI1C_BE_2_L	V22	PCI_SB_CBE_L<2>	62
PCI1C_BE_3_L	V20	PCI_SB_CBE_L<3>	62
PCI1DEVSEL_L	T22	PCI_SB_DEVSEL_L	62
PCI1FRAME_L	T21	PCI_SB_FRAME_L	62
PCI1IRDY_L	R21	PCI_SB_IRDY_L	62
PCI1TRDY_L	P19	PCI_SB_TRDY_L	62
PCI1STOP_L	P17	PCI_SB_STOP_L	62
PCI1PAR_H	N17	PCI_SB_PAR	62
PCI1RST_L	U18	SB_PCI_RESET_L	

PP3V3_PCI 5 23 45 46 47 48 49

RP7400 4.7K 5% 1/16W SM1: PCI_SLOTA_REQ_L 6 45 47
RP7400 4.7K 5% 1/16W SM1: PCI_SLOTA_GNT_L 6 45 47
RP7400 4.7K 5% 1/16W SM1: PCI_SLOTG_REQ_L 45 48
RP7400 4.7K 5% 1/16W SM1: PCI_SLOTG_GNT_L 45 48
RP7401 4.7K 5% 1/16W SM1: PCI_SLOTD_REQ_L 45
RP7401 4.7K 5% 1/16W SM1: PCI_SLOTD_GNT_L 45

PP3V3_PWRON_SB 5 18 21 23

R7455 4.7K 5% 1/16W MF 402
C7450 0.1uF 20% 10V CERM 402
R7450 4.7K 5% 1/16W MF 402

U7450 MC74VHC1G08 SOT23-5
PCI_RESET_L 5 46 47 48

48 23 22 5 SYS_WARM_RESET_L

Shasta drives PCI RESET, but its output may not be valid during power-up, so it is ANDed with a reset from the SMU.

49 48 47 46 45 23 5 PP3V3_PCI

RP7402 4.7K 5% 1/16W SM1: PCI_DEVSEL_L 62 49 48 47 45 6
RP7402 4.7K 5% 1/16W SM1: PCI_FRAME_L 62 49 48 47 45 6
RP7402 4.7K 5% 1/16W SM1: PCI_IRDY_L 62 49 48 47 45 6
RP7402 4.7K 5% 1/16W SM1: PCI_TRDY_L 62 49 48 47 45 6
RP7401 4.7K 5% 1/16W SM1: PCI_STOP_L 62 49 48 47 45 6

Master: Link

Shasta PCI Interface

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 74 OF 103	

DRAWING
TITLE=LINK
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:06:40 2004

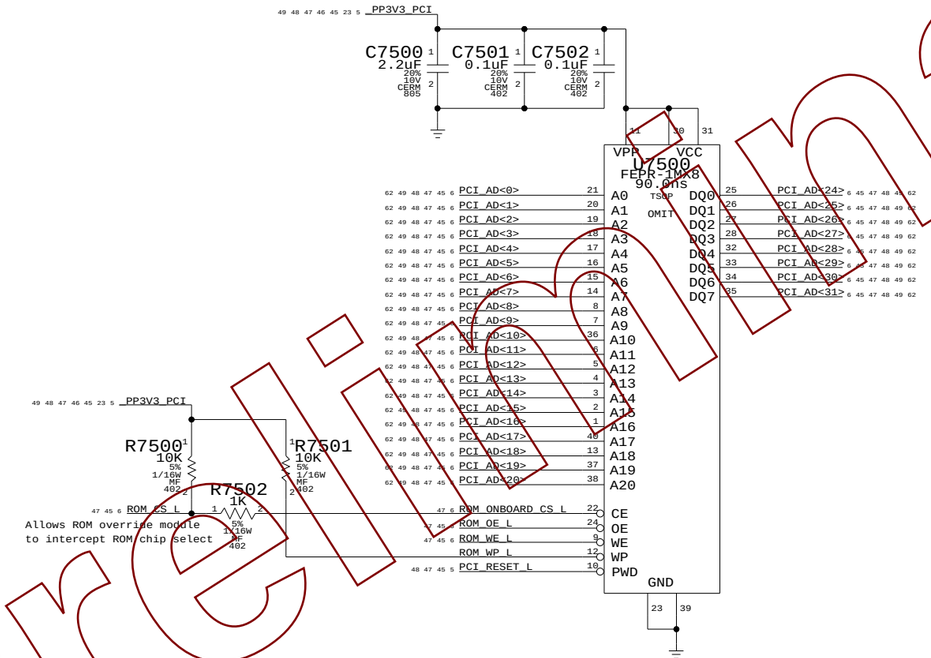
Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



Master: Fizzy

BootROM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	75	103

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:06:47 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

_PCI_CLK33M_AIRPORT 5 47

Page Notes

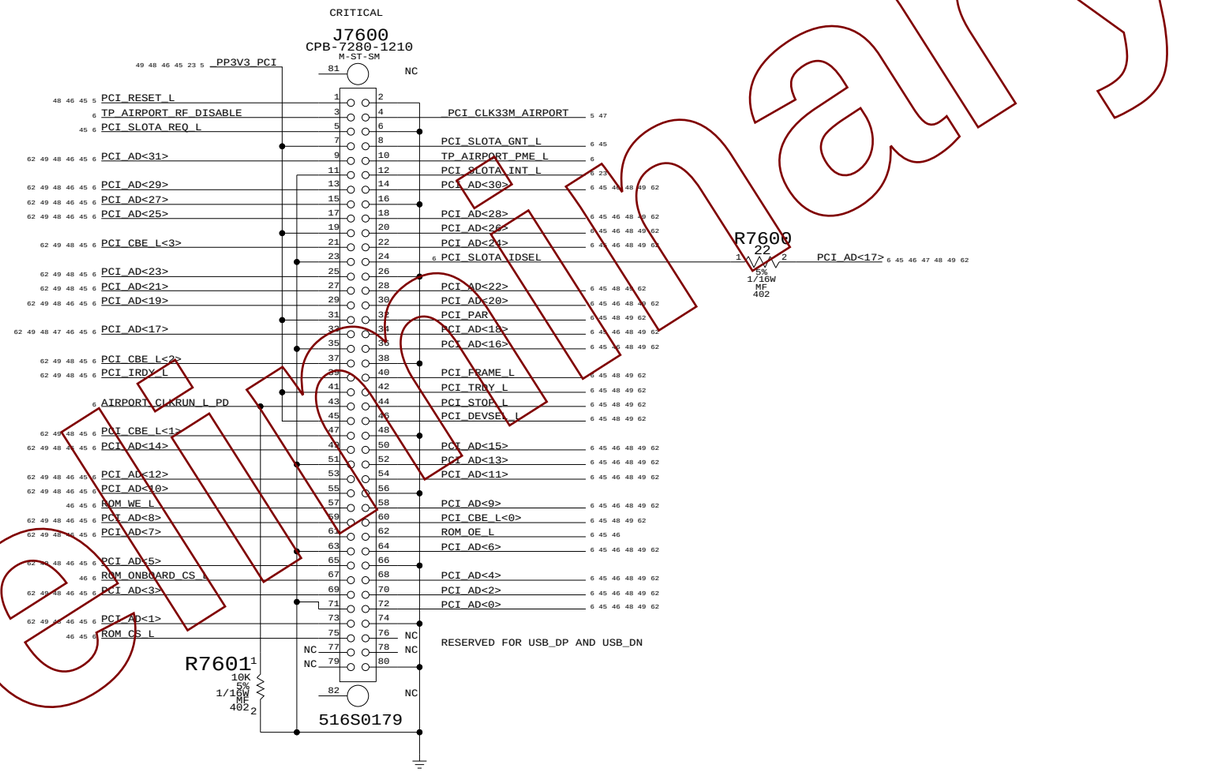
Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.



_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:06:53 2004

AirPort Extreme

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 76 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	

_PCI_CLK33M_USB2 5 48

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.

5 _PPVIO_PCI_USB2

C7703 0.1uF 20% 10V CERM 402

VDD_PCI

CRITICAL
U7700
NEC_uPD720101_USB2
FBGA

PCI_AD<0>	M5	AD0
PCI_AD<1>	P5	AD1
PCI_AD<2>	N5	AD2
PCI_AD<3>	P4	AD3
PCI_AD<4>	N4	AD4
PCI_AD<5>	M3	AD5
PCI_AD<6>	N3	AD6
PCI_AD<7>	M1	AD7
PCI_AD<8>	L2	AD8
PCI_AD<9>	L1	AD9
PCI_AD<10>	K2	AD10
PCI_AD<11>	L3	AD11
PCI_AD<12>	K1	AD12
PCI_AD<13>	K3	AD13
PCI_AD<14>	J2	AD14
PCI_AD<15>	J1	AD15
PCI_AD<16>	F2	AD16
PCI_AD<17>	E3	AD17
PCI_AD<18>	E1	AD18
PCI_AD<19>	D3	AD19
PCI_AD<20>	D1	AD20
PCI_AD<21>	D2	AD21
PCI_AD<22>	C2	AD22
PCI_AD<23>	C1	AD23
PCI_AD<24>	B4	AD24
PCI_AD<25>	A4	AD25
PCI_AD<26>	B5	AD26
(PCI_AD<27>)	C4	AD27
PCI_AD<28>	A5	AD28
PCI_AD<29>	C5	AD29
PCI_AD<30>	B6	AD30
PCI_AD<31>	A6	AD31
PCI_CBE_L<0>	M2	CBE0
PCI_CBE_L<1>	J3	CBE1
PCI_CBE_L<2>	F1	CBE2
PCI_CBE_L<3>	C3	CBE3
PCI_PAR	J4	PAR
PCI_FRAME_L	F3	FRAME
PCI_IRDY_L	F4	IRDY
PCI_TRDY_L	G1	TRDY
PCI_STOP_L	G3	STOP
PCI_SLOTG_IDSEL	B3	IDSEL
PCI_DEVSEL_L	G4	DEVSEL
PCI_SLOTG_REQ_L	C6	REQ
PCI_SLOTG_GNT_L	D6	GNT
NEC_PERR_L_PU	H2	PERR
NEC_SERR_L_PU	H1	SERR OD
NEC_INTA_L	C7	INTA OD
NEC_INTB_L	B7	INTB OD
NEC_INTC_L	A7	INTC OD
48 5 _PCI_CLK33M_USB2	A8	PCLK
NEC_VBBRST_L	B8	VBBRST(CHIP RESET)
NEC_CRUN_L_PD	N6	CRUN
NEC_PME_L	D9	PME OD
NEC_VCCRST_L	C9	VCCRST(PCI RESET)
TP_NEC_SMI_L	L6	SMI OD
NEC_LEGC_PD	L7	LEGC

IPD NTEST1	M8	TP_NEC_NTEST1
IPD SMC	M7	TP_NEC_SMC
IPD TEB	N7	TP_NEC_TEB
IPD AMC	P7	TP_NEC_AMC
IPD TEST	L8	TP_NEC_TEST
NANDTEST	M10	TP_NEC_NANDTEST
SRCLK	M9	TP_NEC_SRCLK
SRDTA	N9	TP_NEC_SRDATA
IPD SRMOD	P9	TP_NEC_SRMOD

62 45 PCI_SB_AD<27>

R7714 22 5% 1/16W MF 402

49 47 46 45 23 5 _PP3V3_PCI

R7716 10K 5% 1/16W MF 402

R7713 10K 5% 1/16W MF 402

23 PCI_SLOTG_INT_L

RP7703 47 5% 1/16W SM1

RP7703 47 5% 1/16W SM1

RP7703 47 5% 1/16W SM1

RP7702 47 5% 1/16W SM1

45 23 22 5 SYS_WARM_RESET_L

RP7702 47 5% 1/16W SM1

23 13 SYS_PME_L

RP7702 47 5% 1/16W SM1

47 46 45 5 PCI_RESET_L

RP7702 & RP7703 required to facilitate NAND-tree testing

R7715 4.7K 5% 1/16W MF 402

RP7703 47 5% 1/16W SM1

Master: Fizzy

USB 2.0 PCI Interface

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	77	103

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:00 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_CBUS	CLOCKS	

PCI_CLK33M_CBUS 5 49

Page Notes

Power aliases required by this page:
- _PP5V_CBUS
- _PP3V3_CBUS
- _PP3V3_PCI
- _PP2V5_PCI
- _PPVIO_PCI (to _PP5V_PCI or _PP3V3_PCI)

NOTE: All 4 rails MUST implement the same power state (PWRON or RUN). For PWRON must alias _PCI_CBUS_RESET_L to SYS_WARM_RESET_L. For RUN must alias to PCI_RESET_L instead.

Signal aliases required by this page:
- _PCI_CBUS_RESET_L (see note above)
- _PCI_CLK33M_CBUS (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD21 (Slot "E") - CardBus (0x104C/0xAC56)

Power Sequencing:

Power Up	Power Down
1. Assert RESET	1. Assert RESET
2. _PP3V3_PCI	2. _PPVIO_PCI
3. _PPVIO_PCI	3. _PP3V3_PCI

(_PPVIO_PCI can be same as _PP3V3_PCI)

NOTE: This CardBus implementation does not provide PME# or 12V Vpp support.

PP3V3_PCI 5 23 45 46 47 48 49

R7802 10K 5% 1/16W MF 402 — CBUS_VR_EN_L_PU 49
R7803 10K 5% 1/16W MF 402 — CBUS_PERR_L_PU 49
R7804 10K 5% 1/16W MF 402 — CBUS_SERR_L_PU 49
R7805 10K 5% 1/16W MF 402 — CBUS_SUSPEND_L_PU 49

PP3V3_PCI 49 48 47 46 45 23 5

C7800 10uF 20% 6.3V CERM 805
C7801 0.22uF 20% 6.3V X5R 402
C7802 0.22uF 20% 6.3V X5R 402
C7803 0.22uF 20% 6.3V X5R 402
C7804 0.22uF 20% 6.3V X5R 402
C7805 0.22uF 20% 6.3V X5R 402
C7806 0.22uF 20% 6.3V X5R 402

VCC: A7 C13 D5 E1 M1 N7 N11

PP2V5_PCI 5

C7807 0.22uF 20% 6.3V X5R 402

CBUS_VR_EN_L_PU 49

PCI_AD<0> 62 48 47 46 45 6 — N8 AD0
PCI_AD<1> — M7 AD1
PCI_AD<2> — L7 AD2
PCI_AD<3> — N6 AD3
PCI_AD<4> — K4 AD4
PCI_AD<5> — M6 AD5
PCI_AD<6> — L6 AD6
PCI_AD<7> — N5 AD7
PCI_AD<8> — N4 AD8
PCI_AD<9> — M2 AD9
PCI_AD<10> — M5 AD10
PCI_AD<11> — L4 AD11
PCI_AD<12> — N3 AD12
PCI_AD<13> — K5 AD13
PCI_AD<14> — L5 AD14
PCI_AD<15> — M4 AD15
PCI_AD<16> — J4 AD16
PCI_AD<17> — H1 AD17
PCI_AD<18> — H3 AD18
PCI_AD<19> — H2 AD19
PCI_AD<20> — G2 AD20
PCI_AD<21> — G4 AD21
PCI_AD<22> — F1 AD22
PCI_AD<23> — C3 AD23
PCI_AD<24> — F3 AD24
PCI_AD<25> — E2 AD25
PCI_AD<26> — F4 AD26
PCI_AD<27> — B1 AD27
PCI_AD<28> — D2 AD28
PCI_AD<29> — E4 AD29
PCI_AD<30> — D3 AD30
PCI_AD<31> — E3 AD31

R7806 22 5% 1/16W MF 402

PCI_CBE_L<0> — K6 C/BE0*
PCI_CBE_L<1> — M3 C/BE1*
PCI_CBE_L<2> — J1 C/BE2*
PCI_CBE_L<3> — A1 C/BE3*

PCI_PAR — N1 PAR
PCI_IRDY_L — K1 IRDY
CBUS_SERR_L_PU — L2 SERR
PCI_SLOTE_IDSEL — F2 IDSEL
CBUS_PERR_L_PU — K3 PERR
PCI_FRAME_L — J2 FRAME
PCI_STOP_L — L1 STOP
PCI_TRDY_L — J3 TRDY
PCI_DEVSEL_L — K2 DEVSEL

R7808 47 5% 1/16W MF 402

PCI_CBUS_RESET_L 5 — PCI_CBUS_RESET_L_R 49 — G3 PRST
PCI_SLOTE_REQ_L 23 — C2 REQ
PCI_SLOTE_GNT_L 23 — C1 GNT
PCI_CLK33M_CBUS 49 5 — G1 PCLK

NC — M9 SPKROUT
NC — M8 RI_OUT/PME
CBUS_SUSPEND_L_PU 49 — N10 SUSPEND

RP7800 10K 5% 1/32W 8SS

5 — 10
6 — CBUS_MFUNC1_PD — N9 MFUNC1
4 — CBUS_MFUNC2_PD — L9 MFUNC2
7 — CBUS_MFUNC3_PD — K10 MFUNC3
3 — CBUS_MFUNC4_PD — M10 MFUNC4
9 — CBUS_MFUNC5_PD — N12 MFUNC5
8 — CBUS_MFUNC6_PD — L10 MFUNC6
2 — NC
1 — NC
SM

PCI_SLOTE_INT_L 23 — K7 MFUNC0

L11 GRST

GND: A2 A11 D1 F13 H4 K8 M13 N2

CRITICAL
U7800
PCI1510GGU
BGA

Clamp for PC Card
Clamp for PCI

NC — H10 CLK_48_RSVD/NC
DA — VR_EN*
L8 — VR_PORT

PPVIO_PCI_CBUS 5

VCCCB — B11 — PPVCC_CBUS_XW (VOLTAGE=5V (or 3.3V) MIN_LINE_WIDTH=10 mil MIN_NECK_WIDTH=6 mil)
VCCP — L3
VCCD0* — N13 — CBUS_VCCD0_L
VCCD1* — L12 — CBUS_VCCD1_L
VPPD0 — K9 — CBUS_VPPD0
VPPD1 — M11 — CBUS_VPPD1

Integrated Pullup CD1*/CCD1* — L13 — CBUS_DET_1_L 49
Integrated Pullup CD2*/CCD2* — B5 — CBUS_DET_2_L 49
IORD*/CAD13 — F12 — CBUS_IORD_L 49
IOWR*/CAD15 — C11 — CBUS_IOWR_L 49
OE*/CAD11 — G10 — CBUS_OE_L 49
CE1*/CC/BE0* — H13 — CBUS_CE1_L 49
Integrated Pullup VS1*/CVS1* — B2 — CBUS_VS1 49
Integrated Pullup VS2*/CVS2* — A9 — CBUS_VS2 49
WE*/CGNT* — D13 — CBUS_WE_L 49
Integrated Pullup RDY/IREQ*/CINT* — A6 — CBUS_READY 49
Integrated Pullup RESET/CRST* — D8 — CBUS_RESET_L 49
REG*/CC/BE3* — A8 — CBUS_REG_L 49
Integrated Pullup / Pulldown BVD1/GSTSCHG/STSCHG*/RI* — C6 — CBUS_BVD1_L 49
Integrated Pullup BVD2/SPKR*/CAUDIO — D6 — CBUS_BVD2_L 49
Integrated Pullup WP/IOIS16*/CCLKRUN* — A5 — CBUS_WP_L 49
CE2/CAD10* — G13 — CBUS_CE2_L 49
Integrated Pullup INPACK/CREQ* — B8 — CBUS_INPACK_L 49
Integrated Pullup WAIT/CSERR* — B6 — CBUS_WAIT_L 49

A0/CAD26 — C7 — CBUS_ADDR<0> 49
A1/CAD25 — D7 — CBUS_ADDR<1> 49
A2/CAD24 — B7 — CBUS_ADDR<2> 49
A3/CAD23 — D10 — CBUS_ADDR<3> 49
A4/CAD22 — B12 — CBUS_ADDR<4> 49
A5/CAD21 — C8 — CBUS_ADDR<5> 49
A6/CAD20 — C9 — CBUS_ADDR<6> 49
A7/CAD18 — A12 — CBUS_ADDR<7> 49
A8/CC/BE1* — E11 — CBUS_ADDR<8> 49
A9/CAD14 — F11 — CBUS_ADDR<9> 49
A10/CAD9 — G11 — CBUS_ADDR<10> 49
A11/CAD12 — G12 — CBUS_ADDR<11> 49
A12/CC/BE2* — D9 — CBUS_ADDR<12> 49
A13/CPAR — E12 — CBUS_ADDR<13> 49
Integrated Pullup A14/CPERR* — D12 — CBUS_ADDR<14> 49
Integrated Pullup A15/CIRDY* — C10 — CBUS_ADDR<15> 49
A16/CCLK — B13 — CBUS_ADDR16_R
A17/CAD16 — F10 — CBUS_ADDR<17> 49
A18/RSVD — E13 — CBUS_ADDR<18> 49
Integrated Pullup A19/CBLOCK* — A13 — CBUS_ADDR<19> 49
Integrated Pullup A20/CSTOP* — E10 — CBUS_ADDR<20> 49
Integrated Pullup A21/CDEVSEL* — D11 — CBUS_ADDR<21> 49
Integrated Pullup A22/CTRDY* — C12 — CBUS_ADDR<22> 49
A23/CFRAME* — A10 — CBUS_ADDR<23> 49
A24/CAD17 — B10 — CBUS_ADDR<24> 49
A25/CAD19 — B9 — CBUS_ADDR<25> 49

D0/CAD27 — A4 — CBUS_DATA<0> 49
D1/CAD29 — C4 — CBUS_DATA<1> 49
D2/RSVD — A3 — CBUS_DATA<2> 49
D3/CAD0 — K11 — CBUS_DATA<3> 49
D4/CAD1 — K12 — CBUS_DATA<4> 49
D5/CAD3 — J13 — CBUS_DATA<5> 49
D6/CAD5 — J10 — CBUS_DATA<6> 49
D7/CAD7 — H12 — CBUS_DATA<7> 49
D8/CAD28 — C5 — CBUS_DATA<8> 49
D9/CAD30 — B4 — CBUS_DATA<9> 49
D10/CAD31 — B3 — CBUS_DATA<10> 49
D11/CAD2 — M12 — CBUS_DATA<11> 49
D12/CAD4 — J11 — CBUS_DATA<12> 49
D13/CAD6 — K13 — CBUS_DATA<13> 49
D14/RSVD — J12 — CBUS_DATA<14> 49
D15/CAD8 — H11 — CBUS_DATA<15> 49

PC Card Power Switch

Make sure Vcc and Vpp are wide plane/traces to minimize inductance!

5 PP5V_CBUS
5 PP3V3_CBUS

CRITICAL
U7801
TPS2211
SSOI

NC — V_12 — AVPP — 10
V_5_1
V_5_2 — AVCC0 — 11
V_3_1 — AVCC1 — 12
V_3_2 — AVCC2 — 13
VCCD0
VCCD1
VPPD0
VPPD1
SHTDWN — 15
GND — 7
OC — 8 NC

PPVPP_CBUS 49 VOLTAGE=5V (or 3.3V) MIN_LINE_WIDTH=25 mil MIN_NECK_WIDTH=10 mil
PPVCC_CBUS 49 VOLTAGE=5V (or 3.3V) MIN_LINE_WIDTH=25 mil MIN_NECK_WIDTH=10 mil

C7808 0.1UF 20% 10V CERM 402
C7809 0.1UF 20% 10V CERM 402

PCI_CBUS_RESET_L_R 49 — Disable card power during reset

0.1uF are used to increase ESD of up to 10kV

XW7800 SM — This is an internal board short. Allows thinner trace to BGA

TI reference schematic does not have bulk on PPVCC_CBUS

C7810 2.2uF 20% 10V CERM 805
C7811 2.2uF 20% 10V CERM 805

R7809 47 5% 1/16W MF 402 — CBUS_ADDR<16> 49

PC Card/CardBus Connector

CRITICAL
J7800
QT500806-L111
M-ST-SM

	84	81	
	2	1	CBUS_DATA<3> 49
	4	3	CBUS_DATA<4> 49
CBUS_DATA<11> 49	6	5	CBUS_DATA<5> 49
CBUS_DATA<12> 49	8	7	CBUS_DATA<6> 49
CBUS_DATA<13> 49	10	9	
	12	11	CBUS_DATA<7> 49
CBUS_DATA<14> 49	14	13	CBUS_CE1_L 49
CBUS_DATA<15> 49	16	15	CBUS_ADDR<10> 49
CBUS_CE2_L 49	18	17	CBUS_OE_L 49
CBUS_VS1 49	20	19	
	22	21	CBUS_ADDR<11> 49
CBUS_IORD_L 49	24	23	CBUS_ADDR<9> 49
CBUS_IOWR_L 49	26	25	CBUS_ADDR<8> 49
CBUS_ADDR<17> 49	28	27	CBUS_ADDR<13> 49
CBUS_ADDR<18> 49	30	29	
	32	31	CBUS_ADDR<14> 49
CBUS_ADDR<19> 49	34	33	CBUS_WE_L 49
CBUS_ADDR<20> 49	36	35	CBUS_READY 49
CBUS_ADDR<21> 49	38	37	PPVCC_CBUS 49
PPVCC_CBUS 49	40	39	
	42	41	PPVPP_CBUS 49
PPVPP_CBUS 49	44	43	CBUS_ADDR<16> 49
CBUS_ADDR<22> 49	46	45	CBUS_ADDR<15> 49
CBUS_ADDR<23> 49	48	47	CBUS_ADDR<12> 49
CBUS_ADDR<24> 49	50	49	
	52	51	CBUS_ADDR<7> 49
CBUS_ADDR<25> 49	54	53	CBUS_ADDR<6> 49
CBUS_VS2 49	56	55	CBUS_ADDR<5> 49
CBUS_RESET_L 49	58	57	CBUS_ADDR<4> 49
CBUS_WAIT_L 49	60	59	
	62	61	CBUS_ADDR<3> 49
CBUS_INPACK_L 49	64	63	CBUS_ADDR<2> 49
CBUS_REG_L 49	66	65	CBUS_ADDR<1> 49
CBUS_BVD2_L 49	68	67	CBUS_ADDR<0> 49
CBUS_BVD1_L 49	70	69	
	72	71	CBUS_DATA<0> 49
CBUS_DATA<8> 49	74	73	CBUS_DATA<1> 49
CBUS_DATA<9> 49	76	75	CBUS_DATA<2> 49
CBUS_DATA<10> 49	78	77	CBUS_WP_L 49
CBUS_DET_2_L 49	80	79	
	83	82	

516S0089

Master: Fizzy

CardBus Interface

NOTICE OF PROPRIETARY PROPERTY

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 78 OF 103	

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:07 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_P1_C
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_N1_C
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_P1
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_N1
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_P2_C
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_N2_C
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_P2
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_N2
UATA_DD			UATA_DD<15..8>
UATA_DD7			UATA_DD<7>
UATA_DD			UATA_DD<6..0>
UATA_HOST			UATA_DA<2..0>
UATA_HOST			UATA_CS0_L
UATA_HOST			UATA_CS1_L
UATA_HOST			UATA_HSTROBE
UATA_HOST			UATA_STOP
UATA_HOST_R			UATA_DMACK_L
UATA_HOST_R			UATA_RESET_L
UATA_DEV_R_C			UATA_DSTROBE
UATA_DEV_R			UATA_DMARQ
UATA_DEV_R			UATA_INTRQ

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils outer
Primary Max Sep:	9 mils inner
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

SATA_VDD x 5

_PP1V2_PWRON_DISK_SB

C8000 0.1uF 20% 10V CERM 402
C8001 0.1uF 20% 10V CERM 402
C8002 0.1uF 20% 10V CERM 402
C8003 0.1uF 20% 10V CERM 402
C8004 0.1uF 20% 10V CERM 402

AB14 AB17 T14 W15 Y18 → SATA_VDD

U2300 OMIT
SHASTA
V2.0
BGA
(5 OF 8)

UD_IDEDD_0_H	J6	UATA_DD_R<0>
UD_IDEDD_1_H	H7	UATA_DD_R<1>
UD_IDEDD_2_H	H6	UATA_DD_R<2>
UD_IDEDD_3_H	E2	UATA_DD_R<3>
UD_IDEDD_4_H	C1	UATA_DD_R<4>
UD_IDEDD_5_H	C2	UATA_DD_R<5>
UD_IDEDD_6_H	E3	UATA_DD_R<6>
UD_IDEDD_7_H	G6	UATA_DD_R<7>
UD_IDEDD_8_H	G5	UATA_DD_R<8>
UD_IDEDD_9_H	D4	UATA_DD_R<9>
UD_IDEDD_10_H	G7	UATA_DD_R<10>
UD_IDEDD_11_H	F6	UATA_DD_R<11>
UD_IDEDD_12_H	C3	UATA_DD_R<12>
UD_IDEDD_13_H	F5	UATA_DD_R<13>
UD_IDEDD_14_H	E5	UATA_DD_R<14>
UD_IDEDD_15_H	D5	UATA_DD_R<15>
UD_IDEDA0_H	E6	UATA_DA_R<0>
UD_IDEDA1_H	C4	UATA_DA_R<1>
UD_IDEDA2_H	D6	UATA_DA_R<2>
UD_IDECS1FX_L	B3	UATA_CS0_L_R
UD_IDECS3FX_L	B4	UATA_CS1_L_R
UD_IDEDMACK_L	E8	UATA_DMACK_L_R
UD_IDERD_L	E4	UATA_HSTROBE_R
UD_IDEWR_L	D3	UATA_STOP_R
UD_IDERST_L	E7	UATA_RESET_L_R

UATA

DSTROBE aka:
IORDY/HDMARDY*

HSTROBE aka:
DIOR*

STOP aka:
DIOW*

UATA_DSTROBE	F9	UD_IDECHRDY_H	
UATA_DMARQ	D7	UD_IDEDMARQ_H	
UATA_INTRQ	C5	UD_IDEINTRQ_H	

SATA_RXD_P1_C	Y17	RXDP1	TXDP1 → AA16 SATA_TXD_P1
SATA_RXD_N1_C	Y16	RXDN1	TXDN1 → AB16 SATA_TXD_N1
SATA_RXD_P2_C	AB15	RXDP2	TXDP2 → Y15 SATA_TXD_P2
SATA_RXD_N2_C	AA15	RXDN2	TXDN2 → Y14 SATA_TXD_N2

SATA 0
SATA 1

SATA_GND → AA14 AA17 T13 W16

AC coupling required for any SATA pair used.
Recommend 0.1uF cap placed close to Shasta.
(Caps provided by device page)

UATA Termination

R8005 10K 5% 1/10W MF 402 → _PP1V2_PWRON_DISK_SB

RP8000	4	5	UATA_DD_R<0> ↔ UATA_DD<0>
RP8000	3	6	UATA_DD_R<1> ↔ UATA_DD<1>
RP8000	2	7	UATA_DD_R<2> ↔ UATA_DD<2>
RP8003	4	5	UATA_DD_R<3> ↔ UATA_DD<3>
RP8001	1	8	UATA_DD_R<4> ↔ UATA_DD<4>
RP8001	2	7	UATA_DD_R<5> ↔ UATA_DD<5>
RP8003	3	6	UATA_DD_R<6> ↔ UATA_DD<6>
RP8002	1	8	UATA_DD_R<7> ↔ UATA_DD<7>
RP8002	2	7	UATA_DD_R<8> ↔ UATA_DD<8>
RP8003	2	7	UATA_DD_R<9> ↔ UATA_DD<9>
RP8000	1	8	UATA_DD_R<10> ↔ UATA_DD<10>
RP8002	4	5	UATA_DD_R<11> ↔ UATA_DD<11>
RP8001	3	6	UATA_DD_R<12> ↔ UATA_DD<12>
RP8002	3	6	UATA_DD_R<13> ↔ UATA_DD<13>
RP8004	1	8	UATA_DD_R<14> ↔ UATA_DD<14>
RP8003	1	8	UATA_DD_R<15> ↔ UATA_DD<15>
RP8004	2	7	UATA_DA_R<0> ↔ UATA_DA<0>
RP8001	4	5	UATA_DA_R<1> ↔ UATA_DA<1>
RP8004	4	5	UATA_DA_R<2> ↔ UATA_DA<2>
RP8004	3	6	UATA_RESET_L_R ↔ UATA_RESET_L
R8000	1	2	UATA_CS0_L_R ↔ UATA_CS0_L
R8001	1	2	UATA_CS1_L_R ↔ UATA_CS1_L
R8002	1	2	UATA_HSTROBE_R ↔ UATA_HSTROBE
R8003	1	2	UATA_STOP_R ↔ UATA_STOP
R8004	1	2	UATA_DMACK_L_R ↔ UATA_DMACK_L

All resistors: 5% 1/16W SM1 (MF 402 for R8000, R8001, R8002, R8003, R8004)

Master: Link

Shasta Disk

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 80 OF 103	

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:21 2004

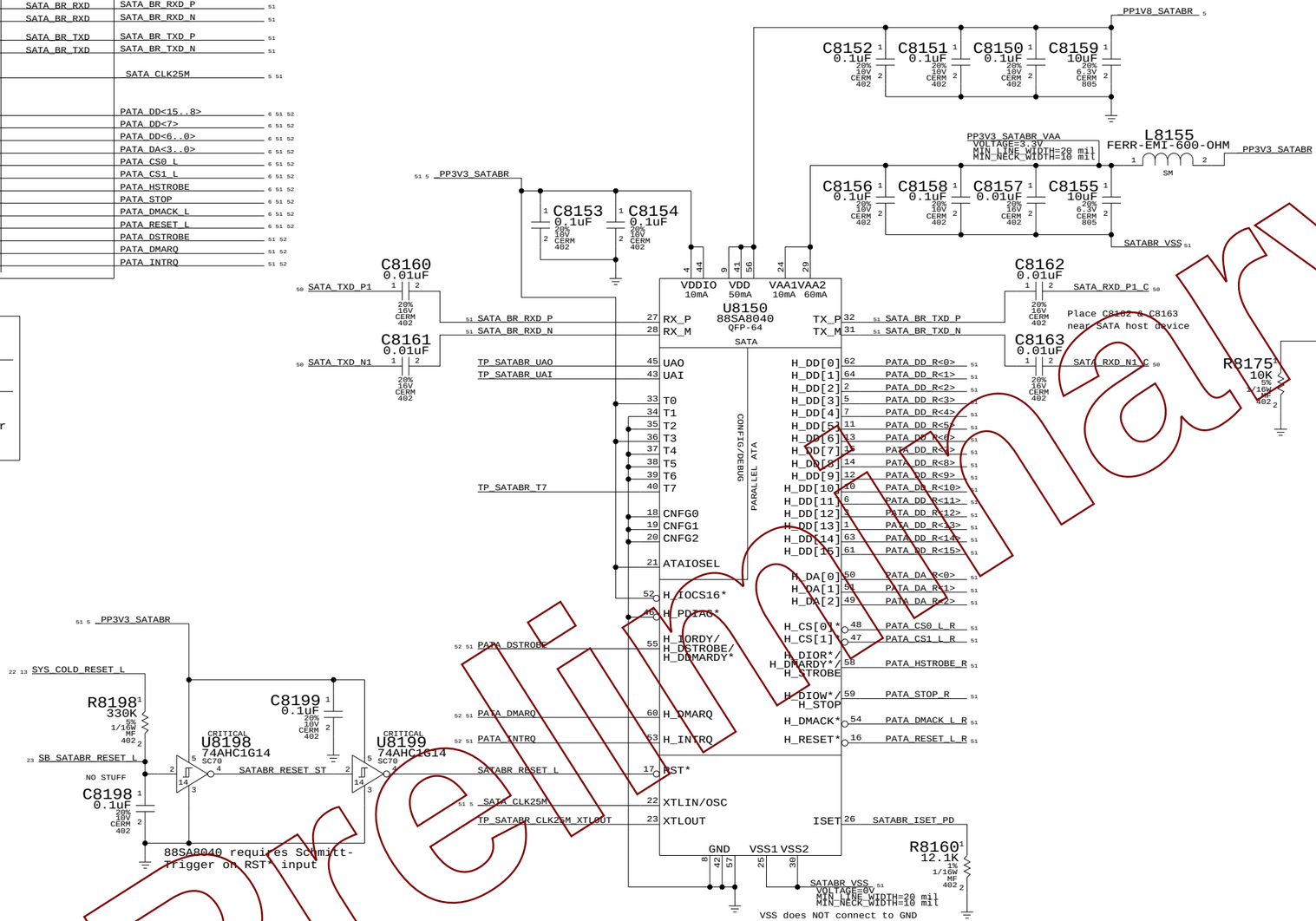
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PROVIDED BY SATA CONTROLLER	SATA	SATA_BR_RXD	SATA_BR_RXD_P 51
	SATA	SATA_BR_RXD	SATA_BR_RXD_N 51
	SATA	SATA_BR_TXD	SATA_BR_TXD_P 51
	SATA	SATA_BR_TXD	SATA_BR_TXD_N 51
	CLOCKS		SATA_CLK25M 5 51
PATA_HOST			PATA_DD<15..8> 6 51 52
PATA_DD7			PATA_DD<7> 6 51 52
PATA_HOST			PATA_DD<6..0> 6 51 52
PATA_HOST			PATA_DA<3..0> 6 51 52
PATA_HOST			PATA_CS0_L 6 51 52
PATA_HOST			PATA_CS1_L 6 51 52
PATA_HOST			PATA_HSTROBE 6 51 52
PATA_HOST			PATA_STOP 6 51 52
PATA_HOST_R			PATA_DMACK_L 6 51 52
PATA_HOST_R			PATA_RESET_L 6 51 52
PATA_DEV_R_C			PATA_DSTROBE 51 52
PATA_DEV_R			PATA_DMARQ 51 52
PATA_DEV_R			PATA_INTRQ 51 52

Page Notes

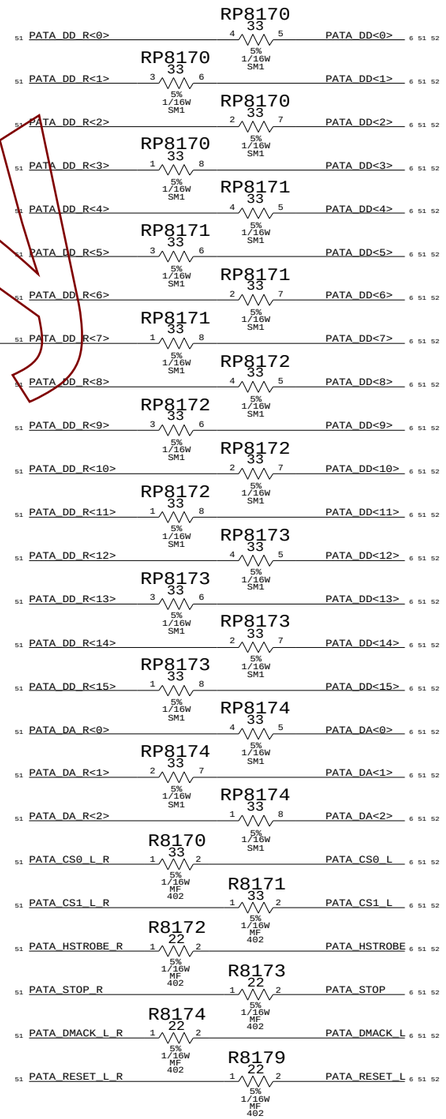
Power aliases required by this page:
- _PP3V3_SATABR
- _PP1V8_SATABR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SATA_1_BRIDGE (/ SATA_1_CONN)
  Selects whether 88SA8040 SATA Bridge or SATA connector is connected to Shasta SATA port 1.



PATA Termination



Sourced by host or bi-directional
Terminate near bridge

88SA8040 Config Straps (Device Mode):

T<1..0> - Vendor Unique (VU) and Read/Write Long

T<1..0>	VU Type	R/W Long Type
00	1	1
01	1	2
10	1	1 (default)
11	2	2

T2 - SSC Enable
1 - Enable SATA Spread Spectrum Clocking
0 - Disable SATA Spread Spectrum Clocking
(Internal Pull-down)

T<4..3> - Reference Clock Configuration

T<4..3>	Clock Frequency
00	20 MHz
01	25 MHz
10	30 MHz
11	40 MHz

(Internal Pull-downs)

T5 - Fixed UDMA
1 - UDMA mode fixed by CNFG<2..0> pins
0 - UDMA mode adjustable with Set Features
(Internal Pull-up)

T6 - Power Mode Enable
1 - Enable translation of ATA power management commands into SATA Partial or Slumber mode
0 - Disable translation
(Internal Pull-down)

T7 - Plug-in (output)
1 - SATA cable plugged in
0 - SATA cable unplugged
(Internal Pull-down)

CNFG<2..0> - Mode Configuration

CNFG<2..0>	Mode
000	Device Mode - 100MB/s
001	Device Mode - 133MB/s
010	Device Mode - 150MB/s (default)
100	Host Mode - 100MB/s
101	Host Mode - 133MB/s
110	Host Mode - 150MB/s
011	Reserved
111	Reserved

H_IOCS16_N - DMA_EN
1 - Good status on Set Features to set DMA
0 - Error status on Set Features to set DMA
(Internal Pull-up)

H_PDIAG_N - PATA_ORDER
1 - Reverse Order mode for Parallel ATA pins
0 - Normal Order mode

ATAIOSEL - ATA I/O Enable
1 - Enable output to ATA bus
0 - Disable output to ATA bus
(Internal Pull-up)

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:28 2004

Master: Link

Serial ATA Bridge

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6532 | REV. 03

SCALE NONE | SHT 81 OF 103

Page Notes

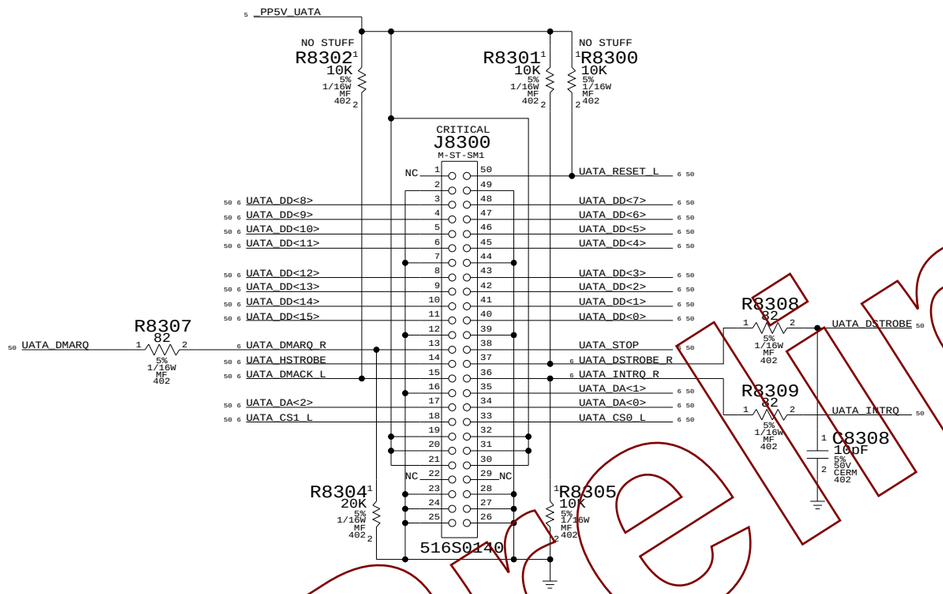
Power aliases required by this page:
- _PP5V_PATA
- _PP5V_UATA
- _PP3V3_PATA
- _PP3V3_UATA

Signal aliases required by this page:
(NONE)

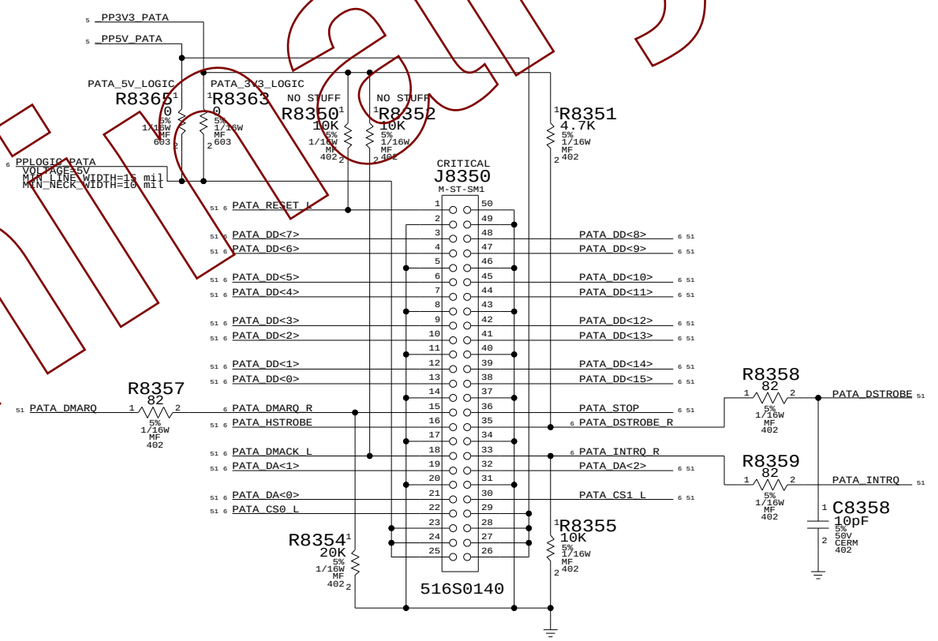
BOM options provided by this page:
(NONE)

NOTE: ATA constraints are expected to be defined on another page (ATA host) and apply to this page via XNets.

UATA (SouthBridge) Connector



PATA (SATA Bridge) Connector



DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:36 2004

IDE Connectors

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 83 OF 103	

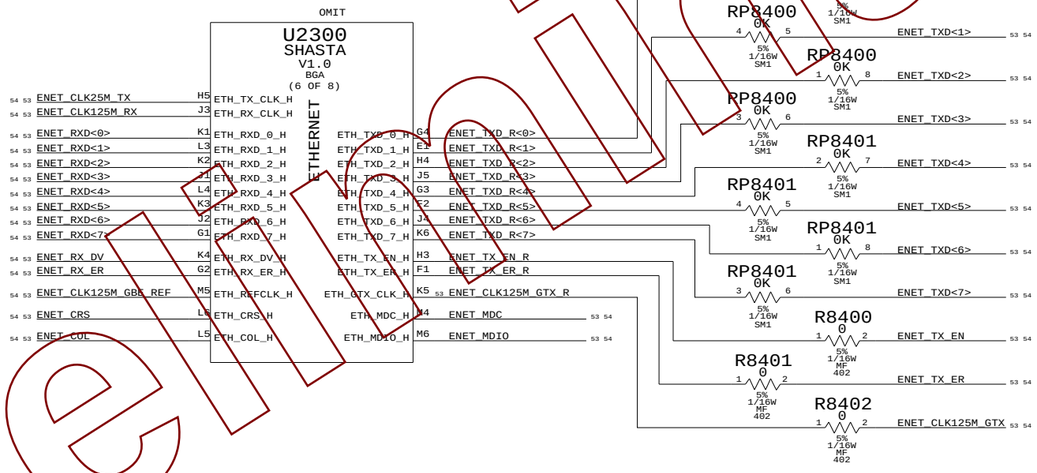
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
ENET_RX_CLK	ENET	15_MIL_SPACING		ENET_CLK25M_TX 53 54
ENET_RX_CLK	ENET	15_MIL_SPACING		ENET_CLK125M_RX 53 54
ENET_GBE_REF	ENET	15_MIL_SPACING		ENET_CLK125M_GBE_REF 53 54
ENET_TX_CLK	ENET	15_MIL_SPACING		ENET_CLK125M_GTX 53 54
	ENET	15_MIL_SPACING		ENET_CLK125M_GTX_R 53
ENET_RX	ENET			ENET_RXD<7..0> 53 54
ENET_RX_CTL	ENET			ENET_RX_DV 53 54
ENET_RX_CTL	ENET			ENET_RX_ER 53 54
ENET_TX	ENET			ENET_TXD<7..0> 53 54
ENET_TX_CTL	ENET			ENET_TX_EN 53 54
ENET_TX_CTL	ENET			ENET_TX_ER 53 54
ENET_RX_CTL	ENET			ENET_CRS 53 54
ENET_RX_CTL	ENET			ENET_COL 53 54
ENET_MDC	ENET			ENET_MDC 53 54
ENET_MDIO	ENET			ENET_MDIO 53 54

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Master: Link

Shasta Ethernet

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE: NONE

SHT 84 OF 103

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 18:36:38 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	15 MIL SPACING		ENET_CLK125M_GBE_REF_R
	15 MIL SPACING		ENET_CLK125M_RX_R
	15 MIL SPACING		ENET_CLK25M_TX_R
ENET_MDI	ENET	ENET_MDI0	ENET_MDI_P<0>
ENET_MDI	ENET	ENET_MDI0	ENET_MDI_N<0>
ENET_MDI	ENET	ENET_MDI1	ENET_MDI_P<1>
ENET_MDI	ENET	ENET_MDI1	ENET_MDI_N<1>
ENET_MDI	ENET	ENET_MDI2	ENET_MDI_P<2>
ENET_MDI	ENET	ENET_MDI2	ENET_MDI_N<2>
ENET_MDI	ENET	ENET_MDI3	ENET_MDI_P<3>
ENET_MDI	ENET	ENET_MDI3	ENET_MDI_N<3>
VESTA_CLK25M_XTAL	15 MIL SPACING		VESTA_CLK25M_XTALI
	15 MIL SPACING		VESTA_CLK25M_XTALO
	15 MIL SPACING		VESTA_CLK25M_XTALO_R

Page Notes

Power aliases required by this page:
- _PP3V3_ENET
- _PP2V5_ENETFW
- _PP1V2_ENETFW

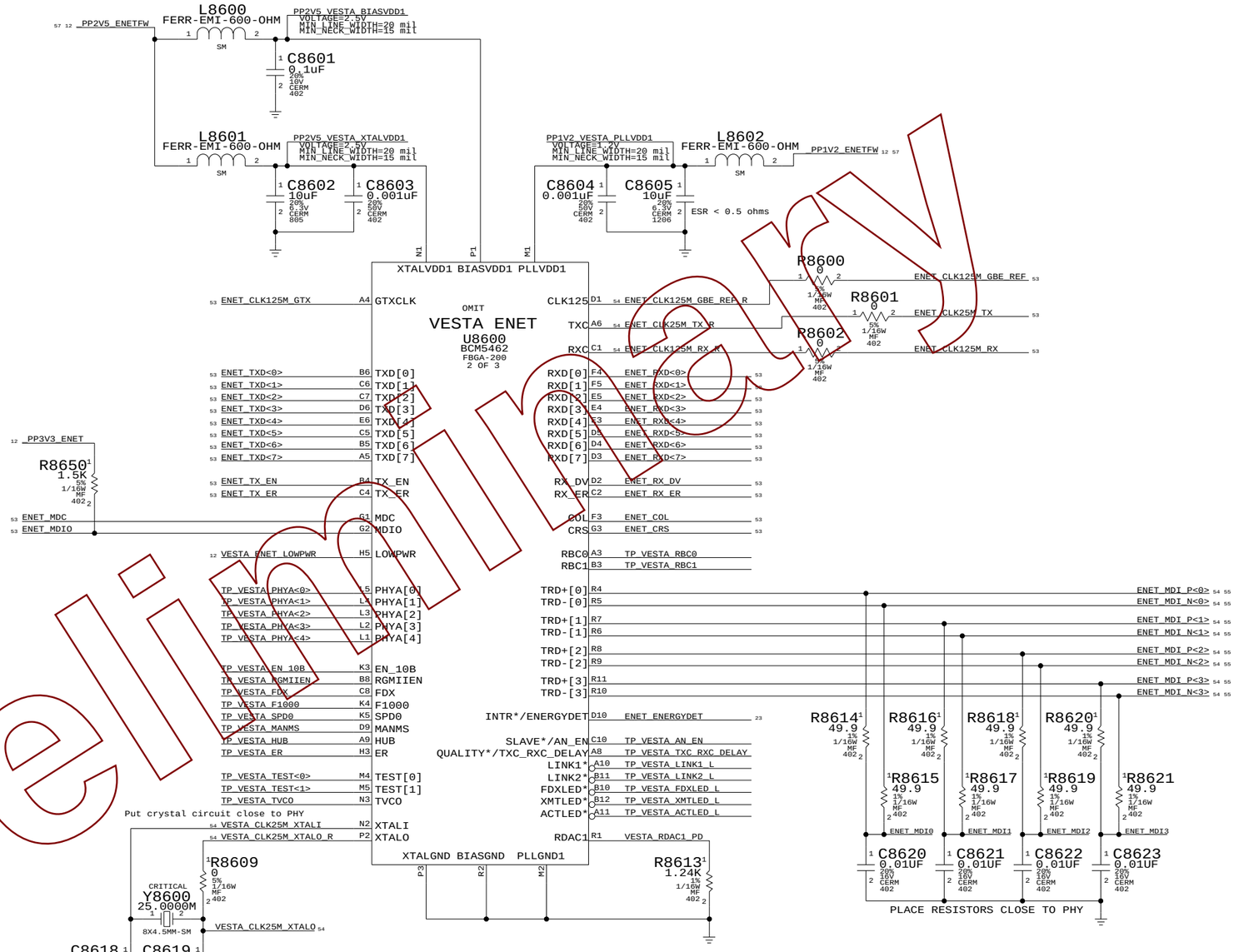
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 15 mils
Length Tolerance: 50 mils
Primary Max Sep: 5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for ENET data pairs is 100 ohms.



Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:51 2004

Master: Link

Vesta Ethernet PHY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 86 OF 103	

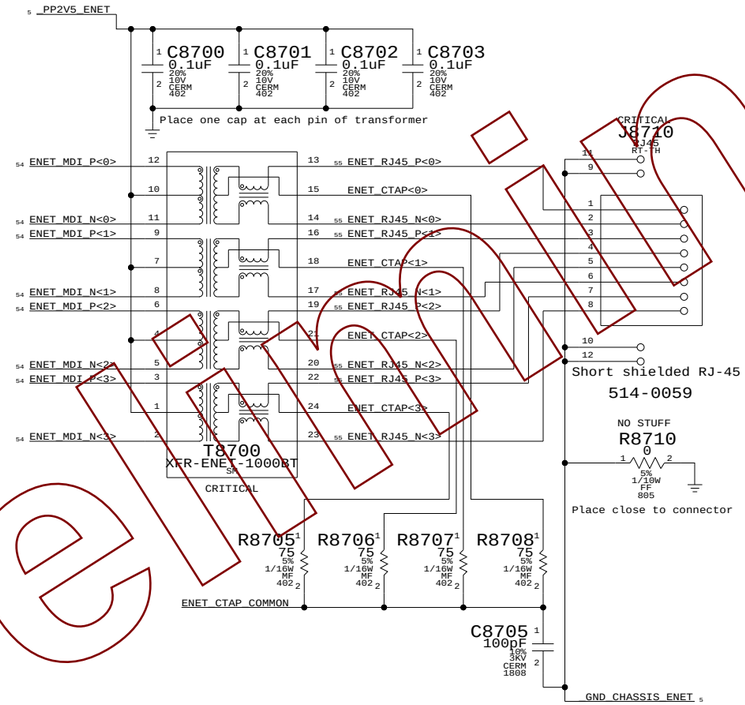
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PROVIDED BY ETHERNET PHY	ENET	ENET_RJ45_0	ENET_RJ45_P<0> 55
	ENET	ENET_RJ45_0	ENET_RJ45_N<0> 55
	ENET	ENET_RJ45_1	ENET_RJ45_P<1> 55
	ENET	ENET_RJ45_1	ENET_RJ45_N<1> 55
	ENET	ENET_RJ45_2	ENET_RJ45_P<2> 55
	ENET	ENET_RJ45_2	ENET_RJ45_N<2> 55
	ENET	ENET_RJ45_3	ENET_RJ45_P<3> 55
	ENET	ENET_RJ45_3	ENET_RJ45_N<3> 55

Page Notes

Power aliases required by this page:
- _PP2V5_ENET
- _GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:58 2004

Ethernet Connector

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 87 OF 103	

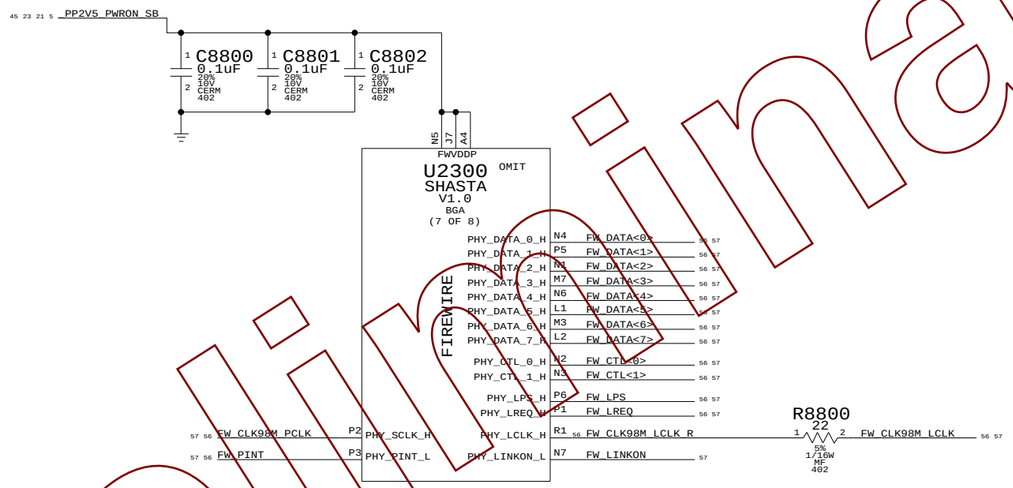
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
FW	FW			FW_DATA<7..0> 56 57
FW	FW			FW_CTL<1..0> 56 57
FW_LPS	FW			FW_LPS 56 57
FW_LREQ	FW			FW_LREQ 56 57
FW_PINT	FW			FW_PINT 56 57
FW_LCLK	FW	15_MIL_SPACING		FW_CLK98M_LCLK 56 57
FW_PCLK	FW	15_MIL_SPACING		FW_CLK98M_PCLK 56 57
		15_MIL_SPACING		FW_CLK98M_LCLK_R 56

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Master: Link

Shasta FireWire

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 88 OF 103	

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:06 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
(PROVIDED BY LINK PAGE)	15 MIL SPACING		FW_CLK98M_PCLK_R	57
FW_TPA1	FW	FW_TPA0	FW_TPA_P<0>	57 58
FW_TPA1	FW	FW_TPA0	FW_TPA_N<0>	57 58
FW_TPB1	FW	FW_TPB0	FW_TPB_P<0>	57 58
FW_TPB1	FW	FW_TPB0	FW_TPB_N<0>	57 58
FW_TPA2	FW	FW_TPA1	FW_TPA_P<1>	57 58
FW_TPA2	FW	FW_TPA1	FW_TPA_N<1>	57 58
FW_TPB2	FW	FW_TPB1	FW_TPB_P<1>	57 58
FW_TPB2	FW	FW_TPB1	FW_TPB_N<1>	57 58
FW_TPA3	FW	FW_TPA2	FW_TPA_P<2>	57 58
FW_TPA3	FW	FW_TPA2	FW_TPA_N<2>	57 58
FW_TPB3	FW	FW_TPB2	FW_TPB_P<2>	57 58
FW_TPB3	FW	FW_TPB2	FW_TPB_N<2>	57 58
VESTA_CLK24M_XTAL	15 MIL SPACING		VESTA_CLK24M_XTALI	57
	15 MIL SPACING		VESTA_CLK24M_XTALO	57
	15 MIL SPACING		VESTA_CLK24M_XTALO_R	57

Page Notes

Power aliases required by this page:
- _PPFW_PHY
- _PP3V3_FW
- _PP3V3_ENETFW
- _PP2V5_ENETFW
- _PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW

Line To Line: 15 mils
Length Tolerance: 100 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

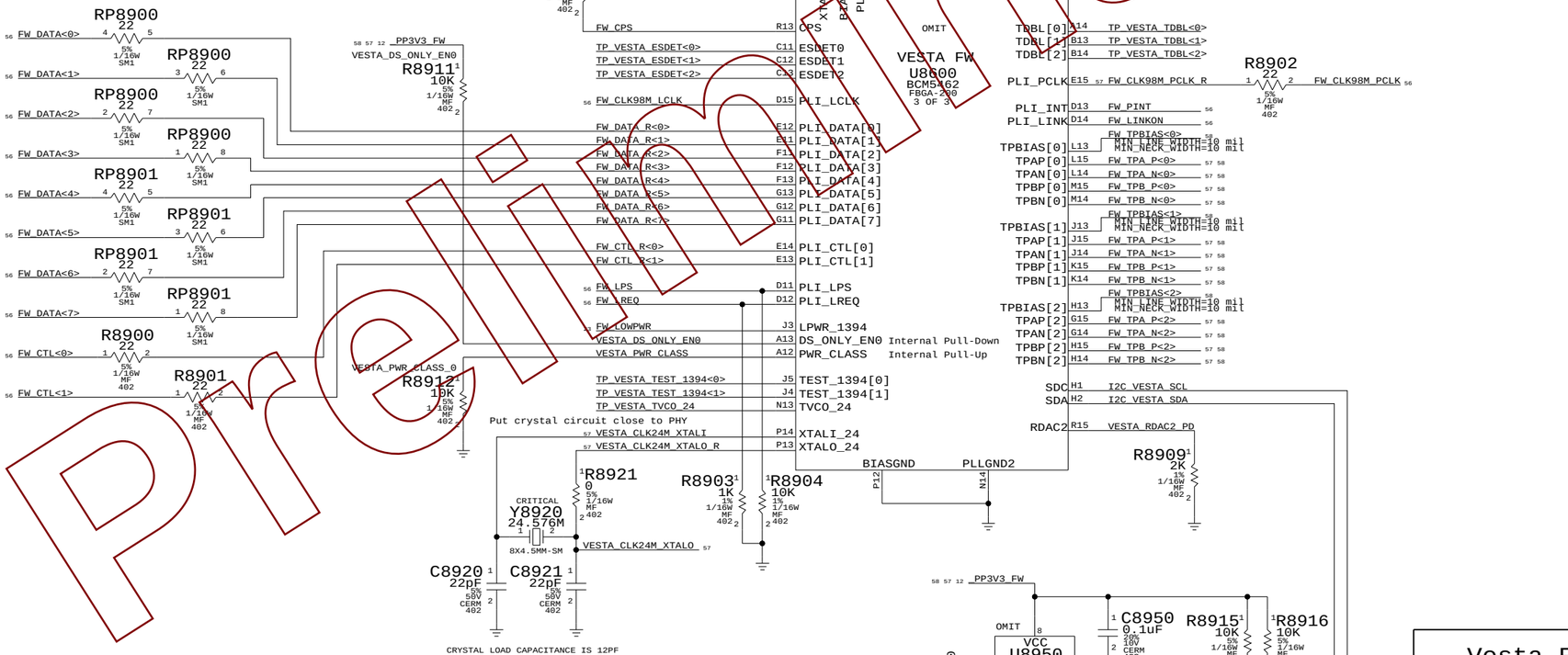
NOTE: Target differential impedance for FW data pairs is 110 ohms.

Vesta Config Straps:

PWR_CLASS - FireWire Power Class
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

DS_ONLY_EN0 - Port 0 Data/Strobe
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:14 2004



Master: Link

Vesta FireWire PHY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 89 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
PROVIDED BY PHY PAGE	FW	FW_PORT1_TPA_FL	FW_PORT1_TPA_P_FL	6 58
	FW	FW_PORT1_TPA_FL	FW_PORT1_TPA_N_FL	6 58
	FW	FW_PORT1_TPB_FL	FW_PORT1_TPB_P_FL	6 58
	FW	FW_PORT1_TPB_FL	FW_PORT1_TPB_N_FL	6 58
	FW	FW_PORT2_TPA_FL	FW_PORT2_TPA_P_FL	6 58
	FW	FW_PORT2_TPA_FL	FW_PORT2_TPA_N_FL	6 58
	FW	FW_PORT2_TPB_FL	FW_PORT2_TPB_P_FL	6 58
	FW	FW_PORT2_TPB_FL	FW_PORT2_TPB_N_FL	6 58

Page Notes

Power aliases required by this page:
- _PPFW_PORT1
- _PPFW_PORT2
- _PPFW_PORT3
- _PP3V3_FW
- _GND_CHASSIS_FW_PORT1
- _GND_CHASSIS_FW_PORT2
- _GND_CHASSIS_FW_PORT3

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

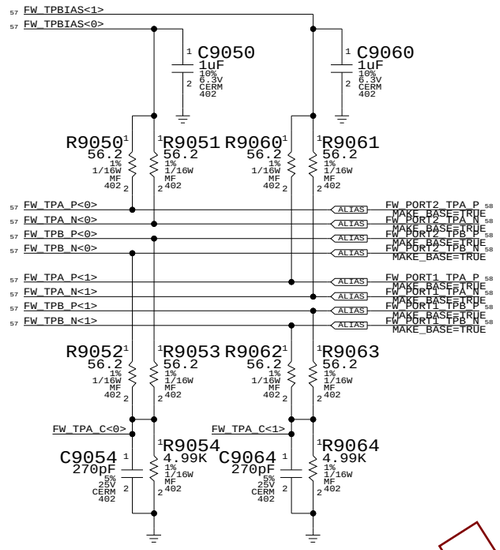
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

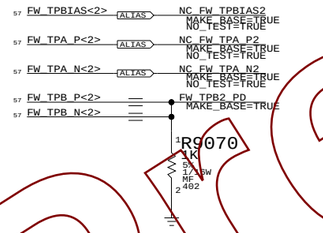
Termination

Place close to FireWire PHY

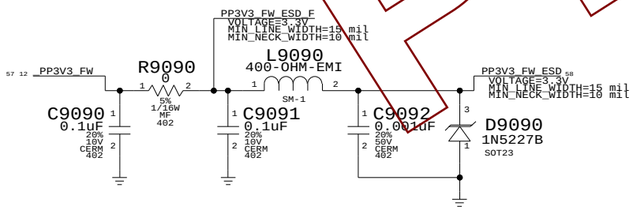


3rd TPA/TPB pair unused

(Is this correct for Vesta?)

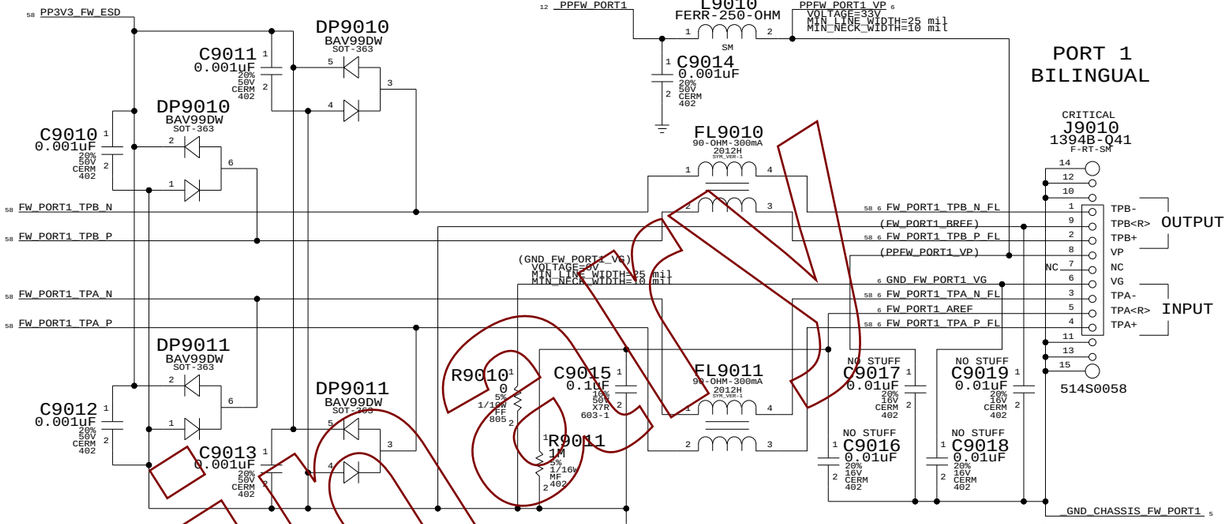


ESD Rail



Cable Power

"Snapback" & "Late VG" Protection

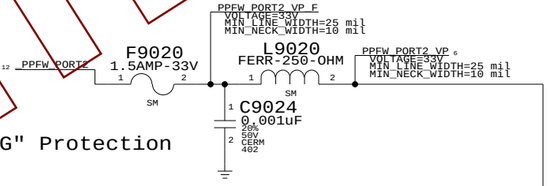


AREF needs to be isolated from all local grounds per 1394b spec

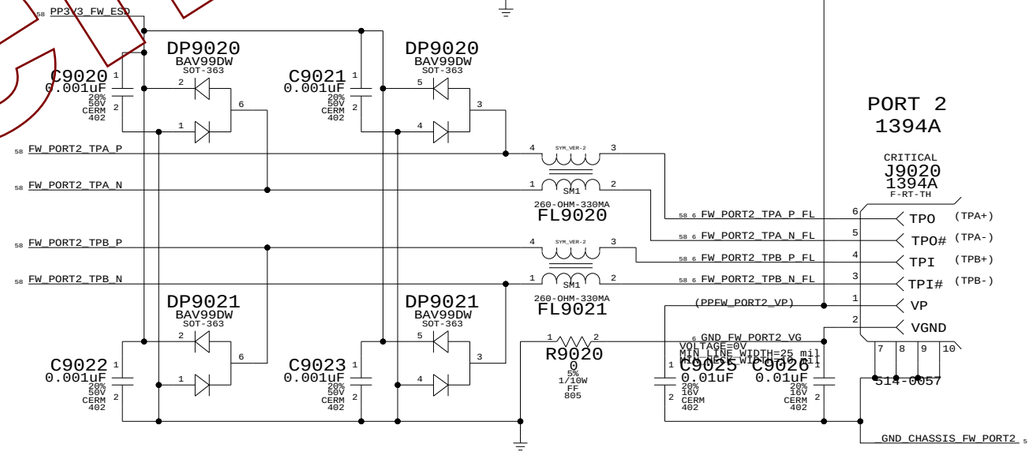
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Cable Power



"Snapback" & "Late VG" Protection



FireWire Ports

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:30 2004

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 90 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_0	USB2_P<0> 5 6 59
USB2_0	USB2	USB2	USB2_0	USB2_N<0> 5 6 59
USB2_1	USB2	USB2	USB2_1	USB2_P<1> 5 6 59
USB2_1	USB2	USB2	USB2_1	USB2_N<1> 5 6 59
USB2_2	USB2	USB2	USB2_2	USB2_P<2> 5 6 59
USB2_2	USB2	USB2	USB2_2	USB2_N<2> 5 6 59
USB2_3	USB2	USB2	USB2_3	USB2_P<3> 5 6 59
USB2_3	USB2	USB2	USB2_3	USB2_N<3> 5 6 59
USB2_4	USB2	USB2	USB2_4	USB2_P<4> 5 6 59
USB2_4	USB2	USB2	USB2_4	USB2_N<4> 5 6 59
USB2_NEC_XTAL		15_MIL_SPACING		NEC_CLK30M_XT1 59
		15_MIL_SPACING		NEC_CLK30M_XT2 59
		15_MIL_SPACING		NEC_CLK30M_XT2_R 59

Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

U2300 SHASTA V1.0 BGA (8 OF 8) OMIT

NC0	P7	TP_SB_NC_P7
NC1	P8	TP_SB_NC_P8
NC2	R3	TP_SB_NC_R3
NC3	R4	TP_SB_NC_R4
NC4	R5	TP_SB_NC_R5
NC5	R6	TP_SB_NC_R6
NC6	R7	TP_SB_NC_R7
NC7	R8	TP_SB_NC_R8
NC8	T1	TP_SB_NC_T1
NC9	T2	TP_SB_NC_T2
NC10	T3	TP_SB_NC_T3
NC11	T4	TP_SB_NC_T4
NC12	T5	TP_SB_NC_T5
NC13	T6	TP_SB_NC_T6
NC14	T7	TP_SB_NC_T7
NC15	T8	TP_SB_NC_T8
NC16	U1	TP_SB_NC_U1
NC17	U2	TP_SB_NC_U2
NC18	U3	TP_SB_NC_U3
NC19	U4	TP_SB_NC_U4
NC20	U5	TP_SB_NC_U5
NC21	U6	TP_SB_NC_U6
NC22	V1	TP_SB_NC_V1
NC23	V2	TP_SB_NC_V2
NC24	V3	TP_SB_NC_V3
NC25	V4	TP_SB_NC_V4
NC26	W1	TP_SB_NC_W1
NC27	W3	TP_SB_NC_W3
NC28	Y1	TP_SB_NC_Y1
NC29	Y3	TP_SB_NC_Y3

59 5 _PP3V3_PWRON_USB
L9135 FERR-EMI-100-OHM SM
PP3V3_PWRON_NEC_AVDD VOLTAGE=3.3V MIN_LINE_WIDTH=20 mil MIN_NECK_WIDTH=10 mil
R9135 4.7 5% 1/16W MF 603
C9135 10uF 20% 6.3V CERM 805
C9136 0.1uF 20% 10V CERM 402
C9137 0.1uF 20% 10V CERM 402
C9120 10uF 20% 6.3V CERM 805
C9121 0.1uF 20% 10V CERM 402
C9122 0.1uF 20% 10V CERM 402
C9123 0.1uF 20% 10V CERM 402
C9124 0.1uF 20% 10V CERM 402
C9125 0.1uF 20% 10V CERM 402
C9126 0.1uF 20% 10V CERM 402
C9127 0.1uF 20% 10V CERM 402
C9128 0.1uF 20% 10V CERM 402
C9129 0.1uF 20% 10V CERM 402
C9130 0.1uF 20% 10V CERM 402
P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 VDD
M10 N12 AVDD

CRITICAL
U7700 NEC_uPD720101_USB2 FCBGA

59 5 _PP3V3_PWRON_USB
R9110 10K 5% 1/16W MF 402
RP9110 10K 5% 1/16W SM1
6 5 USB2_OC<0> (USB2_OC<0>) B12 OCI1
6 5 USB2_OC<1> (USB2_OC<1>) B11 OCI2
5 USB2_OC<2> (USB2_OC<2>) B10 OCI3
5 USB2_OC<3> (USB2_OC<3>) C10 OCI4
5 USB2_OC<4> (USB2_OC<4>) B9 OCI5
6 5 USB2_PWREN<0> C12 PRON1
6 5 USB2_PWREN<1> A11 PRON2
5 USB2_PWREN<2> C11 PRON3
5 USB2_PWREN<3> C10 PRON4
5 USB2_PWREN<4> A9 PRON5

59 5 _PP3V3_PWRON_USB
R9140 1.5K 5% 1/16W MF 402
R9141 1.5K 5% 1/16W MF 402
NEC_NC1_PU P6 NC1
NEC_NC2_PU M6 NC2

59 NEC_CLK30M_XT1 L9 XT1/SCLK
59 NEC_CLK30M_XT2_R P8 XT2
R9145 100 5% 1/16W MF 402
CRITICAL
Y9145 30.0000M 8X4.5MM-SM
NEC_CLK30M_XT2 59
C9145 22pF 5% 50V CERM 402
C9146 22pF 5% 50V CERM 402
Y9145 LOAD CAPACITANCE IS 16pF

VSS
B1 N2 P10 M3 H5 B5 A2 D2 M2 K1 B4 M1 L12 H12 D12 G4 J11 F11 D8
R9139 0 5% 1/16W MF 603
AVSS AVSS(R)
Tie to GND at ball N11
GND_NEC_AVSS_R VOLTAGE=0V MIN_LINE_WIDTH=20 mil MIN_NECK_WIDTH=10 mil

RREF P11 NEC_RREF_PD
R9138 9.09K 1% 1/16W MF 402

R9100 36 1% 1/16W MF 402
RSDM1 M14 USB_NEC_N<0>
DM1 M13 (USB2_N<0>) USB2_N<0> 5 6 59
DP1 L14 (USB2_P<0>) USB2_P<0> 5 6 59
RSDP1 K13 USB_NEC_P<0>

R9101 36 1% 1/16W MF 402

R9102 36 1% 1/16W MF 402
RSDM2 K14 USB_NEC_N<1>
DM2 K12 (USB2_N<1>) USB2_N<1> 5 6 59
DP2 J14 (USB2_P<1>) USB2_P<1> 5 6 59
RSDP2 J12 USB_NEC_P<1>

R9103 36 1% 1/16W MF 402

R9104 36 1% 1/16W MF 402
RSDM3 H11 USB_NEC_N<2>
DM3 G11 (USB2_N<2>) USB2_N<2> 5 6 59
DP3 G13 (USB2_P<2>) USB2_P<2> 5 6 59
RSDP3 G14 USB_NEC_P<2>

R9105 36 1% 1/16W MF 402

R9106 36 1% 1/16W MF 402
RSDM4 F12 USB_NEC_N<3>
DM4 F14 (USB2_N<3>) USB2_N<3> 5 6 59
DP4 E12 (USB2_P<3>) USB2_P<3> 5 6 59
RSDP4 E14 USB_NEC_P<3>

R9107 36 1% 1/16W MF 402

R9108 36 1% 1/16W MF 402
RSDM5 E13 USB_NEC_N<4>
DM5 D14 (USB2_N<4>) USB2_N<4> 5 6 59
DP5 C13 (USB2_P<4>) USB2_P<4> 5 6 59
RSDP5 C14 USB_NEC_P<4>

R9109 36 1% 1/16W MF 402

Master: Fizzy

USB Host Interfaces

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 91 OF 103	

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:38 2004

Page Notes

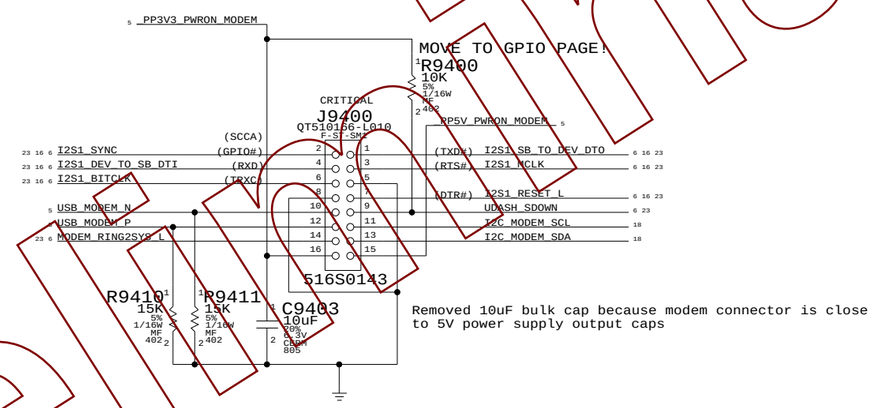
Power aliases required by this page:
- _PP3V3_PWRON_MODEM
  Spec Load: 0.5 A active, 3 mA auxiliary

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Modem Connector

Supports both The Last Dash and Q52 Modems



Removed 10uF bulk cap because modem connector is close to 5V power supply output caps

Modem Interface

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT
NONE	94 OF 103

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:46 2004

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_AUDIO
- _PP3V3_PWRON_AUDIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: It is considered the responsibility of the audio section to provide the appropriate pull-ups and pull-downs for ALL audio GPIOs.

EMI Filtering

L9530 FERR-220-OHM 0402
23 I2S0_SYNC 1 2 I2S0_SYNC_F 6 61

L9531 FERR-220-OHM 0402
23 I2S0_MCLK 1 2 I2S0_MCLK_F 6 61

L9532 FERR-220-OHM 0402
23 I2S0_DEV_TO_SB_DTI 1 2 I2S0_DEV_TO_SB_DTI_F 6 61

L9533 FERR-220-OHM 0402
23 I2S0_SB_TO_DEV_DTO 1 2 I2S0_SB_TO_DEV_DTO_F 6 61

L9534 FERR-220-OHM 0402
23 6 AUDIO_SPKR_MUTE_L 1 2 AUDIO_SPKR_MUTE_L_F 61

L9535 FERR-220-OHM 0402
23 I2S0_RESET_L 1 2 I2S0_RESET_L_F 6 61

L9536 FERR-220-OHM 0402
23 I2S0_BITCLK 1 2 I2S0_BITCLK_F 6 61

L9537 FERR-220-OHM 0402
23 I2S2_SYNC 1 2 I2S2_SYNC_F 6 61

L9538 FERR-220-OHM 0402
23 I2S2_BITCLK 1 2 I2S2_BITCLK_F 6 61

L9539 FERR-220-OHM 0402
23 I2S2_DEV_TO_SB_DTI 1 2 I2S2_DEV_TO_SB_DTI_F 6 61

L9540 FERR-220-OHM 0402
23 I2S2_RESET_L 1 2 I2S2_RESET_L_F 6 61

Sound Board Connector

Place shorts at 3.3V and 5V regulators

XW9505 SM
5 PP5V_PWRON_AUDIO 2 1 6 PP5V_PWRON_AUDIO
VOLTAGE=5V
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil
This is an internal board short

CRITICAL
J9500 QT500406-L111 M-ST-SM1
41 42
1 2 3 4 5 6 7 8 9 10 11 12
5 PP5V_RUN_AUDIO
23 6 AUDIO_GPIO_11 13 14 AUDIO_LO_DET_L 6 23
15 16 AUDIO_LO_OPTICAL_PLUG_L 6 23
23 6 AUDIO_EXT_MCLK_SEL 17 18 AUDIO_LI_DET_L 6 23
23 6 AUDIO_LO_MUTE_L 19 20 AUDIO_LI_OPTICAL_PLUG_L 6 23
21 22 AUDIO_SPKR_MUTE_L_F 61
61 6 I2S0_MCLK_F 23 24
61 6 I2S0_BITCLK_F 25 26 I2S0_RESET_L_F 6 61
61 6 I2S0_SYNC_F 27 28 I2S2_RESET_L_F 61
61 6 I2S0_SB_TO_DEV_DTO_F 29 30
61 6 I2S0_DEV_TO_SB_DTI_F 31 32 I2C_AUDIO_SDA 18
33 34 I2C_AUDIO_SCL 18
61 6 I2S2_BITCLK_F 35 36
61 6 I2S2_SYNC_F 37 38 SLEEPLED_ANODE 6 19
6 I2S2_DEV_TO_SB_DTI_F 39 40 (SLEEP_LED_GND)
43 44
516S0154

Place shorts at 3.3V and 5V regulators

XW9503 SM
6 PP3V3_PWRON_AUDIO 2 1 PP3V3_PWRON_AUDIO 61
VOLTAGE=3.3V
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil
This is an internal board short

Place ground short near 3.3V and 5V regulators

XW9500 SM
6 GND_AUDIO 2 1
VOLTAGE=0V
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil
This is an internal board short

Audio GPIO Pull-ups & Pull-downs

61 5 PP3V3_PWRON_AUDIO

AUDIO_LO_DET_L - 100k PU on Kazoo (pg 6)
AUDIO_LO_OPTICAL_PLUG_L - 100k PU on Kazoo (pg 6)
AUDIO_LI_DET_L - 100k PU on Kazoo (pg 7)
AUDIO_LI_OPTICAL_PLUG_L - 100k PU on Kazoo (pg 8)

23 AUDIO_HP_DET_L — R9504 10K 5% 1/16W MF 402 — NO STUFF
23 AUDIO_SPKR_DET_L — R9515 10K 5% 1/16W MF 402 — R9505 10K 5% 1/16W MF 402

AUDIO_LO_MUTE_L - 100k PD on Kazoo (pg 6)

23 AUDIO_HP_MUTE_L — R9507 10K 5% 1/16W MF 402

AUDIO_SPKR_MUTE_L - 100k PD on Kazoo (pg 5)
AUDIO_EXT_MCLK_SEL - 100k PD on Kazoo (pg 8)
AUDIO_GPIO_11 - 100k PD on Kazoo (pg 8)

23 AUDIO_GPIO_12 — R9511 10K 5% 1/16W MF 402

I2S0_RESET_L - 100k PD on Kazoo (pg 4)
I2S2_RESET_L - 100k PD on Kazoo (pg 8)

DRAWING
TITLE=LINK
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:54 2004

Audio Interface

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 95 OF 103	

Electrical Constraints

No series termination on PCI signals

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
	RAM_CAD		RAM_DQS_R<15..0>	33 34
	RAM_CAD		RAM_DQ_R<127..0>	33 34
RAM_DQS0	RAM_CAD		RAM_DQS<0>	34 35
RAM_DQS0	RAM_CAD		RAM_DQ<7..0>	34 35
RAM_DQS1	RAM_CAD		RAM_DQS<1>	34 35
RAM_DQS1	RAM_CAD		RAM_DQ<15..8>	34 35
RAM_DQS2	RAM_CAD		RAM_DQS<2>	34 35
RAM_DQS2	RAM_CAD		RAM_DQ<23..16>	34 35
RAM_DQS3	RAM_CAD		RAM_DQS<3>	34 35
RAM_DQS3	RAM_CAD		RAM_DQ<31..24>	34 35
RAM_DQS4	RAM_CAD		RAM_DQS<4>	34 35
RAM_DQS4	RAM_CAD		RAM_DQ<39..32>	34 35
RAM_DQS5	RAM_CAD		RAM_DQS<5>	34 35
RAM_DQS5	RAM_CAD		RAM_DQ<47..40>	34 35
RAM_DQS6	RAM_CAD		RAM_DQS<6>	34 35
RAM_DQS6	RAM_CAD		RAM_DQ<55..48>	34 35
RAM_DQS7	RAM_CAD		RAM_DQS<7>	34 35
RAM_DQS7	RAM_CAD		RAM_DQ<63..56>	34 35
RAM_DQS8	RAM_CAD		RAM_DQS<8>	34 35
RAM_DQS8	RAM_CAD		RAM_DQ<71..64>	34 35
RAM_DQS9	RAM_CAD		RAM_DQS<9>	34 35
RAM_DQS9	RAM_CAD		RAM_DQ<79..72>	34 35
RAM_DQS10	RAM_CAD		RAM_DQS<10>	34 35
RAM_DQS10	RAM_CAD		RAM_DQ<87..80>	34 35
RAM_DQS11	RAM_CAD		RAM_DQS<11>	34 35
RAM_DQS11	RAM_CAD		RAM_DQ<95..88>	34 35
RAM_DQS12	RAM_CAD		RAM_DQS<12>	34 35
RAM_DQS12	RAM_CAD		RAM_DQ<103..96>	34 35
RAM_DQS13	RAM_CAD		RAM_DQS<13>	34 35
RAM_DQS13	RAM_CAD		RAM_DQ<111..104>	34 35
RAM_DQS14	RAM_CAD		RAM_DQS<14>	34 35
RAM_DQS14	RAM_CAD		RAM_DQ<119..112>	34 35
RAM_DQS15	RAM_CAD		RAM_DQS<15>	34 35
RAM_DQS15	RAM_CAD		RAM_DQ<127..120>	34 35

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
	RAM_CLK	RAM_CLK_A_R	RAM_CLK_A_P_R	33 34
	RAM_CLK	RAM_CLK_A_R	RAM_CLK_A_N_R	33 34
	RAM_CLK	RAM_CLK_B_R	RAM_CLK_B_P_R	33 34
	RAM_CLK	RAM_CLK_B_R	RAM_CLK_B_N_R	33 34
	RAM_CLK	RAM_CLK_D_R	RAM_CLK_D_P_R	33 34
	RAM_CLK	RAM_CLK_D_R	RAM_CLK_D_N_R	33 34
	RAM_CLK	RAM_CLK_E_R	RAM_CLK_E_P_R	33 34
	RAM_CLK	RAM_CLK_E_R	RAM_CLK_E_N_R	33 34
RAM_CLK0	RAM_CLK	RAM_CLK_A	RAM_CLK_A_P	34 35
RAM_CLK0	RAM_CLK	RAM_CLK_A	RAM_CLK_A_N	34 35
RAM_CLK0	RAM_CLK	RAM_CLK_B	RAM_CLK_B_P	34 35
RAM_CLK0	RAM_CLK	RAM_CLK_B	RAM_CLK_B_N	34 35
RAM_CLK1	RAM_CLK	RAM_CLK_D	RAM_CLK_D_P	34 35
RAM_CLK1	RAM_CLK	RAM_CLK_D	RAM_CLK_D_N	34 35
RAM_CLK1	RAM_CLK	RAM_CLK_E	RAM_CLK_E_P	34 35
RAM_CLK1	RAM_CLK	RAM_CLK_E	RAM_CLK_E_N	34 35
	RAM_CAD		RAM_CKE_R<1..0>	33 34
	RAM_CAD		RAM_CKE_R<5..4>	33 34
RAM_CKE0	RAM_CAD		RAM_CKE<0>	34 35
RAM_CKE0	RAM_CAD		RAM_CKE<1>	34 35
RAM_CKE1	RAM_CAD		RAM_CKE<4>	34 35
RAM_CKE1	RAM_CAD		RAM_CKE<5>	34 35
	RAM_CAD		RAM_CS_L_R<1..0>	33 34
	RAM_CAD		RAM_CS_L_R<9..8>	33 34
RAM_CS0	RAM_CAD		RAM_CS_L<0>	34 35
RAM_CS0	RAM_CAD		RAM_CS_L<1>	34 35
RAM_CS1	RAM_CAD		RAM_CS_L<8>	34 35
RAM_CS1	RAM_CAD		RAM_CS_L<9>	34 35
	RAM_CAD		RAM_A_R<13..0>	33 34
	RAM_CAD		RAM_BA_R<1..0>	33 34 62
	RAM_CAD		RAM_RAS_L_R	33 34 62
	RAM_CAD		RAM_CAS_L_R	33 34 62
	RAM_CAD		RAM_WE_L_R	33 34 62
RAM_A_CTL	RAM_CAD		RAM_A<13..0>	34 35
RAM_A_CTL	RAM_CAD		RAM_BA_R<1..0>	33 34 62
RAM_A_CTL	RAM_CAD		RAM_RAS_L_R	33 34 62
RAM_A_CTL	RAM_CAD		RAM_CAS_L_R	33 34 62
RAM_A_CTL	RAM_CAD		RAM_WE_L_R	33 34 62

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
	TMDS	TMDS_D0	TMDS_DP<0>	6 41 42
	TMDS	TMDS_D0	TMDS_DN<0>	6 41 42
	TMDS	TMDS_D1	TMDS_DP<1>	6 41 42
	TMDS	TMDS_D1	TMDS_DN<1>	6 41 42
	TMDS	TMDS_D2	TMDS_DP<2>	6 41 42
	TMDS	TMDS_D2	TMDS_DN<2>	6 41 42
	TMDS	TMDS_CLK	TMDS_CLKP	41 42
	TMDS	TMDS_CLK	TMDS_CLKN	41 42
	TMDS	TMDS_D3	TMDS_DP<3>	41 42
	TMDS	TMDS_D3	TMDS_DN<3>	41 42
	TMDS	TMDS_D4	TMDS_DP<4>	41 42
	TMDS	TMDS_D4	TMDS_DN<4>	41 42
	TMDS	TMDS_D5	TMDS_DP<5>	41 42
	TMDS	TMDS_D5	TMDS_DN<5>	41 42
	TMDS	CONN_TMDS_D0	TMDS_CONN_DP<0>	42
	TMDS	CONN_TMDS_D0	TMDS_CONN_DN<0>	42
	TMDS	CONN_TMDS_D1	TMDS_CONN_DP<1>	42
	TMDS	CONN_TMDS_D1	TMDS_CONN_DN<1>	42
	TMDS	CONN_TMDS_D2	TMDS_CONN_DP<2>	42
	TMDS	CONN_TMDS_D2	TMDS_CONN_DN<2>	42
	TMDS	CONN_TMDS_CLK	TMDS_CONN_CLKP	6 42
	TMDS	CONN_TMDS_CLK	TMDS_CONN_CLKN	6 42
	TMDS	CONN_TMDS_D3	TMDS_CONN_DP<3>	42
	TMDS	CONN_TMDS_D3	TMDS_CONN_DN<3>	42
	TMDS	CONN_TMDS_D4	TMDS_CONN_DP<4>	42
	TMDS	CONN_TMDS_D4	TMDS_CONN_DN<4>	42
	TMDS	CONN_TMDS_D5	TMDS_CONN_DP<5>	42
	TMDS	CONN_TMDS_D5	TMDS_CONN_DN<5>	42
	TMDS	SI_TMDS_D0	SI_TMDS_DP<0>	41
	TMDS	SI_TMDS_D0	SI_TMDS_DN<0>	41
	TMDS	SI_TMDS_D1	SI_TMDS_DP<1>	41
	TMDS	SI_TMDS_D1	SI_TMDS_DN<1>	41
	TMDS	SI_TMDS_D2	SI_TMDS_DP<2>	41
	TMDS	SI_TMDS_D2	SI_TMDS_DN<2>	41
	TMDS	SI_TMDS_CLK	SI_TMDS_CLKP	41
	TMDS	SI_TMDS_CLK	SI_TMDS_CLKN	41
	TMDS	SI_TMDS_D3	SI_TMDS_DP<3>	41
	TMDS	SI_TMDS_D3	SI_TMDS_DN<3>	41
	TMDS	SI_TMDS_D4	SI_TMDS_DP<4>	41
	TMDS	SI_TMDS_D4	SI_TMDS_DN<4>	41
	TMDS	SI_TMDS_D5	SI_TMDS_DP<5>	41
	TMDS	SI_TMDS_D5	SI_TMDS_DN<5>	41
	TMDS	GPU_TMDS_D0	GPU_TMDS_DP<0>	39 41
	TMDS	GPU_TMDS_D0	GPU_TMDS_DN<0>	39 41
	TMDS	GPU_TMDS_D1	GPU_TMDS_DP<1>	39 41
	TMDS	GPU_TMDS_D1	GPU_TMDS_DN<1>	39 41
	TMDS	GPU_TMDS_D2	GPU_TMDS_DP<2>	39 41
	TMDS	GPU_TMDS_D2	GPU_TMDS_DN<2>	39 41
	TMDS	GPU_TMDS_CLK	GPU_TMDS_CLKP	39 41
	TMDS	GPU_TMDS_CLK	GPU_TMDS_CLKN	39 41
	TMDS	GPU_TMDS_D0_R	GPU_TMDS_DP_R<0>	41
	TMDS	GPU_TMDS_D0_R	GPU_TMDS_DN_R<0>	41
	TMDS	GPU_TMDS_D1_R	GPU_TMDS_DP_R<1>	41
	TMDS	GPU_TMDS_D1_R	GPU_TMDS_DN_R<1>	41
	TMDS	GPU_TMDS_D2_R	GPU_TMDS_DP_R<2>	41
	TMDS	GPU_TMDS_D2_R	GPU_TMDS_DN_R<2>	41
	TMDS	GPU_TMDS_CLK_R	GPU_TMDS_CLKP_R	41
	TMDS	GPU_TMDS_CLK_R	GPU_TMDS_CLKN_R	41

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
			EI_CPU_TO_NB_CLK_P	26 27
			EI_CPU_TO_NB_CLK_N	26 27
			EI_NB_TO_CPU_CLK_P	26 27
			EI_NB_TO_CPU_CLK_N	26 27
			EI_CPU_TO_NB_AD<43..0>	26 27
			EI_NB_TO_CPU_AD<43..0>	26 27
			EI_CPU_TO_NB_SR_P<0>	26 27
			EI_CPU_TO_NB_SR_N<0>	26 27
			EI_CPU_TO_NB_SR_P<1>	26 27
			EI_CPU_TO_NB_SR_N<1>	26 27
			EI_NB_TO_CPU_SR_P<0>	26 27
			EI_NB_TO_CPU_SR_N<0>	26 27
			EI_NB_TO_CPU_SR_P<1>	26 27
			EI_NB_TO_CPU_SR_N<1>	26 27

45	PCI_SB_AD<0>	ALTAS	PCI_AD<0> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<1>	ALTAS	PCI_AD<1> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<2>	ALTAS	PCI_AD<2> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<3>	ALTAS	PCI_AD<3> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<4>	ALTAS	PCI_AD<4> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<5>	ALTAS	PCI_AD<5> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<6>	ALTAS	PCI_AD<6> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<7>	ALTAS	PCI_AD<7> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<8>	ALTAS	PCI_AD<8> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<9>	ALTAS	PCI_AD<9> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<10>	ALTAS	PCI_AD<10> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<11>	ALTAS	PCI_AD<11> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<12>	ALTAS	PCI_AD<12> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<13>	ALTAS	PCI_AD<13> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<14>	ALTAS	PCI_AD<14> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<15>	ALTAS	PCI_AD<15> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<16>	ALTAS	PCI_AD<16> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<17>	ALTAS	PCI_AD<17> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<18>	ALTAS	PCI_AD<18> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<19>	ALTAS	PCI_AD<19> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<20>	ALTAS	PCI_AD<20> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<21>	ALTAS	PCI_AD<21> MAKE_BASE=TRUE	6 45 47 48 49
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45	PCI_SB_AD<23>	ALTAS	PCI_AD<23> MAKE_BASE=TRUE	6 45 47 48 49
45	PCI_SB_AD<24>	ALTAS	PCI_AD<24> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<25>	ALTAS	PCI_AD<25> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<26>	ALTAS	PCI_AD<26> MAKE_BASE=TRUE	6 45 46 47 48 49
48 45	PCI_SB_AD<27>	ALTAS	PCI_AD<27> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<28>	ALTAS	PCI_AD<28> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<29>	ALTAS	PCI_AD<29> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<30>	ALTAS	PCI_AD<30> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_AD<31>	ALTAS	PCI_AD<31> MAKE_BASE=TRUE	6 45 46 47 48 49
45	PCI_SB_CBE_L<0>	ALTAS	PCI_CBE_L<0> MAKE_BASE=TRUE	6 45 47 48 49
45	PCI_SB_CBE_L<1>	ALTAS	PCI_CBE_L<1> MAKE_BASE=TRUE	6 45 47 48 49
45	PCI_SB_CBE_L<2>	ALTAS	PCI_CBE_L<2> MAKE_BASE=TRUE	6 45 47 48 49
45	PCI_SB_CBE_L<3>	ALTAS	PCI_CBE_L<3> MAKE_BASE=TRUE	6 45 47 48 49
45	PCI_SB_DEVSEL_L		PCI_DEVSEL_L MAKE_BASE=TRUE	6 45 47 48 49
45	PCI_SB_FRAME_L		PCI_FRAME_L MAKE_BASE=TRUE	6 45 47 48 49
45	PCI_SB_IRDY_L		PCI_IRDY_L MAKE_BASE=TRUE	6 45 47 48 49
45	PCI_SB_TRDY_L		PCI_TRDY_L MAKE_BASE=TRUE	6 45 47 48 49
45	PCI_SB_STOP_L		PCI_STOP_L MAKE_BASE=TRUE	6 45 47 48 49
45	PCI_SB_PAR		PCI_PAR MAKE_BASE=TRUE	6 45 47 48 49

_DRAWING
TITLE=LINK
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 18:36:43 2004

Electrical Constraints

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 99 OF 103	

*** Signal Cross-Reference for the entire design ***

1V2PWRON_ITH 9B6<>
1V2PWRON_ITH_RC 9A7<
1V2PWRON_MODE 9A6<>
1V2PWRON_PGOOD 9B4<>
1V2PWRON_RT 9B6<
1V2PWRON_RUNSS 9B6<>
1V2PWRON_SGND 9A6<>
1V2PWRON_SW 9B4<>
1V2PWRON_VFB 9A5<>
1V2PWRON_VFB_DIV 9A5<
1V2RUN_EN 9A2<> 14C6<
1V5PWRON_SW 9C5<>
1V5PWRON_VFB_DIV 9B5<
1V5RUN_EN 9C2<> 14C6<
1V8RUN_CC 9D5<>
1V8RUN_PGOOD 9D5<> 14B8<
1V8RUN_SHDN_L 9D6<> 14B6<
2V5NBVCORE_STBY_L 11C3< 14D6<
2V5PWRON_SW 11C3<>
2V5RUN_EN_L 11D2<> 14C6<
2V5_BOOST_ESR 11C3<>
2V5_BST_HI 11C4<>
2V5_BST_LO 11C4<>
2V5_FB 11C4<>
2V5_FB_RC 11B2<
2V5_HI_GATE 11C4<>
2V5_INV 11C4<
2V5_INV_RC 11C1<
2V5_ITRIP 11C4<
2V5_LO_GATE 11C4<>
2V5_NBVCORE_CT 11C4<>
2V5_NBVCORE_FLT 11C4<>
2V5_NBVCORE_PGOOD 11B4<> 14B8<
2V5_NBVCORE_PWM 11B5<
2V5_NBVCORE_REF 11C4<>
2V5_NBVCORE_VCC 11D3<
2V5_NBVCORE_VREF5 11D5<>
2V5_SS 11C4<>
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3V3ALL_FB 11A4<
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3V3PWRON_FB 10C4<>
3V3PWRON_FB_RC 10C2<
3V3PWRON_INV 10C4<
3V3PWRON_INV_RC 10C2<
3V3PWRON_LH 10C4<>
3V3PWRON_LL 10C4<>
3V3PWRON_OUT_D 10C4<>
3V3PWRON_OUT_U 10C4<>
3V3PWRON_SS 10C4<>
3V3PWRON_SW 10C2<>
3V3PWRON_TRIP 10C4<
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3V3_STBY_L 10D4< 14D6<
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4V85ALL_FB 11A6<
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5V3VPWRON_FLT 10C4<>
5V3VPWRON_PGOOD 10C5<> 14B8<
5V3VPWRON_REF 10C4<>
5V3VPWRON_SKIP 10C5<
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5VRUN_EN_L 10A6<> 14D5<
5V_STBY_L 10D5< 14D4<
ACIN_1V20_REF 7C6<
ACIN_DIV 7C6<
ACIN_ENABLE_L 7C3<>
ACIN_ENABLE_L_DIV 7D3<>
ADAPTER_ID 6A3> 17D7<>
ADAPTER_PD 7C6<
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AGP_AD_STBS<1> 36C7<> 36D3< 37D6<>
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AGP_ATI_VREFG 37B7<
AGP_BUSY_L 36C3<> 37D6<
AGP_BUSY_L_F 36C2<>
AGP_CBE<0> 36D7<> 37B7<>
AGP_CBE<1..0> 36D3<
AGP_CBE<1> 36D7<> 37B7<>
AGP_CBE<2> 36C7<> 37B7<>
AGP_CBE<3..2> 36D3<
AGP_CBE<3> 36C7<> 37C7<>
AGP_CLK66M_GPU 25B1< 25D8< 37B7<
AGP_CLK66M_GPU_R 25B4<>
AGP_CLK66M_NB 25B1< 25D8< 36B4<>
AGP_CLK66M_NB_R 25B4<>
AGP_DBI_HI 36C7<> 36D3< 37C6<>
AGP_DBI_LO 36D3< 36D7<> 37C6<>
AGP_DEVSEL 36B7<> 37B7<>
AGP_FRAME 36B7<> 37B7<>
AGP_GNT 36B7> 37B7<
AGP_INT_L 23B3<> 37B7<>
AGP_IRDY 36B7<> 37B7<>
AGP_PAR 36B7<> 37B7>
AGP_PVTREF1 36B5<>
AGP_PVTREF2 36B5<>
AGP_RBF 36B7< 37C6>
AGP_REQ 36B7< 37B7<>
AGP_SBA_L<0> 36C4< 37C6>
AGP_SBA_L<7..0> 36D3<
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AGP_SB_STBS 36C7< 36D3< 37C6<>
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AGP_ST<1> 36B7> 37C6<
AGP_ST<2> 36B7> 37C6<
AGP_STOP 36B7<> 37B7<>
AGP_SUS_STAT_L_PU 37C6<
AGP_TRDY 36B7<> 37B7<>
AGP_TYPEDET_L 36B7< 37D5<
AGP_VREF_GC 36B4<> 37D5< 37D7<

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AIRPORT_CLKRUN_L_PD 6A8> 47B5<>
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ALS1_GAIN_BOOST_L 19C7<>
ALS1_OP_IN 19D8<
ALS1_OUT 13A7> 19D5<
ALS1_OUT_DIV 19C7<
ALS1_OUT_R 19D7<>
ALS1_PHOTODIODE 19C8<>
ALS_GAIN_BOOST 6A3> 13A7> 17D6<> 19C7<>
ATI_DVOVMODE 40A3<
ATI_RSTB_MSK 37C6<>
AUDIO_EXT_MCLK_SEL 6C2> 23A3<> 61C5<>
AUDIO_GPIO_11 6C2> 23A3<> 61C5<>
AUDIO_GPIO_12 23A3<> 61B2<
AUDIO_HP_DET_L 23B3<> 61C2<
AUDIO_HP_MUTE_L 23A3<> 61B2<
AUDIO_LI_DET_L 6C2> 23B3<> 61C4<>
AUDIO_LI_OPTICAL_PLUG_L 6C2> 23B3<> 61C4<>
AUDIO_LO_DET_L 6C2> 23B3<> 61C4<>
AUDIO_LO_MUTE_L 6C2> 23A3<> 61C5<>
AUDIO_LO_OPTICAL_PLUG_L 6C2> 23B3<> 61C4<>
AUDIO_SPKR_DET_L 23A3<> 61C2<
AUDIO_SPKR_MUTE_L 6C2> 23A3<> 61C8<
AUDIO_SPKR_MUTE_L_F 61C4<> 61C7<
AVPRESET_L 27B8<> 28B3<
BATT_ACIN_L_RC 8B2<>
BATT_DET_L 6A5> 7A7<>
BATT_PBUSA_EN_L 8B2<>
BATT_PBUSB_EN_L 8C2<>
BATT_PBUS_EN_L 8B2<>
BIMODE_L 27B8<> 28C7<
BKFD_PROT_EN_L 8D8<>
BKFD_PROT_EN_L_DIV 8D8<>
BRIGHT_PWM 6A7> 42A2<>
BRIGHT_PWM_UF 42A2<>
BUSCFG0 27B6<> 28B3<
BUSCFG1 27B6<> 28B3<
BUSCFG2 27B6<> 28B3<
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C2UNDGLOBAL 27B8<> 28C8<
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CBUS_CE1_L 49C1<> 49C3>
CBUS_CE2_L 49B2<> 49B3>
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CBUS_DATA<14> 49A3<> 49C2<>
CBUS_DATA<15> 49A3<> 49C2<>
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CBUS_DET_2_L 49A2<> 49C3<
CBUS_INPACK_L 49B2<> 49B3<
CBUS_IORD_L 49B2<> 49C3>
CBUS_IOWR_L 49B2<> 49C3>
CBUS_MFUNC1_PD 49A6<>
CBUS_MFUNC2_PD 49A6<>
CBUS_MFUNC3_PD 49A6<>
CBUS_MFUNC4_PD 49A6<>
CBUS_MFUNC5_PD 49A6<>
CBUS_MFUNC6_PD 49A6<>
CBUS_OE_L 49B1<> 49C3>
CBUS_PERR_L_PU 49B6<> 49C7<
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*** Part Cross-Reference for the entire design ***

BS510	PCB_STANDOFF	17
C700	CAP	7
C710	CAP	7
C720	CAP	7
C800	CAP	8
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J750	CON_M10RT_S_SM	7
J790	CON_F14RT_S2MT_SM	17
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J1600	CON_F14RT_S2MT_SM	17
J1699	CON_F16ST_D_SMA	16
J21[illegible]0	CON_F14RT_S2MT_SM	17
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J4010	CON_F200RT_DDRDIMM_SM1	35
J4020	CON_F200RT_DDRDIMM_SM2	35
J5900	CON_F30RT_T6MT_TH1	42
J5960	CON_F5RT_MINIDIN_TH	42
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APPLE COMPUTER INC.

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U2110 OPAMP_MAX4236EUTT 19
U2150 MAX1561   19
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U2600 PULSAR    24 25
U2900 GPUL      27 29
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	103	103