1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
C		397426	PRODUCTION RELEASED	08/30/05	?

SCHEM,MLB,PBG4 17"

8/23/2005

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8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	200PIN DDR MEMORY SODIMM CONNECTORS
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	M10 AGP & CLOCKS
19	M10 LVDS/TMDS/VGA/GPIO & GPU VCORE
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23	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
24	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
25	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
26	USB 2.0
27	MARVELL GIGABIT ETHERNET PHY
28	FIREWIRE A/B PHY
29	FIREWIRE A/B CONNECTORS, PORT POWER LIMITER
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41-42	SIGNAL NAMES
43-44	COMPONENT LOCATIONS

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS		✓
INT_TMDS	✓	
NO_4XVCORE	✓	
INT_CLK	✓	
EXT_CLK		✓

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6654	1	SCHEM,MLB,PBG4 17	SCH1	
820-1615	1	PCBF,MLB,PBG4 17	PCB1	
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:R94	LABEL_64MB
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:R95	LABEL_128MB

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PBG4 17"

DRAWING NUMBER 051-6654 REV. C

SHT 1 OF 44

U44 INTREPID

J18 Ethernet Connector P.28 — 4 DATA PAIRS — U49 Ethernet PHY P.28 — G/MII 3.3V 10/100/1000 8BIT TX 8BIT RX 125MHZ

J24 FW - A Connector P.30 — 2 DATA PAIRS @ 200MHz

J22 FW - B Connector P.30 — 2 DATA PAIRS @ 400MHZ

U28 FireWire PHY P.29 — 1394 OHCI 3.3V 8BIT TX/RX 100MHZ

J11 OPTICAL DRIVE Connector P.25 — EIDE

J13 ULTRA ATA/100 Connector P.25 — UIDE

SLEEP LED P.26 — LMU

J14 TUBA (SOUND) Connector P.26 — I2S, I2C

U48/J2/J4 Fan Circuit P.26 — I2C

J25 Battery Connector P.32 — SMBUS 3.3V

Power Supply & Charger P.32-36

J19 SUTRO (PWR) Connector P.32

U36 LMU P.24 — I2C

U39 PMU P.31 — SERIAL 5V

J10 CARDBUS Connector P.18 — 33MHZ 16/32 BITS 3.3V/5V

J15 TRACKPAD Connector; Keyboard Connector; KB LED LIGHT SENSOR P.24

U26 TI PCI1510 CardBus Controller P.18

U52 USB 2.0 CONTROLLER P.27

U17 BOOT ROM 1M X 8 P.10

J5 Serial Debug Connector P.26

NOT USED

ETHERNET 10/100/1000 P.14	FIREWIRE 800 MB/S P.14	UATA 100 P.14	EIDE P.14	CARDSLOT P.14	I2S P.15	I2C P.14 P.15
USB PORT A P.15					SCCA P.15	
USB PORT B P.15					VIA/PMU P.15	
USB PORT C P.15					BOOTROM P.14	
USB PORT D P.15					PCI 32BITS 33MHZ P.13	
USB PORT E P.15						
USB PORT F P.15						
MAXBUS P.9	DDR MEMORY P.10				4X AGP P.13	

J3 (SHARE WITH BLUETOOTH) LEFT USB P.25 — USB 2.0

J12 RIGHT USB BACKUP BATTERY P.33 — NOT USED — USB 2.0

J3 (SHARE WITH LEFT USB) BlueTooth P.25 — NOT USED

J9 Modem Board Connector P.26 — INTRPEID I2C

MAXBUS 1.8V 167MHZ 32BIT ADDRESS 64BIT DATA

U42 APOLLO CPU (MPC7457) P.5-6

CPU PLL Config P.7 — PMU

U11/U12/U13/U14 2:1 DDR MUXES P.11 — MEMORY BUS 2.5V 167MHZ 64BITS

J20/J23 DDR SDRAM DIMM 0; DDR SDRAM DIMM 1 SO-DIMM Connector P.12

AGP BUS 1.5V/3.3V 32BITS 66MHZ

U43 ATI M11 64MB P.18-21 — MEMORY CH. A (INTERNAL MEM); MEMORY CH. C (INTERNAL MEM); MEMORY CH. B (INTERNAL MEM); MEMORY CH. D (INTERNAL MEM)

J8 Inverter Connector P.22

LVDS; EDID (I2C); S-VIDEO; COMPOSITE; TMDS; RGB; (DDC TOO)

J7 LCD Panel Connector P.22

J17 S-Video Connector P.22

J16 DVI-I Connector P.22

PCI BUS 32BITS 33MHZ 3.3V

J21 AIRPOPT Connector P.25

SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6654 | REV. C

SCALE NONE | SHT 2 OF 44

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
U21 PG 31
>-13.44V TURNS-ON
<-13.44V SHUTS-OFF

RUN/SS
BUCK REGULATOR (LTC1625) PG 32
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN
VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER
+2.5V_MAIN
1_5V_2_5V_OK
+1.5V_MAIN
INTREPID CORE
AGP I/O

+PBUS

DCDC_EN
SLEEP
MAXBUS SEQUENCING

+5V_MAIN
VCC SHDN
DC/DC (MAX1717) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
CPU_VCORE (+1.4V/+1.5V)

14V_PBUS

+3V_PMU LDO PG 32
+BATT
+5V_MAIN
+3V_PMU
+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707) PG 33 STBYMD
VCC
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK
HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN
+3.3V_MAIN

+5V_MAIN
DCDC_EN_L
AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+PBUS (12.8V)
+5V_MAIN
EXT_VCC
VCC
DC/DC (LTC1778) PG 20
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS
GPU_VCORE +1.2V/+1.0V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING
1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER
1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT
1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS
BACKUP BATTERY
CHARGER INPUT & BOOST OUTPUT PG 32
12.8V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY
BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

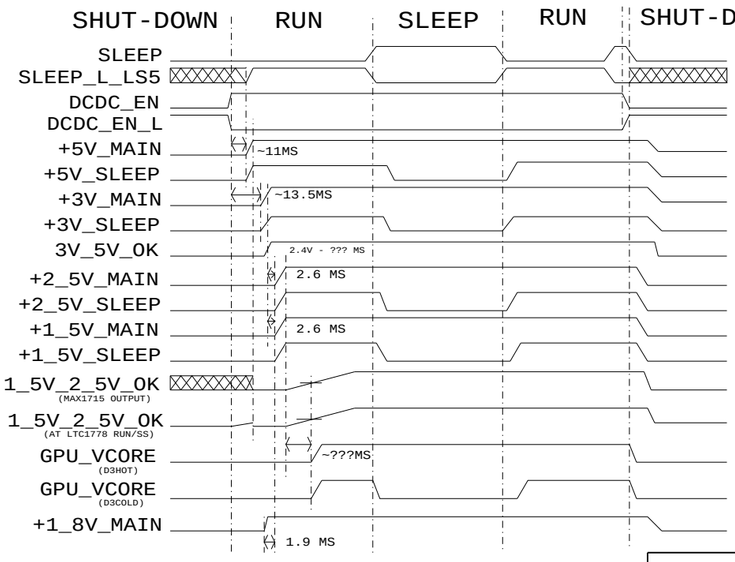
NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
+24V_PBUS

DC/DC (LTC3411) PG 35
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
+1.8V_MAIN
MAXBUS BROADCOM

BATTERY CHARGER (MAX1772) PG 31
+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
BATTERY VOLTAGE FEED-IN PATH PG 31
+PBUS



POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 3 OF 44	

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

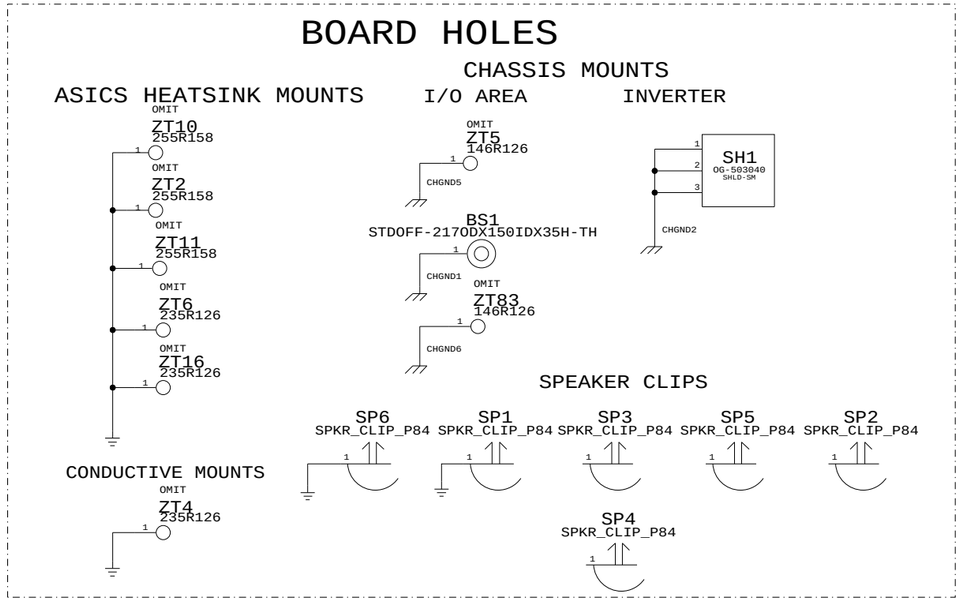
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

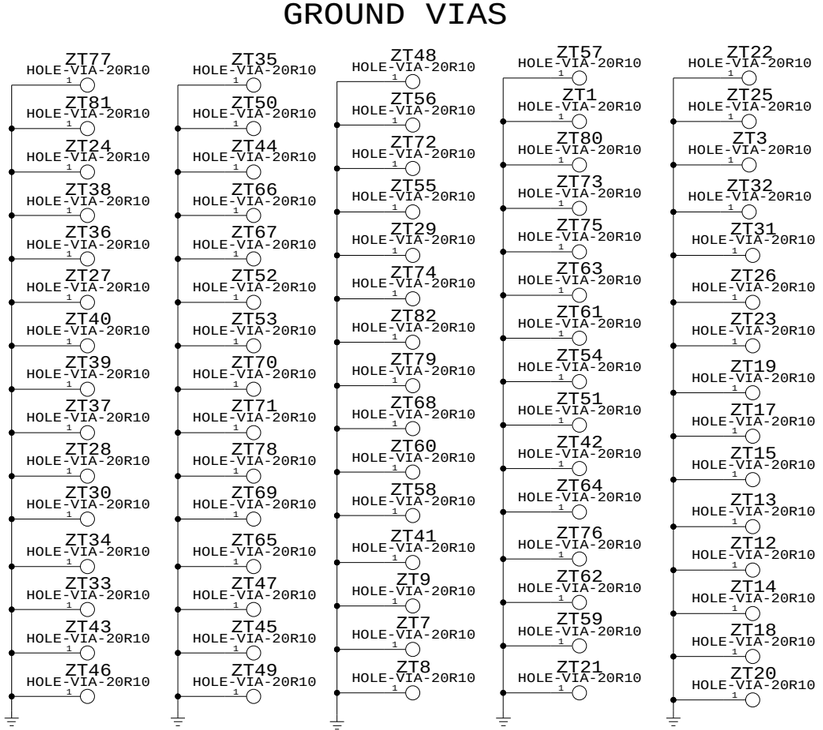
20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS



BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 4 OF 44	

CPU_VCORE DECOUPLING NETWORK

CPU_VCORE_SLEEP 5 6 34 38 39

R241 470 5% 1/16W MF 402

C25 10uF 20% 6.3V CERM 805 · C342 10uF 20% 6.3V CERM 805 · C344 10uF 20% 6.3V CERM 805

C346 10uF 20% 6.3V CERM 805 · C8 10uF 20% 6.3V CERM 805 · C153 0.1uF 20% 10V CERM 402

C12 2.2uF 20% 10V CERM 805 · C340 2.2uF 20% 10V CERM 805 · C193 0.1uF 20% 10V CERM 402

C223 0.1uF 20% 10V CERM 402 · C91 0.1uF 20% 10V CERM 402 · C114 0.1uF 20% 10V CERM 402 · C104 0.1uF 20% 10V CERM 402 · C103 0.1uF 20% 10V CERM 402 · C110 0.1uF 20% 10V CERM 402 · C190 0.1uF 20% 10V CERM 402 · C189 0.1uF 20% 10V CERM 402

C138 0.1uF 20% 10V CERM 402 · C191 0.1uF 20% 10V CERM 402 · C112 0.1uF 20% 10V CERM 402 · C168 0.1uF 20% 10V CERM 402 · C149 0.1uF 20% 10V CERM 402 · C111 0.1uF 20% 10V CERM 402 · C150 0.1uF 20% 10V CERM 402 · C105 0.1uF 20% 10V CERM 402

C154 0.1uF 20% 10V CERM 402 · C115 0.1uF 20% 10V CERM 402 · C113 0.1uF 20% 10V CERM 402 · C152 0.1uF 20% 10V CERM 402 · C151 0.1uF 20% 10V CERM 402 · C202 0.1uF 20% 10V CERM 402 · C201 0.1uF 20% 10V CERM 402 · C192 0.1uF 20% 10V CERM 402

MAXBUS_SLEEP 5 7 8 15 16 23 34 38

R206 470 5% 1/16W MF 402

CPU_OVDD DECOUPLING NETWORK

C72 0.1uF 20% 10V CERM 402 · C48 0.1uF 20% 10V CERM 402 · C38 0.1uF 20% 10V CERM 402 · C74 0.1uF 20% 10V CERM 402 · C275 0.1uF 20% 10V CERM 402 · C46 0.1uF 20% 10V CERM 402 · C47 0.1uF 20% 10V CERM 402 · C170 0.1uF 20% 10V CERM 402

C73 0.1uF 20% 10V CERM 402 · C39 0.1uF 20% 10V CERM 402 · C107 0.1uF 20% 10V CERM 402 · C90 0.1uF 20% 10V CERM 402 · C257 0.1uF 20% 10V CERM 402 · C272 0.1uF 20% 10V CERM 402 · C188 0.1uF 20% 10V CERM 402 · C155 0.1uF 20% 10V CERM 402 · C92 0.1uF 20% 10V CERM 402

C224 0.1uF 20% 10V CERM 402 · C40 0.1uF 20% 10V CERM 402 · C194 0.1uF 20% 10V CERM 402 · C203 0.1uF 20% 10V CERM 402 · C273 0.1uF 20% 10V CERM 402 · C41 0.1uF 20% 10V CERM 402 · C169 0.1uF 20% 10V CERM 402 · C139 0.1uF 20% 10V CERM 402 · C106 0.1uF 20% 10V CERM 402

MORE 0805 10UF CAPS ON VCORE POWER SUPPLY PAGE (PG 33)

PLCAE SHORT CLOSE TO CENTER OF CPU

XW31 SM

25 ADT7460_VCORE_MON 1 OMIT 2

C195 10UF 20% 6.3V CERM 805 · C347 10UF 20% 6.3V CERM 805 · C258 10UF 20% 6.3V CERM 805 · C345 10UF 20% 6.3V CERM 805

C156 10UF 20% 6.3V CERM 805 · C341 10UF 20% 6.3V CERM 805 · C225 10UF 20% 6.3V CERM 805 · C343 10UF 20% 6.3V CERM 805

PLACE BELOW CPU IN FORMER L3 AREA

H8 H10 H12 J7 J9 J11 J13 K8 K10 K12 K14 L7 L9 L11 L13 M8 M10 M12 — VDD

B4 C2 C12 D5 F2 H3 J5 K2 L5 M3 N6 P2 P8 P11 R4 R13 R16 T6 T9 U2 U12 U16 V4 V7 V10 V14 E18 G18 — OVDD

A8 AVDD

OVDDSENSE

36 8 CPU_BR_L	D2	BR*	
36 8 CPU_BG_L	M1	BG*	
NC	L4	TS*	
36 8 CPU_TS_L			
5 CPU_PULLDOWN	E11	A0	
	H1	A1	
	C11	A2	
	G3	A3	
36 8 CPU_ADDR<0>	F10	A4	
36 8 CPU_ADDR<1>	L2	A5	
36 8 CPU_ADDR<2>	D11	A6	
36 8 CPU_ADDR<3>	D1	A7	
36 8 CPU_ADDR<4>	C10	A8	
36 8 CPU_ADDR<5>	G2	A9	
36 8 CPU_ADDR<6>	D12	A10	
36 8 CPU_ADDR<7>	L3	A11	
36 8 CPU_ADDR<8>	G4	A12	
36 8 CPU_ADDR<9>	T2	A13	
36 8 CPU_ADDR<10>	F4	A14	
36 8 CPU_ADDR<11>	V1	A15	
36 8 CPU_ADDR<12>	J4	A16	
36 8 CPU_ADDR<13>	R2	A17	
36 8 CPU_ADDR<14>	K5	A18	
36 8 CPU_ADDR<15>	W2	A19	
36 8 CPU_ADDR<16>	J2	A20	
36 8 CPU_ADDR<17>	K4	A21	
36 8 CPU_ADDR<18>	N4	A22	
36 8 CPU_ADDR<19>	J3	A23	
36 8 CPU_ADDR<20>	M5	A24	
36 8 CPU_ADDR<21>	P5	A25	
36 8 CPU_ADDR<22>	N3	A26	
36 8 CPU_ADDR<23>	T1	A27	
36 8 CPU_ADDR<24>	V2	A28	
36 8 CPU_ADDR<25>	U1	A29	
36 8 CPU_ADDR<26>	N5	A30	
36 8 CPU_ADDR<27>	W1	A31	
36 8 CPU_ADDR<28>	B12	A32	
36 8 CPU_ADDR<29>	C4	A33	
36 8 CPU_ADDR<30>	G10	A34	
36 8 CPU_ADDR<31>	B11	A35	
NC	C1	AP0	
NC	E3	AP1	
NC	H6	AP2	
NC	F5	AP3	
NC	G7	AP4	
36 8 CPU_TT<0>	E5	TT0	
36 8 CPU_TT<1>	E6	TT1	
36 8 CPU_TT<2>	F6	TT2	
36 8 CPU_TT<3>	E9	TT3	
36 8 CPU_TT<4>	C5	TT4	
36 8 CPU_TBST_L	F11	TBST*	
36 8 CPU_TSIZ<0>	G6	TSIZ0	
36 8 CPU_TSIZ<1>	F7	TSIZ1	
36 8 CPU_TSIZ<2>	E7	TSIZ2	
36 8 CPU_GBL_L	E2	GBL*	
36 8 CPU_WT_L	D3	WT*	
36 8 CPU_CI_L	J1	CI*	
36 8 CPU_AACK_L	R1	AACK*	
36 8 CPU_ARTRY_L	N2	ARTRY*	
5 CPU_SHD0_L	E4	SHD0*	
5 CPU_SHD1_L	H5	SHD1*	
36 8 CPU_HIT_L	B2	HIT*	

CRITICAL

U43
1.50GHZ-1.28V
APOLL7_PM-R1.1
BGA
(1 OF 3)

BVSEL	B7	CPU_BUS_VSEL	7
SYSCLK	A10	SYSCLK_CPU	8 36
CLK_OUT	H2	CPU_CLKOUT_SPN	
PLL_CFG0	B8	CPU_PLL_CFG<0>	7
PLL_CFG1	C8	CPU_PLL_CFG<1>	7
PLL_CFG2	C7	CPU_PLL_CFG<2>	7
PLL_CFG3	D7	CPU_PLL_CFG<3>	7
PLL_CFG4	A7	CPU_PLL_CFG<4>	7
DBG*	M2	CPU_DBG_L	8 36
DRDY*	R3	CPU_DRDY_L	8 36
DTI0	G1	CPU_EDTI	5
DTI1	K1	CPU_DTI<0>	8 36
DTI2	P1	CPU_DTI<1>	8 36
DTI3	N1	CPU_DTI<2>	8 36
TDI	B9	JTAG_CPU_TDI	5 23 39
TDO	A4	JTAG_CPU_TDO_TP	39
TMS	F1	JTAG_CPU_TMS	5 23 39
TCK	C6	JTAG_CPU_TCK	5 23 39
TRST*	A5	JTAG_CPU_TRST_L	5 23 39
LSSD_MODE*	E8	CPU_LSSD_MODE	5
L1_TSTCLK	G8	CPU_L1TSTCLK	5
L2_TSTCLK	B3	CPU_L2TSTCLK	5
TA*	K6	CPU_TA_L	8 36
TEA*	L1	CPU_TEA_L	8 36
TBEN	E1	CPU_TBEN	5 8
QREQ*	P4	CPU_QREQ_L	8 36
QACK*	G5	CPU_QACK_L	8 36
CKSTP_IN*	A3		
CKSTP_OUT*	B1	CPU_CHKSTP_OUT_L	5 39
INT*	D4	MPIC_CPU_INT_L	5 14
SMI*	F9	CPU_SMI_L	5 30
MCP*	C9	CPU_MCP_L	5
SRESET*	A2	CPU_SRESET_L	5 39
HRESET*	D8	CPU_HRESET_L	5 7 23 39
PMON_IN*	D9	CPU_PMONIN_L	5
PMON_OUT*	A9	NC	
BMODE0*	G9	CPU_EMODE0_L	7
BMODE1*	F8	CPU_EMODE1_L	5
EXT_QUAL	A11	CPU_PULLDOWN	5
CHKS*	A12	CPU_CHKS_L	5
SRW0*	B10	CPU_PULLUP	5
SRW1*	E10	CPU_SRWX_L	5
IARTRY0*	B6	CPU_PULLUP	5
DX*	D10	CPU_PULLDOWN	5

GND

B5 C3 D6 D13 E17 F3 G17 H4 H7 H9 H11 H13 J6 J8 J10 J12 K7 K9 K11 K13 L6 L8 L10 L12 M4 M7 M9 M11 M13 N7 P3 P9 P12 R5 R14 R17 T7 T10 U3 U13 U17 V5 V8 V11 V15

NO STUFF

R106 10 1% 1/16W MF 402 — 38 CPU_AVDD — 1 — 2 CPU_VCORE_SLEEP 5 6 34 38 39

C137 0.1uF 20% 10V CERM 402 · C136 4.7UF 20% 6.3V CERM 805

R280 10 1% 1/16W MF 402 — CPU_AVDD_VOUT

VOUT = 0.59*(1+R1/R2)
PLACE_R3XX AND R4XX CLOSE TO U3X PIN 5 AND 6

+3V_SLEEP

R276 0 5% 1/16W MF 603

R275 47K 5% 1/16W MF 402

CRITICAL

U6 FAN2558 SOT23-6

CPU_AVDD_VIN	1	VIN	VOUT 6
CPU_AVDD_PG	4	PG	
VCORE_SHDN_L 34	3	EN	ADJ 5 — CPU_AVDD_ADJ
	2	GND	

R282 63.4K 1% 1/16W MF 402

R283 52.3K 1% 1/16W MF 402

C283 2.2UF 20% 6.3V CERM1 603

C909 1UF 10% 6.3V CERM 402

CPU INTERNAL PLL FILTERING

MAXBUS_SLEEP 5 7 8 15 16 23 34 38

BBANG

R86 470 5% 1/16W MF 402

470OHM FOR BOOT BANGER

39 23 5 JTAG_CPU_TRST_L

NO_BBANG

R85 200 5% 1/16W MF 402

+1_5V_SLEEP — 1_5V_MAXBUS — R702 0 5% 1/16W MF 603

+1_8V_SLEEP — 1_8V_MAXBUS — R693 0 5% 1/16W MF 603

MPC7447 PULL-UPS

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

8 5 CPU_TBEN	R58	10K
5 CPU_CHKS_L	R160	10K
5 CPU_SHD0_L	R73	10K
5 CPU_SHD1_L	R87	10K
5 CPU_MCP_L	R139	10K
5 CPU_LSSD_MODE	R108	10K
5 CPU_L2TSTCLK	R72	10K
39 5 CPU_CHKSTP_OUT_L	R57	1K
5 CPU_SRWX_L	R148	10K
5 CPU_PMONIN_L	R120	10K
5 CPU_EMODE1_L	R109	10K
5 CPU_PULLUP	R98	1K
39 23 7 5 CPU_HRESET_L	R107	10K
30 5 CPU_SMI_L	R129	10K
39 23 5 JTAG_CPU_TMS	R59	470
39 23 5 JTAG_CPU_TDI	R128	470
14 5 MPIC_CPU_INT_L	R79	10K
39 5 CPU_SRESET_L	R65	10K
5 CPU_L1TSTCLK	R130	10K
5 CPU_EDTI	R60	10K
39 23 5 JTAG_CPU_TCK	R97	10K
5 CPU_PULLDOWN	R61	470

470OHM FOR BOOT BANGER

470OHM FOR BOOT BANGER

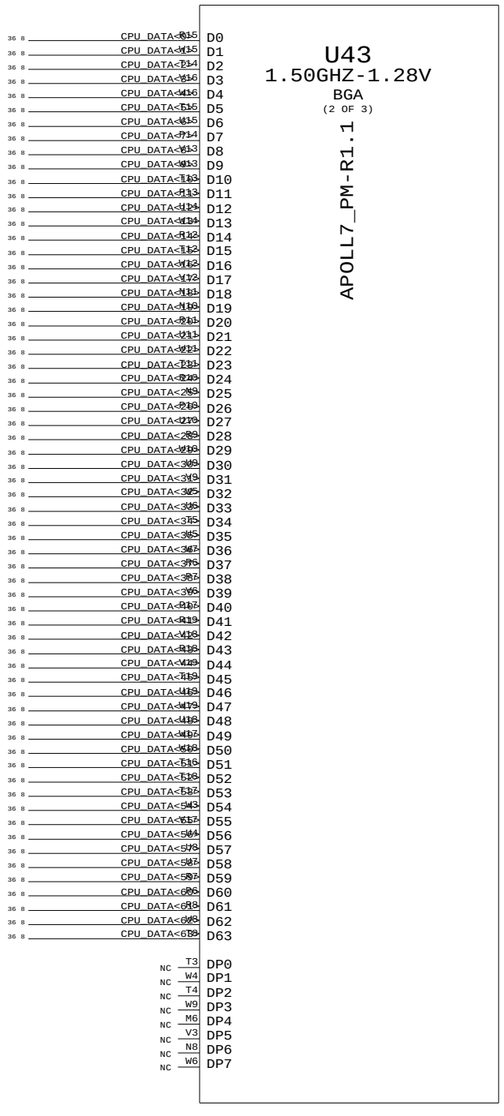
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S2855	337S2885	?	U43	ALT FOR Q16A CPU
337S2911	337S2885	?	U43	ALT FOR Q41A REV1.1.1
337S2912	337S2885	?	U43	ALT FOR Q16A REV1.1.1

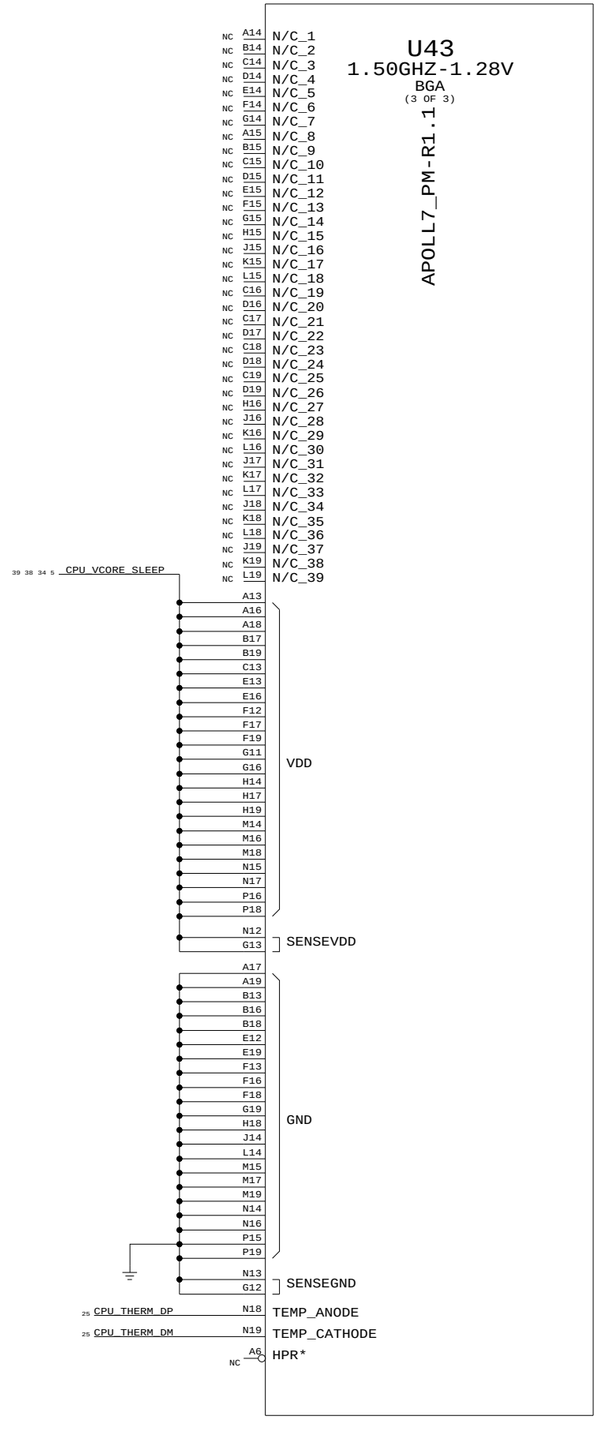
MPC7447 MAXBUS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 5 OF 44	

BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22





MPC7447/BBANG

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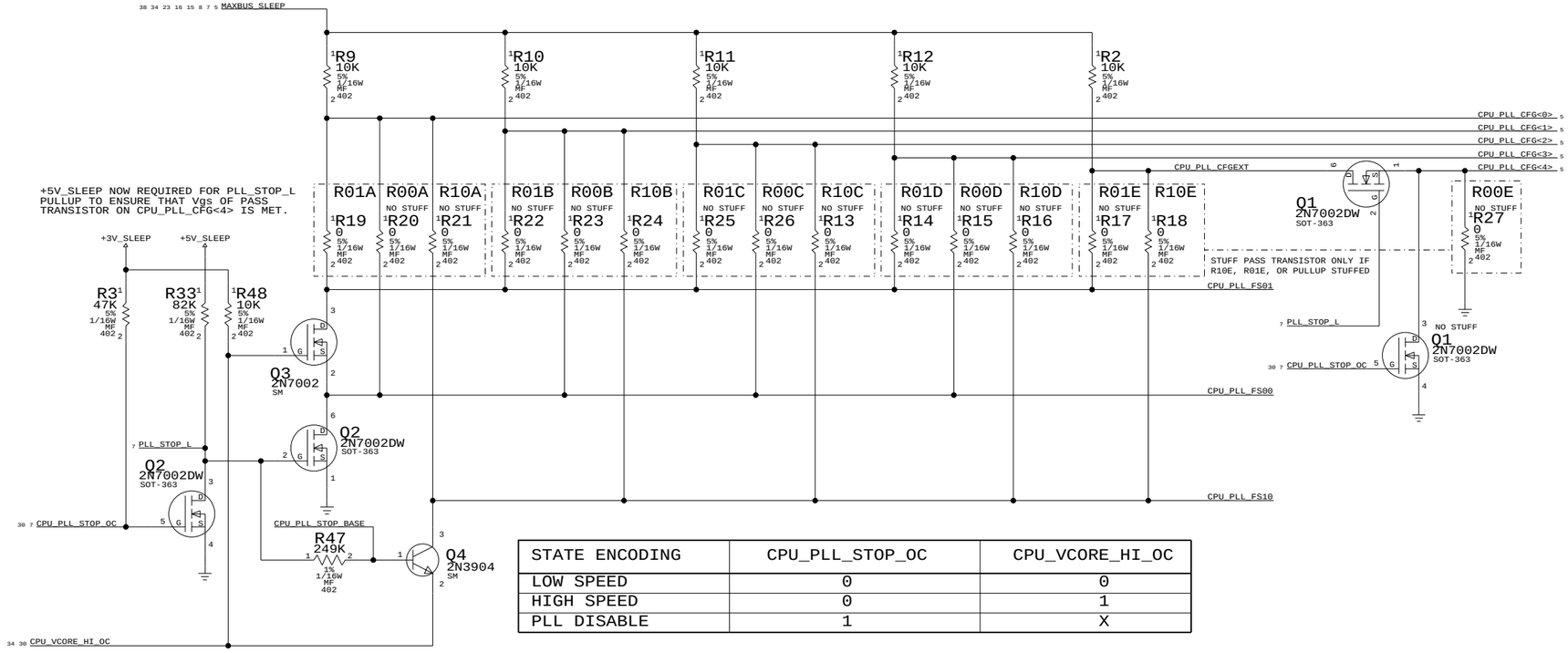
SIZE	DRAWING NUMBER	REV.
D	051-6654	C

SCALE	SHT	OF
NONE	6	44

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

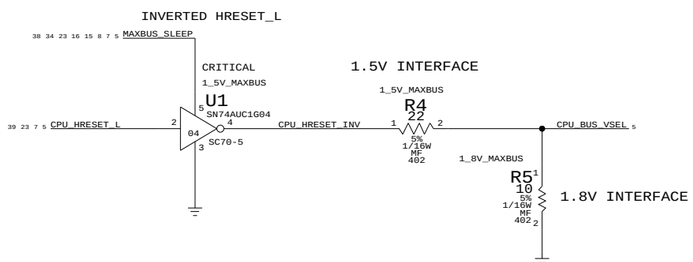
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD HEX
0.0X	PLL OFF		0	1111 0F
1.0X	PLL BYPASS		0	0011 03
2.0X	333	267	0	0100 04
3.0X	500	400	0	1000 08
4.0X	667	533	0	1010 0A
5.0X	833	667	0	1011 0B
5.5X	917	733	0	1001 09
6.0X	1000	800	0	1101 0D
6.5X	1083	867	0	0101 05
7.0X	1167	933	0	0010 02
7.5X	1250	1000	0	0001 01
8.0X	1333	1067	0	1100 0C
8.5X	1417	1133	0	0110 06
9.0X	1500	1200	1	0111 17
9.5X	1583	1267	0	0111 07
10.0X	1667	1333	1	1010 1A
10.5X	1750	1400	1	1000 18
11.0X	1833	1467	1	1001 19
11.5X	1917	1533	0	0000 00
12.0X	2000	1600	1	1011 1B
12.5X	2083	1667	1	1111 1F
13.0X	2167	1733	1	0101 15
13.5X	2250	1800	0	1110 0E
14.0X	2333	1867	1	1100 1C
15.0X	2500	2000	1	0001 11
16.0X	2667	2133	1	1101 1D
17.0X	2833	2267	1	0000 10
18.0X	3000	2400	1	0010 12
20.0X	3333	2667	1	0011 13
21.0X	3500	2800	1	0100 14
24.0X	4000	3200	1	0110 16
28.0X	4667	3733	1	1110 1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 7 OF 44	

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

R642	R135	R123	R153	R166	R179	R651	R178
NO STUFF	NO STUFF	NO STUFF		NO STUFF	NO STUFF	NO STUFF	NO STUFF
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>

R136	R643	R639	R657	R664	R673	R143	R674
			NO STUFF				
0: Disable Fuse Read 1: Active low	0: Active 1: Analyzerclk_En_h	0: Disable Fuse Read 1: Active low	0: Active low 1: ExtPLL_SDwn_Pol	Spare	Spare	Spare	Spare

(Default is Enable Fuse Read (Active low) 1: Fuse read disabled 0: Fuse read enabled)

BIT 40 TO 47

MAXBUS_SLEEP

R122	R142	R164	R134	R184	R177	R152	R165
NO STUFF	NO STUFF	NO STUFF	EXT_CLK	NO STUFF	INT_CLK	INT_CLK	INT_CLK
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>

R640	R652	R665	R644	R683	R675	R658	R666
			INT_CLK		EXT_CLK	EXT_CLK	EXT_CLK
Spare	Spare	BIT2	BIT1	BIT0	Internal spreadEn 1: Active	PCI1 Source Clock 0: PLL4 1: PLL5 (NO SPREAD)	PCI0 Source Clock 0: PLL5 1: PLL5 (NO SPREAD)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

R133	R121	R163	R151	R162	R141	R183	R176
EXT_CLK	EXT_CLK		NO STUFF	NO STUFF	NO STUFF		NO STUFF
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>

R645	R641	R668	R659	R667	R653	R684	R676
INT_CLK	INT_CLK	NO STUFF				NO STUFF	
BUF_REF_CLK_OUTEnable_h 1: Active	SelPLL4ExtSrc 1: External source	Spare	Spare	BIT2	BIT1	BIT0	Spare

TI 1394b workaround
1: TI PHY workaround

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

R227 4.7 5% 1/16W MF 402 — +1_5V_INTREPID_PLL — +1_5V_INTREPID_PLL7

C308 0.22UF 20% 6.3V CERM 402

U45 INTREPID-REV2.1 BGA

VDD15A_7 (PLL6)	H26		
CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER
CPU_ADDR<0>	D24	A_0	
CPU_ADDR<1>	D25	A_1	
CPU_ADDR<2>	A27	A_2	
CPU_ADDR<3>	E24	A_3	
CPU_ADDR<4>	G23	A_4	
CPU_ADDR<5>	B26	A_5	
CPU_ADDR<6>	A26	A_6	
CPU_ADDR<7>	D23	A_7	
CPU_ADDR<8>	A25	A_8	
CPU_ADDR<9>	E23	A_9	
CPU_ADDR<10>	J22	A_10	
CPU_ADDR<11>	B25	A_11	
CPU_ADDR<12>	H22	A_12	
CPU_ADDR<13>	G22	A_13	
CPU_ADDR<14>	D22	A_14	
CPU_ADDR<15>	B24	A_15	
CPU_ADDR<16>	B23	A_16	
CPU_ADDR<17>	E22	A_17	
CPU_ADDR<18>	J21	A_18	
CPU_ADDR<19>	G21	A_19	
CPU_ADDR<20>	E21	A_20	
CPU_ADDR<21>	A24	A_21	
CPU_ADDR<22>	D21	A_22	
CPU_ADDR<23>	A23	A_23	
CPU_ADDR<24>	H20	A_24	
CPU_ADDR<25>	B22	A_25	
CPU_ADDR<26>	H21	A_26	
CPU_ADDR<27>	A22	A_27	
CPU_ADDR<28>	E20	A_28	
CPU_ADDR<29>	B21	A_29	
CPU_ADDR<30>	D20	A_30	
CPU_ADDR<31>	A21	A_31	
CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	
INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - ? / NO BUS KEEPER - PU
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU
VSSA_7 (PLL6)	H25		

MAXBUS INTERFACE

(1 OF 9)

INTREPID OUTPUTS HIGH BY DEFAULT

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

D_0	D10	CPU_DATA<0>	6 36
D_1	G12	CPU_DATA<1>	6 36
D_2	E11	CPU_DATA<2>	6 36
D_3	H11	CPU_DATA<3>	6 36
D_4	B9	CPU_DATA<4>	6 36
D_5	B8	CPU_DATA<5>	6 36
D_6	A9	CPU_DATA<6>	6 36
D_7	A8	CPU_DATA<7>	6 36
D_8	E12	CPU_DATA<8>	6 36
D_9	D11	CPU_DATA<9>	6 36
D_10	B10	CPU_DATA<10>	6 36
D_11	J13	CPU_DATA<11>	6 36
D_12	A10	CPU_DATA<12>	6 36
D_13	D12	CPU_DATA<13>	6 36
D_14	E13	CPU_DATA<14>	6 36
D_15	G13	CPU_DATA<15>	6 36
D_16	B11	CPU_DATA<16>	6 36
D_17	D13	CPU_DATA<17>	6 36
D_18	A11	CPU_DATA<18>	6 36
D_19	G14	CPU_DATA<19>	6 36
D_20	H14	CPU_DATA<20>	6 36
D_21	E14	CPU_DATA<21>	6 36
D_22	B12	CPU_DATA<22>	6 36
D_23	G15	CPU_DATA<23>	6 36
D_24	B13	CPU_DATA<24>	6 36
D_25	H15	CPU_DATA<25>	6 36
D_26	D14	CPU_DATA<26>	6 36
D_27	B14	CPU_DATA<27>	6 36
D_28	A12	CPU_DATA<28>	6 36
D_29	G16	CPU_DATA<29>	6 36
D_30	E15	CPU_DATA<30>	6 36
D_31	J16	CPU_DATA<31>	6 36
D_32	D15	CPU_DATA<32>	6 8 36
D_33	A14	CPU_DATA<33>	6 8 36
D_34	A13	CPU_DATA<34>	6 8 36
D_35	D16	CPU_DATA<35>	6 8 36
D_36	E16	CPU_DATA<36>	6 8 36
D_37	G17	CPU_DATA<37>	6 8 36
D_38	B15	CPU_DATA<38>	6 8 36
D_39	H17	CPU_DATA<39>	6 8 36
D_40	A15	CPU_DATA<40>	6 8 36
D_41	B16	CPU_DATA<41>	6 8 36
D_42	E17	CPU_DATA<42>	6 8 36
D_43	A16	CPU_DATA<43>	6 8 36
D_44	J18	CPU_DATA<44>	6 8 36
D_45	H18	CPU_DATA<45>	6 8 36
D_46	D17	CPU_DATA<46>	6 8 36
D_47	G18	CPU_DATA<47>	6 8 36
D_48	A17	CPU_DATA<48>	6 8 36
D_49	B17	CPU_DATA<49>	6 8 36
D_50	E18	CPU_DATA<50>	6 8 36
D_51	B18	CPU_DATA<51>	6 8 36
D_52	D18	CPU_DATA<52>	6 8 36
D_53	A18	CPU_DATA<53>	6 8 36
D_54	A19	CPU_DATA<54>	6 8 36
D_55	H19	CPU_DATA<55>	6 8 36
D_56	B19	CPU_DATA<56>	6 8 36
D_57	J19	CPU_DATA<57>	6 8 36
D_58	A20	CPU_DATA<58>	6 8 36
D_59	D19	CPU_DATA<59>	6 8 36
D_60	E19	CPU_DATA<60>	6 8 36
D_61	G19	CPU_DATA<61>	6 8 36
D_62	B20	CPU_DATA<62>	6 8 36
D_63	G20	CPU_DATA<63>	6 8 36
DBG	A30	CPU_DBG_L	5 8 36
DRDY	G28	CPU_DRDY_L	5 8 36
DTI_0	K25	CPU_DTI<0>	5 36
DTI_1	D29	CPU_DTI<1>	5 36
DTI_2	B30	CPU_DTI<2>	5 36
TA	E27	CPU_TA_L	5 8 36
TEA	E28	CPU_TEA_L	5 8 36

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R197 511 1% 1/16W MF 402

R144 0 5% 1/16W MF 402 — SYSCLK_CPU — SYSCLK_CPU_UF

R137 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH

R167 0 5% 1/16W MF 402 — INT_CPUFB_OUT — INT_CPUFB_OUT_SHORT

R225 0 5% 1/16W MF 402 (NO STUFF)

R215 0 5% 1/16W MF 402

R226 0 5% 1/16W MF 402 — INT_CPUFB_IN

LONG = 1" LONGER THAN MATCHED LENGTH

R207 0 5% 1/16W MF 402 (NO STUFF) — INT_CPUFB_OUT_NORM — INT_CPUFB_LONG

R208 0 5% 1/16W MF 402

R196 0 5% 1/16W MF 402 (NO STUFF) — INT_CPUFB_IN_NORM

MAXBUS PULL-UPS

MAXBUS_SLEEP

CPU_TS_L	RP21 10K	5% 1/16W SM1
CPU_TA_L	RP21 10K	5% 1/16W SM1
CPU_ARTRY_L	RP21 10K	5% 1/16W SM1
CPU_BR_L	RP23 10K	5% 1/16W SM1
CPU_HIT_L	RP24 10K	5% 1/16W SM1
CPU_DRDY_L	RP23 10K	5% 1/16W SM1
CPU_TEA_L	RP23 10K	5% 1/16W SM1
CPU_AACK_L	RP23 10K	5% 1/16W SM1
CPU_DBG_L	RP24 10K	5% 1/16W SM1
CPU_BG_L	RP21 10K	5% 1/16W SM1
CPU_QREQ_L	RP24 10K	5% 1/16W SM1

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

R140	R161	R175	R132	R131	R150	R174	R182
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF		NO STUFF
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>

R654	R669	R677	R646	R647	R660	R678	R685
						NO STUFF	
Spare	Spare	Spare	PCI1_REQ2_L / PCI1_GNT2_L 1: GPIO2	PCI1_REQ1_L / PCI1_GNT1_L 1: GPIO1	PCI1_REQ0_L / PCI1_GNT0_L 1: GPIO0	Firewire PHY interface 0: Legacy interface 1: B-mode interface	Processor Bus Mode 0: 60x bus (G3) 1: MPX bus (G4)

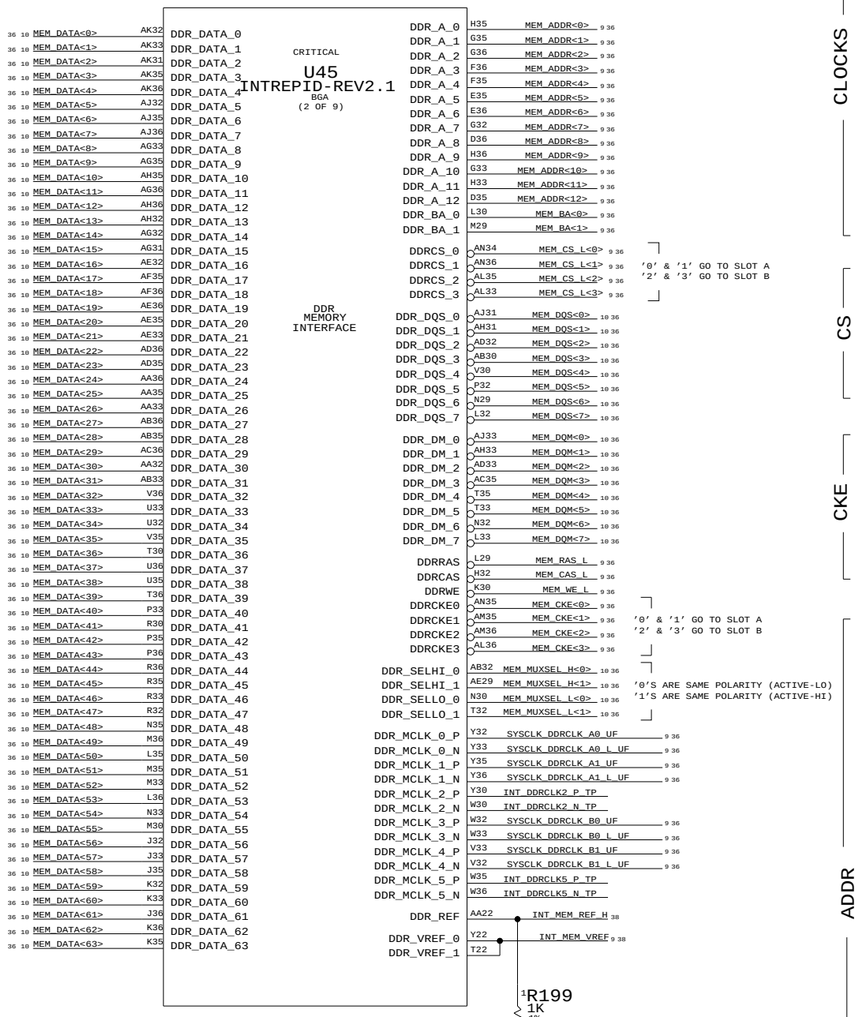
Intrepid MaxBus

APPLE COMPUTER INC.

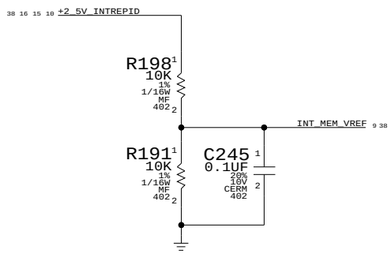
SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 8 OF 44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

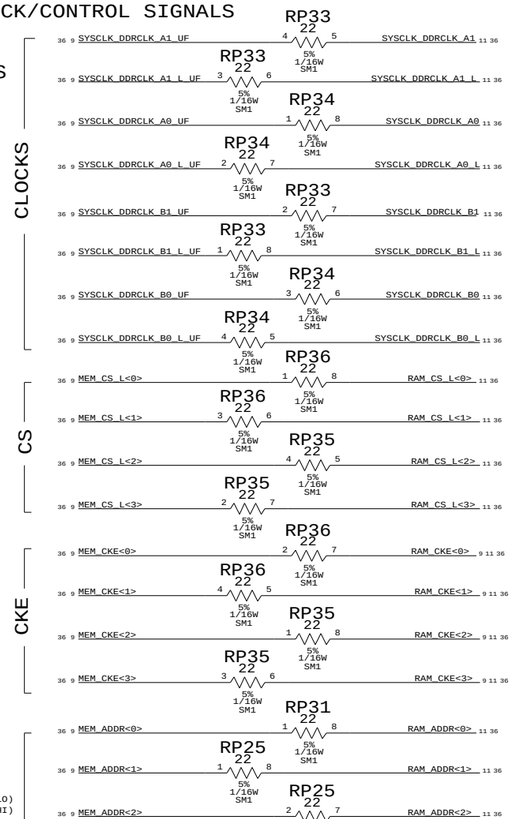
PINS ARE SWAPABLE FOR RPAKS



MEM_VREF



CLOCKS

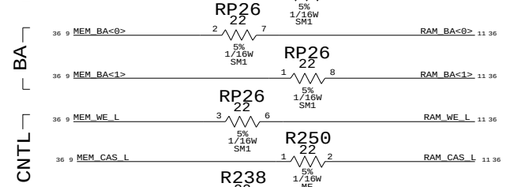


CS

CKE

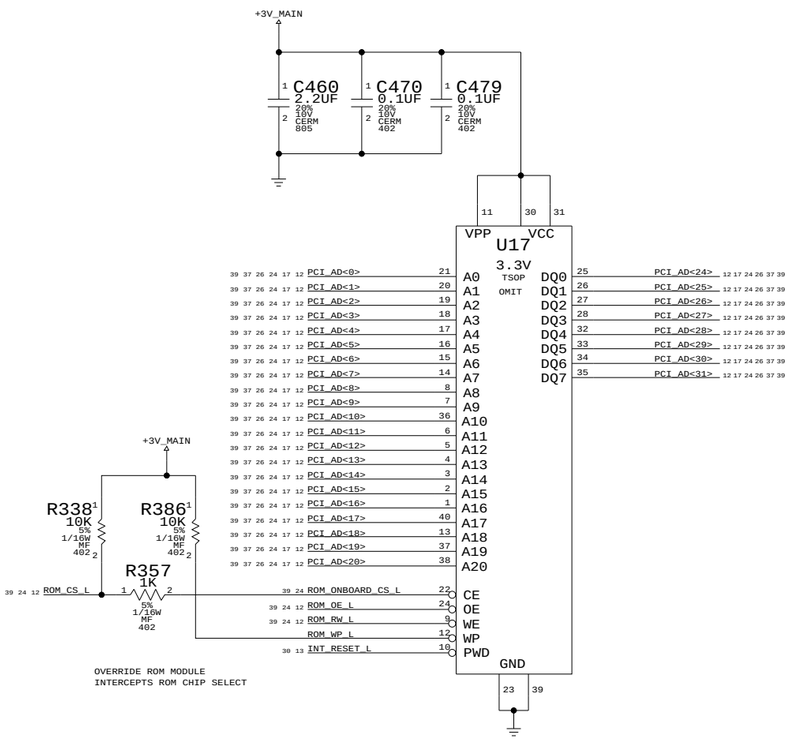
ADDR

BA



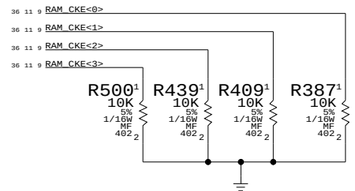
CNTL

1MB BOOT ROM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1465	1	BOOTROM,FINAL,Q41A	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF



INT - DDR/BOOTROM

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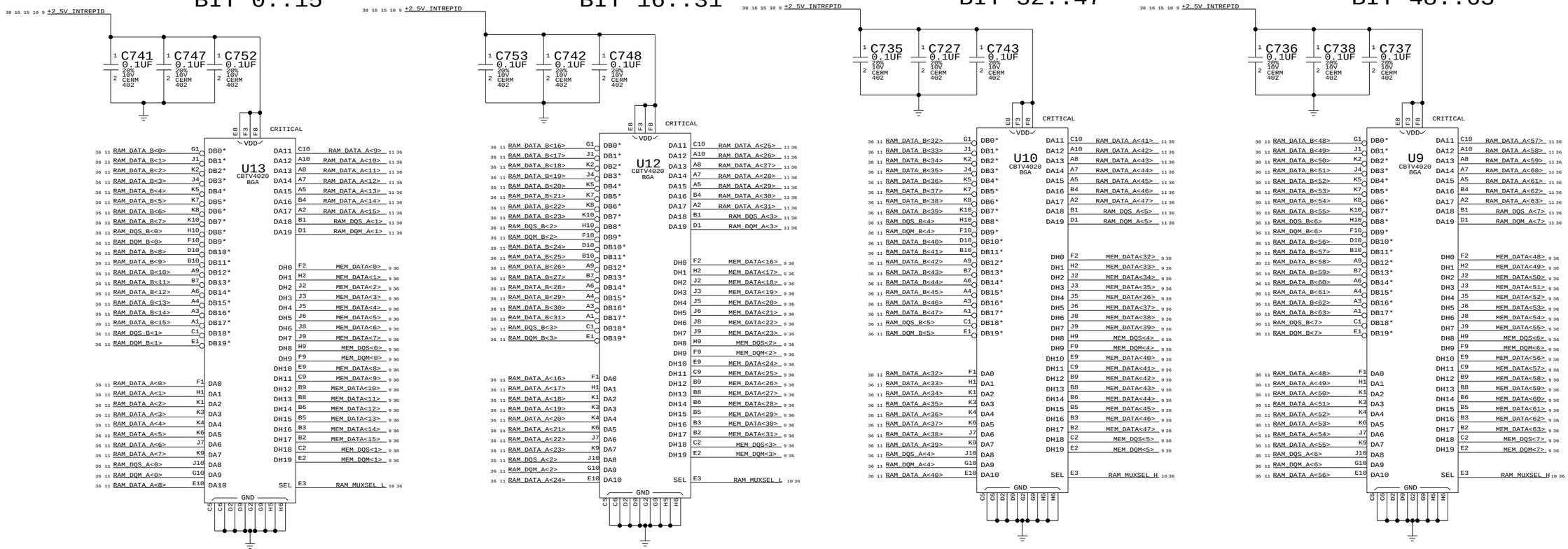
SCALE: NONE	SHT 9 OF 44	



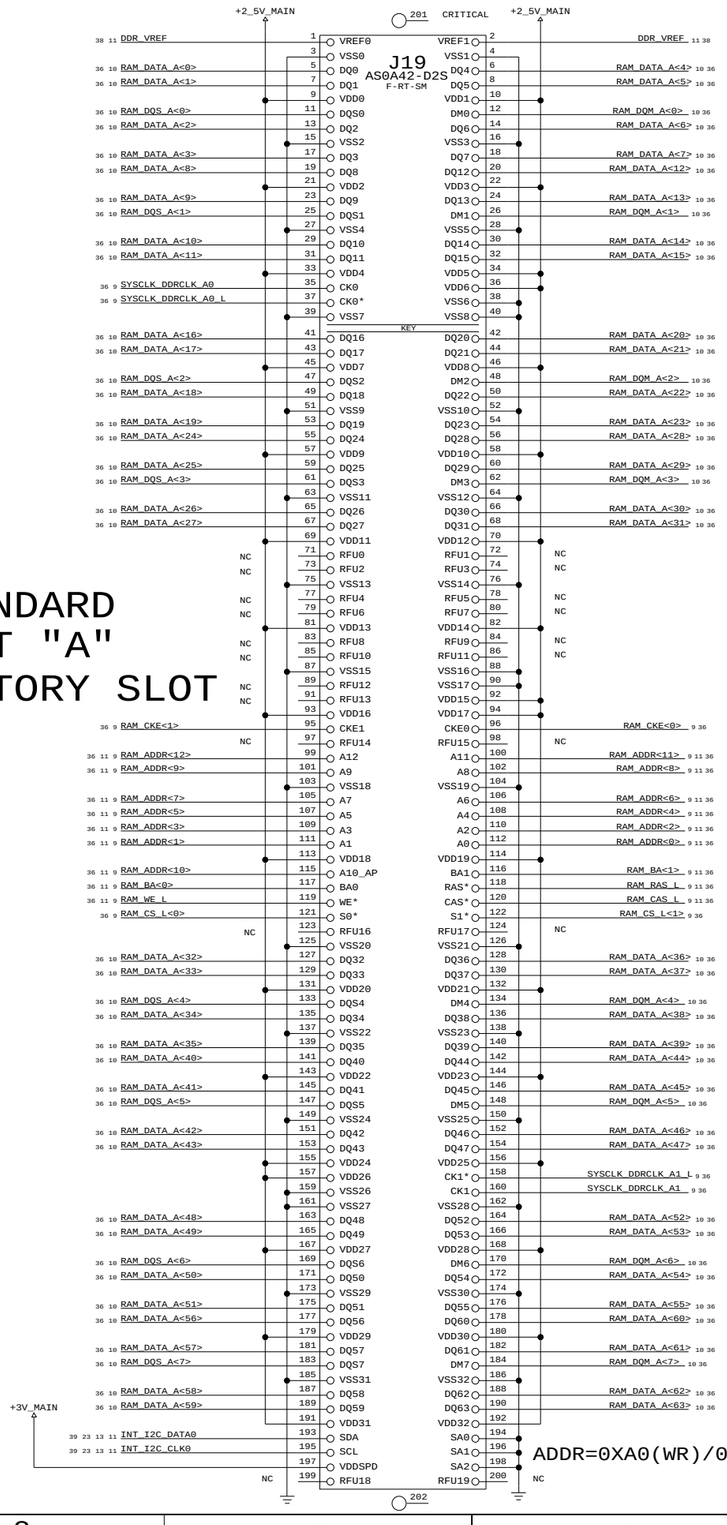
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

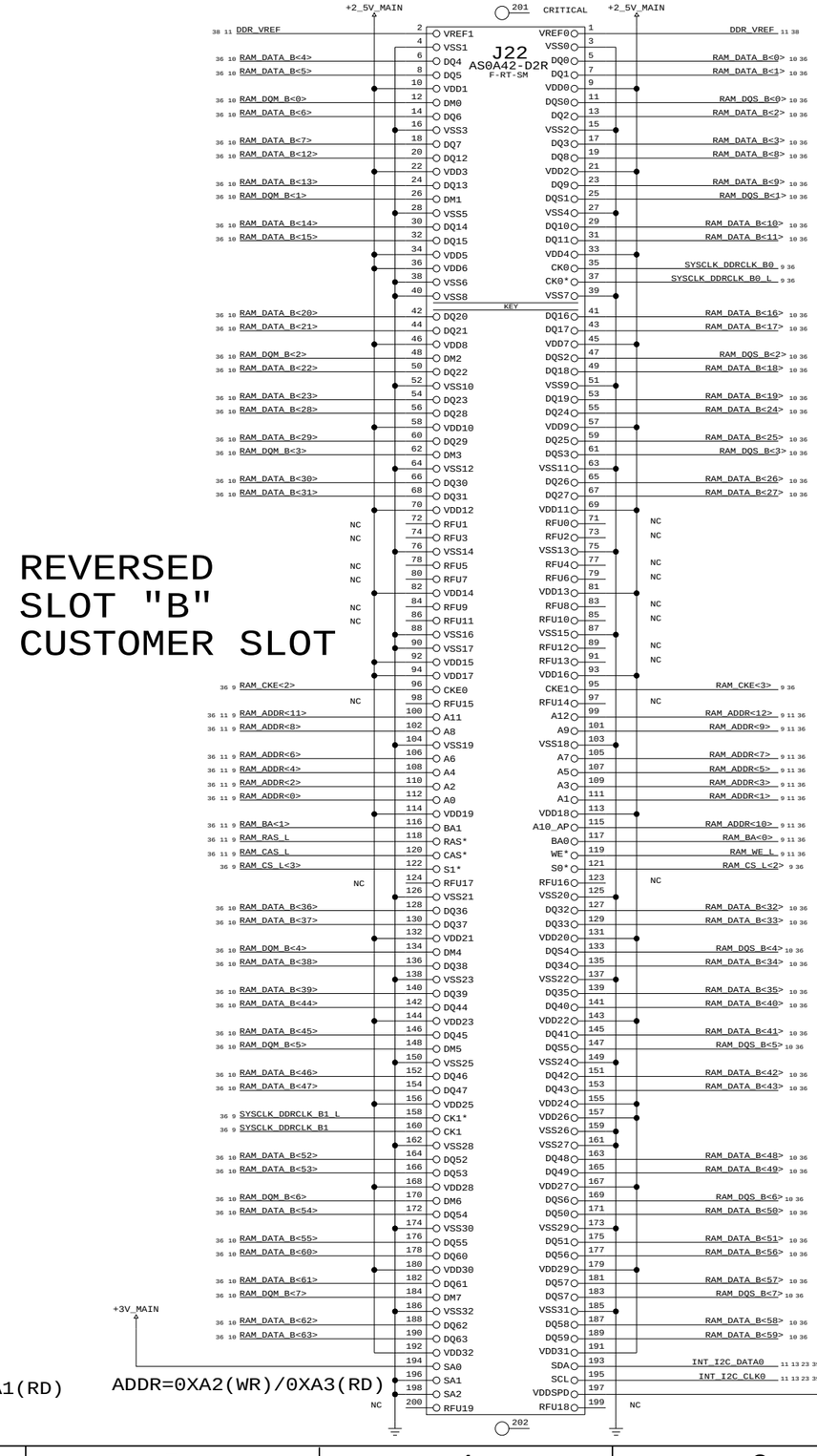
16BIT 2:1 DDR MUXES

APPLE COMPUTER INC.

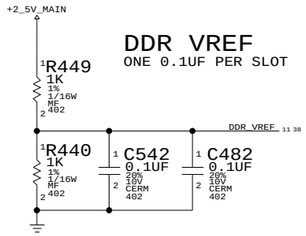
SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 10 OF 44	

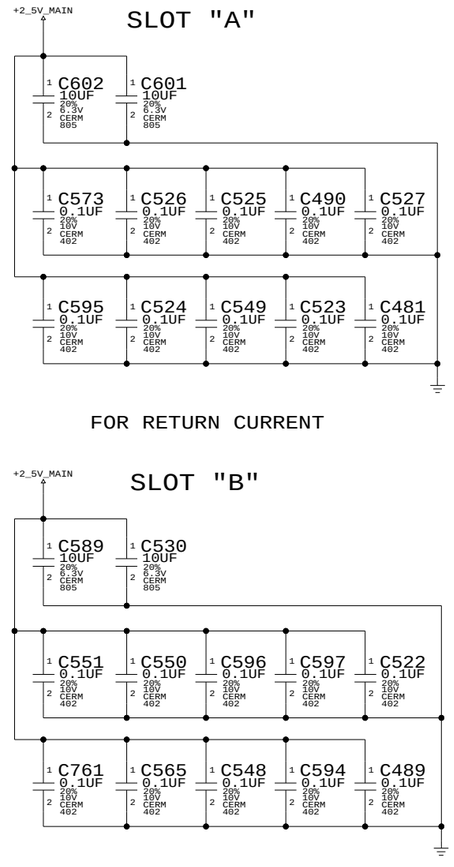


STANDARD
SLOT "A"
FACTORY SLOT



REVERSED
SLOT "B"
CUSTOMER SLOT





DDR SODIMM CONNS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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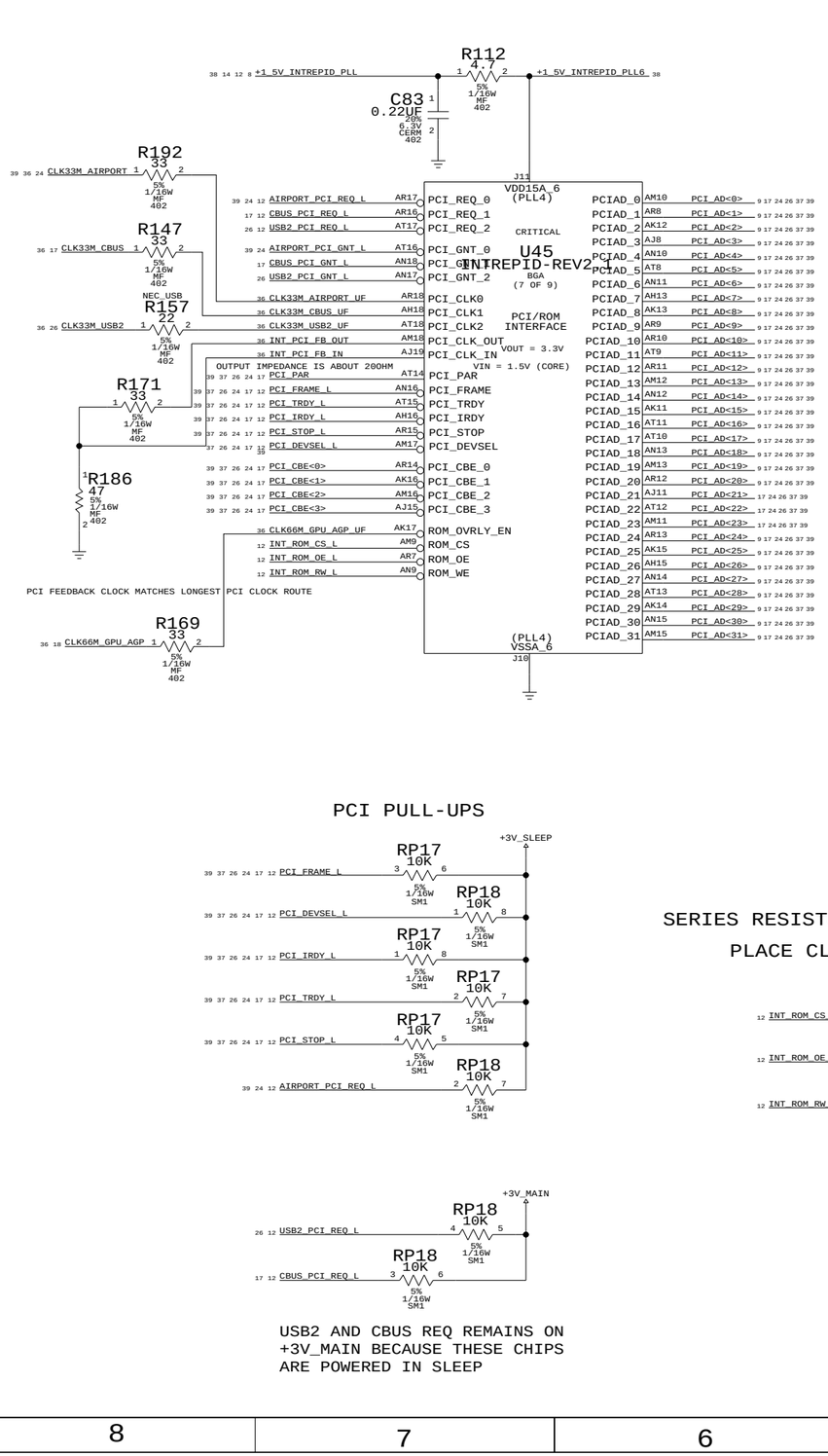
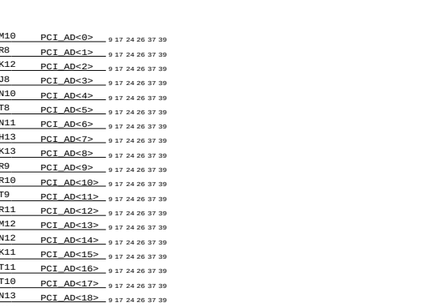
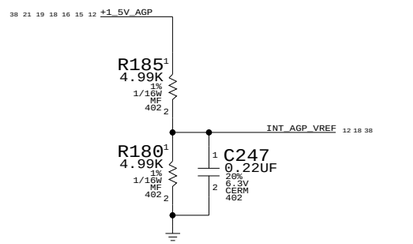
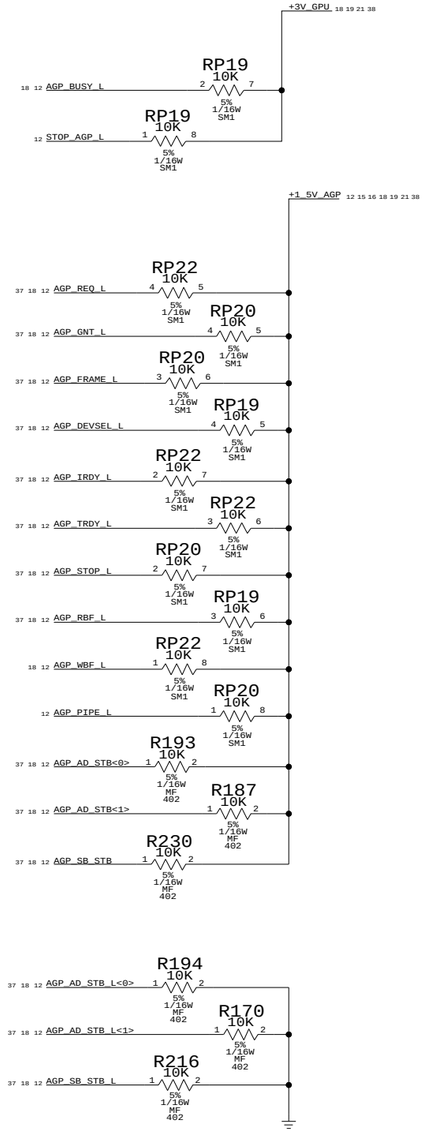
SCALE NONE

SHT 11 OF 44









INTREPID AGP/PCI

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
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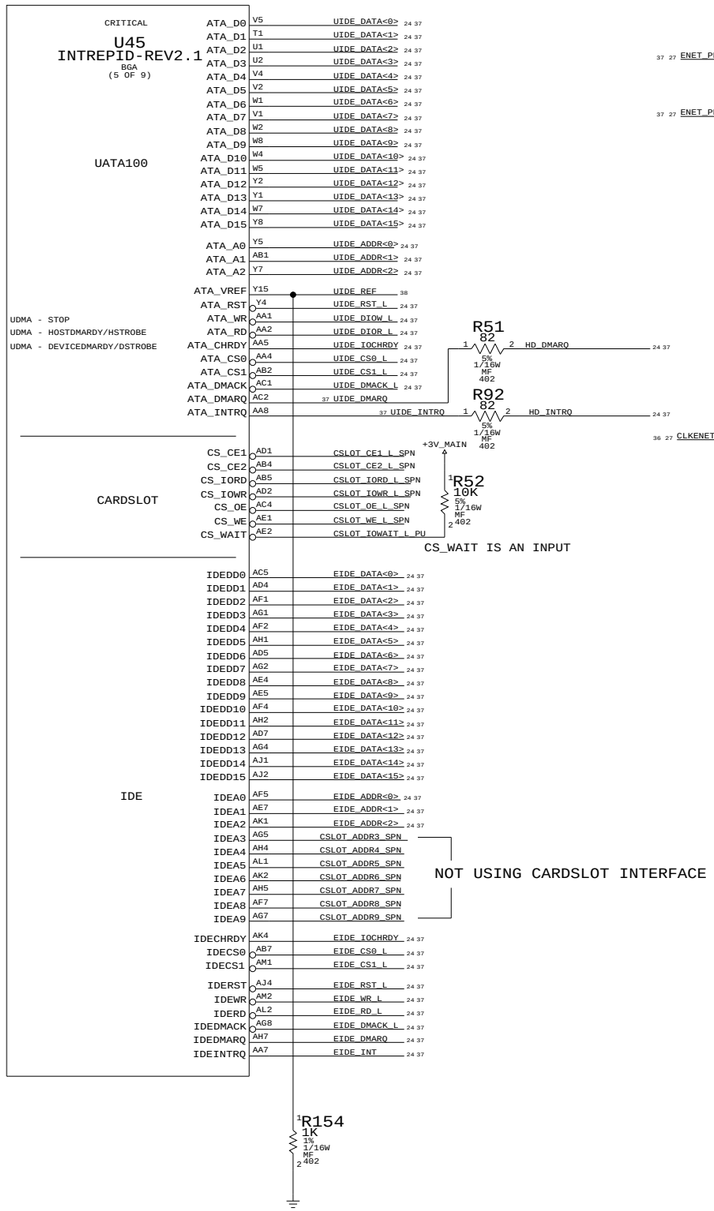

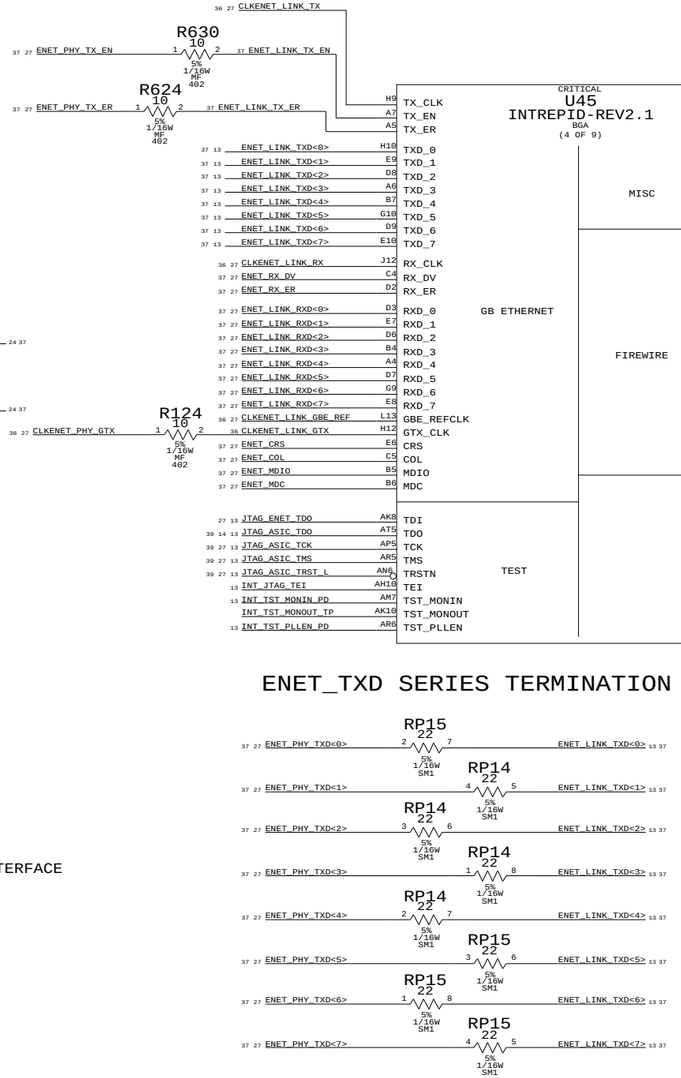

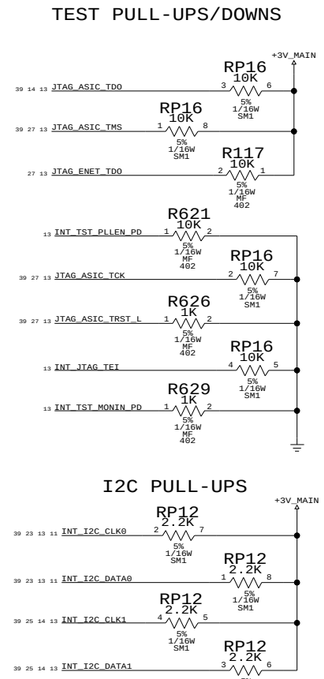

BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ (‘1’) OR WRITE (‘0’) MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 13 OF 44	

USB POWER FAULT SIGNALS

USB PORT ASSIGNMENTS

PORT A - RIGHT USB 1

PORT B - UNUSED

PORT C - LEFT USB

PORT D - UNUSED

PORT E - BLUETOOTH

PORT F - MODEM

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
359S0074	359S0086	?	U42	ALT FOR NEW SCREEN

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

INT - USB/GPIOS/I2S

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SIZE	DRAWING NUMBER	REV.
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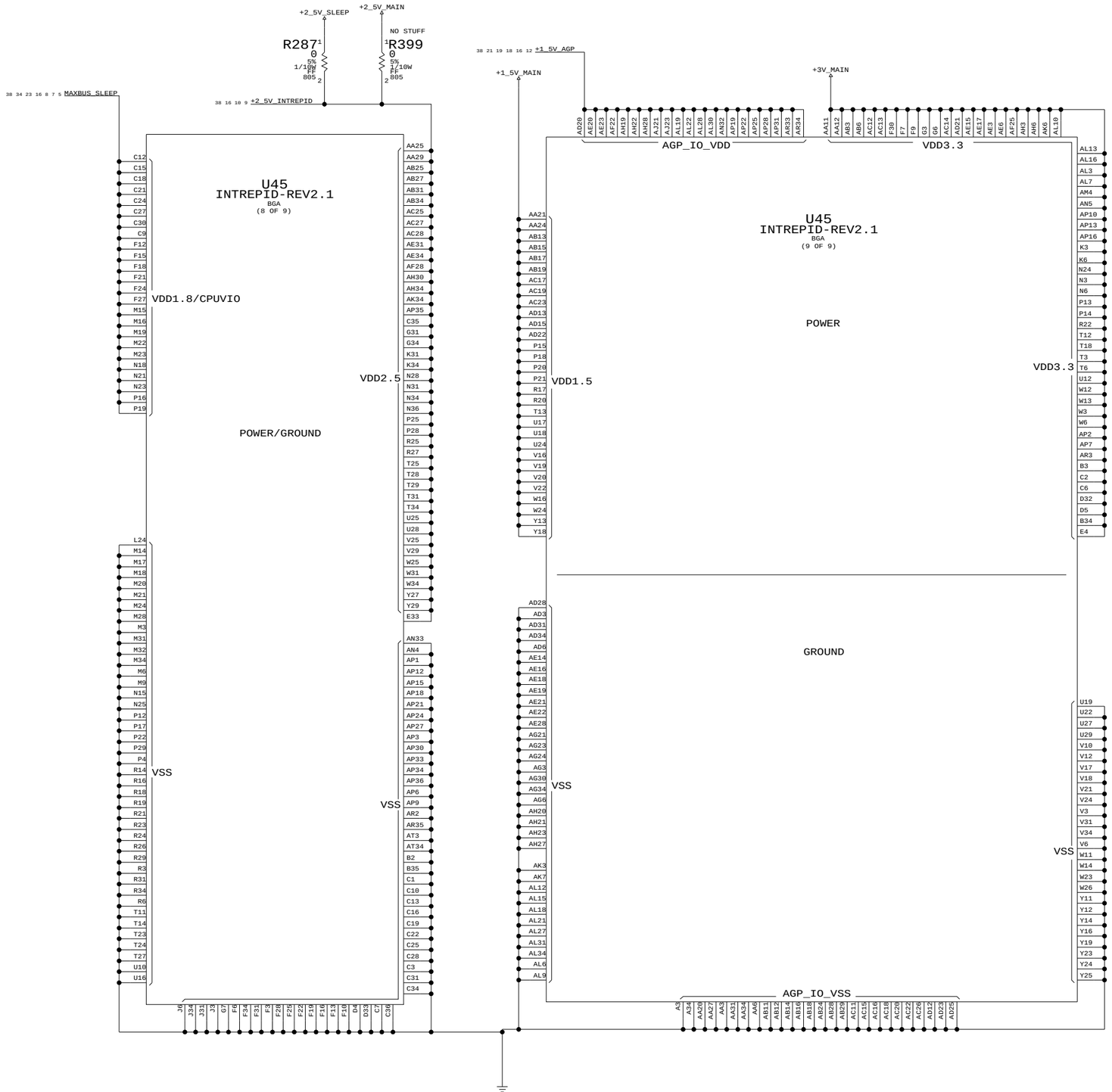
SCALE: NONE	SHT 14 OF 44	



Intrepid Power

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SCALE: NONE	SHT 15 OF 44	

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

23 15 8 7 5 38 34 MAXBUS_SLEEP

C204 10uF 20% 6.3V CERM 805 1 2
C348 10uF 20% 6.3V CERM 805 1 2
C236 10uF 20% 6.3V CERM 805 1 2
C196 10uF 20% 6.3V CERM 805 1 2

C239 0.22uF 20% 6.3V CERM 402 1 2
C240 0.22uF 20% 6.3V CERM 402 1 2
C350 0.22uF 20% 6.3V CERM 402 1 2
C312 0.22uF 20% 6.3V CERM 402 1 2
C176 0.22uF 20% 6.3V CERM 402 1 2
C288 0.22uF 20% 6.3V CERM 402 1 2
C313 0.22uF 20% 6.3V CERM 402 1 2
C94 0.22uF 20% 6.3V CERM 402 1 2
C286 0.22uF 20% 6.3V CERM 402 1 2
C158 0.22uF 20% 6.3V CERM 402 1 2
C174 0.22uF 20% 6.3V CERM 402 1 2
C206 0.22uF 20% 6.3V CERM 402 1 2
C259 0.22uF 20% 6.3V CERM 402 1 2
C237 0.22uF 20% 6.3V CERM 402 1 2
C238 0.22uF 20% 6.3V CERM 402 1 2
C95 0.22uF 20% 6.3V CERM 402 1 2
C117 0.22uF 20% 6.3V CERM 402 1 2
C241 0.22uF 20% 6.3V CERM 402 1 2
C260 0.22uF 20% 6.3V CERM 402 1 2
C314 0.22uF 20% 6.3V CERM 402 1 2
C173 0.22uF 20% 6.3V CERM 402 1 2
C171 0.22uF 20% 6.3V CERM 402 1 2
C175 0.22uF 20% 6.3V CERM 402 1 2
C226 0.22uF 20% 6.3V CERM 402 1 2
C172 0.22uF 20% 6.3V CERM 402 1 2
C207 0.22uF 20% 6.3V CERM 402 1 2
C118 0.22uF 20% 6.3V CERM 402 1 2
C287 0.22uF 20% 6.3V CERM 402 1 2
C119 0.22uF 20% 6.3V CERM 402 1 2
C349 0.22uF 20% 6.3V CERM 402 1 2
C205 0.22uF 20% 6.3V CERM 402 1 2
C209 0.22uF 20% 6.3V CERM 402 1 2

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

38 21 19 18 15 12 +1_5V_AGP

C371 10uF 20% 6.3V CERM 805 1 2
C231 10uF 20% 6.3V CERM 805 1 2
C281 10uF 20% 6.3V CERM 805 1 2
C394 10uF 20% 6.3V CERM 805 1 2

C356 0.22uF 20% 6.3V CERM 402 1 2
C297 0.22uF 20% 6.3V CERM 402 1 2
C268 0.22uF 20% 6.3V CERM 402 1 2
C217 0.22uF 20% 6.3V CERM 402 1 2
C355 0.22uF 20% 6.3V CERM 402 1 2
C267 0.22uF 20% 6.3V CERM 402 1 2
C250 0.22uF 20% 6.3V CERM 402 1 2
C298 0.22uF 20% 6.3V CERM 402 1 2
C377 0.22uF 20% 6.3V CERM 402 1 2
C216 0.22uF 20% 6.3V CERM 402 1 2
C228 0.22uF 20% 6.3V CERM 402 1 2
C230 0.22uF 20% 6.3V CERM 402 1 2
C265 0.22uF 20% 6.3V CERM 402 1 2
C378 0.22uF 20% 6.3V CERM 402 1 2
C357 0.22uF 20% 6.3V CERM 402 1 2
C229 0.22uF 20% 6.3V CERM 402 1 2
C325 0.22uF 20% 6.3V CERM 402 1 2
C393 0.22uF 20% 6.3V CERM 402 1 2
C324 0.22uF 20% 6.3V CERM 402 1 2
C323 0.22uF 20% 6.3V CERM 402 1 2
C251 0.22uF 20% 6.3V CERM 402 1 2
C266 0.22uF 20% 6.3V CERM 402 1 2
C249 0.22uF 20% 6.3V CERM 402 1 2

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C422 10uF 20% 6.3V CERM 805 1 2
C417 10uF 20% 6.3V CERM 805 1 2
C418 10uF 20% 6.3V CERM 805 1 2
C423 10uF 20% 6.3V CERM 805 1 2

C407 0.22uF 20% 6.3V CERM 402 1 2
C391 0.22uF 20% 6.3V CERM 402 1 2
C310 0.22uF 20% 6.3V CERM 402 1 2
C317 0.22uF 20% 6.3V CERM 402 1 2
C480 0.22uF 20% 6.3V CERM 402 1 2
C390 0.22uF 20% 6.3V CERM 402 1 2
C370 0.22uF 20% 6.3V CERM 402 1 2
C320 0.22uF 20% 6.3V CERM 402 1 2
C365 0.22uF 20% 6.3V CERM 402 1 2
C366 0.22uF 20% 6.3V CERM 402 1 2
C367 0.22uF 20% 6.3V CERM 402 1 2
C292 0.22uF 20% 6.3V CERM 402 1 2
C295 0.22uF 20% 6.3V CERM 402 1 2
C403 0.22uF 20% 6.3V CERM 402 1 2
C291 0.22uF 20% 6.3V CERM 402 1 2
C352 0.22uF 20% 6.3V CERM 402 1 2
C322 0.22uF 20% 6.3V CERM 402 1 2
C392 0.22uF 20% 6.3V CERM 402 1 2
C385 0.22uF 20% 6.3V CERM 402 1 2
C376 0.22uF 20% 6.3V CERM 402 1 2
C321 0.22uF 20% 6.3V CERM 402 1 2
C318 0.22uF 20% 6.3V CERM 402 1 2
C399 0.22uF 20% 6.3V CERM 402 1 2
C410 0.22uF 20% 6.3V CERM 402 1 2
C335 0.22uF 20% 6.3V CERM 402 1 2
C369 0.22uF 20% 6.3V CERM 402 1 2
C384 0.22uF 20% 6.3V CERM 402 1 2
C294 0.22uF 20% 6.3V CERM 402 1 2
C406 0.22uF 20% 6.3V CERM 402 1 2
C405 0.22uF 20% 6.3V CERM 402 1 2
C404 0.22uF 20% 6.3V CERM 402 1 2
C400 0.22uF 20% 6.3V CERM 402 1 2
C386 0.22uF 20% 6.3V CERM 402 1 2
C289 0.22uF 20% 6.3V CERM 402 1 2
C387 0.22uF 20% 6.3V CERM 402 1 2
C401 0.22uF 20% 6.3V CERM 402 1 2
C354 0.22uF 20% 6.3V CERM 402 1 2
C389 0.22uF 20% 6.3V CERM 402 1 2
C309 0.22uF 20% 6.3V CERM 402 1 2
C398 0.22uF 20% 6.3V CERM 402 1 2
C337 0.22uF 20% 6.3V CERM 402 1 2
C290 0.22uF 20% 6.3V CERM 402 1 2
C402 0.22uF 20% 6.3V CERM 402 1 2
C397 0.22uF 20% 6.3V CERM 402 1 2
C368 0.22uF 20% 6.3V CERM 402 1 2
C334 0.22uF 20% 6.3V CERM 402 1 2
C388 0.22uF 20% 6.3V CERM 402 1 2
C293 0.22uF 20% 6.3V CERM 402 1 2
C319 0.22uF 20% 6.3V CERM 402 1 2
C336 0.22uF 20% 6.3V CERM 402 1 2
C316 0.22uF 20% 6.3V CERM 402 1

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C128 10uF 20% 6.3V CERM 805 1 2
C101 10uF 20% 6.3V CERM 805 1 2
C157 10uF 20% 6.3V CERM 805 1 2
C315 10uF 20% 6.3V CERM 805 1 2

C147 0.22uF 20% 6.3V CERM 402 1 2
C243 0.22uF 20% 6.3V CERM 402 1 2
C262 0.22uF 20% 6.3V CERM 402 1 2
C242 0.22uF 20% 6.3V CERM 402 1 2
C227 0.22uF 20% 6.3V CERM 402 1 2
C181 0.22uF 20% 6.3V CERM 402 1 2
C142 0.22uF 20% 6.3V CERM 402 1 2
C215 0.22uF 20% 6.3V CERM 402 1 2
C278 0.22uF 20% 6.3V CERM 402 1 2
C264 0.22uF 20% 6.3V CERM 402 1 2
C244 0.22uF 20% 6.3V CERM 402 1 2
C212 0.22uF 20% 6.3V CERM 402 1 2
C178 0.22uF 20% 6.3V CERM 402 1 2
C179 0.22uF 20% 6.3V CERM 402 1 2
C177 0.22uF 20% 6.3V CERM 402 1 2
C159 0.22uF 20% 6.3V CERM 402 1 2
C161 0.22uF 20% 6.3V CERM 402 1 2
C162 0.22uF 20% 6.3V CERM 402 1 2
C280 0.22uF 20% 6.3V CERM 402 1 2
C279 0.22uF 20% 6.3V CERM 402 1 2
C144 0.22uF 20% 6.3V CERM 402 1 2
C246 0.22uF 20% 6.3V CERM 402 1 2
C211 0.22uF 20% 6.3V CERM 402 1 2
C263 0.22uF 20% 6.3V CERM 402 1 2
C180 0.22uF 20% 6.3V CERM 402 1 2
C213 0.22uF 20% 6.3V CERM 402 1 2
C197 0.22uF 20% 6.3V CERM 402 1 2
C208 0.22uF 20% 6.3V CERM 402 1 2
C214 0.22uF 20% 6.3V CERM 402 1 2

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

+3V_MAIN

C164 10uF 20% 6.3V CERM 805 1 2
C395 10uF 20% 6.3V CERM 805 1 2
C10 10uF 20% 6.3V CERM 805 1 2
C9 10uF 20% 6.3V CERM 805 1 2

C375 0.22uF 20% 6.3V CERM 402 1 2
C351 0.22uF 20% 6.3V CERM 402 1 2
C53 0.22uF 20% 6.3V CERM 402 1 2
C42 0.22uF 20% 6.3V CERM 402 1 2
C21 0.22uF 20% 6.3V CERM 402 1 2
C185 0.22uF 20% 6.3V CERM 402 1 2
C31 0.22uF 20% 6.3V CERM 402 1 2
C143 0.22uF 20% 6.3V CERM 402 1 2
C123 0.22uF 20% 6.3V CERM 402 1 2
C121 0.22uF 20% 6.3V CERM 402 1 2
C33 0.22uF 20% 6.3V CERM 402 1 2
C184 0.22uF 20% 6.3V CERM 402 1 2
C43 0.22uF 20% 6.3V CERM 402 1 2
C35 0.22uF 20% 6.3V CERM 402 1 2
C261 0.22uF 20% 6.3V CERM 402 1 2
C60 0.22uF 20% 6.3V CERM 402 1 2
C52 0.22uF 20% 6.3V CERM 402 1 2
C199 0.22uF 20% 6.3V CERM 402 1 2
C57 0.22uF 20% 6.3V CERM 402 1 2
C19 0.22uF 20% 6.3V CERM 402 1 2
C16 0.22uF 20% 6.3V CERM 402 1 2
C108 0.22uF 20% 6.3V CERM 402 1 2
C55 0.22uF 20% 6.3V CERM 402 1 2
C32 0.22uF 20% 6.3V CERM 402 1 2
C125 0.22uF 20% 6.3V CERM 402 1 2
C45 0.22uF 20% 6.3V CERM 402 1 2
C76 0.22uF 20% 6.3V CERM 402 1 2
C277 0.22uF 20% 6.3V CERM 402 1 2
C28 0.22uF 20% 6.3V CERM 402 1 2
C26 0.22uF 20% 6.3V CERM 402 1 2
C34 0.22uF 20% 6.3V CERM 402 1 2
C23 0.22uF 20% 6.3V CERM 402 1 2
C120 0.22uF 20% 6.3V CERM 402 1 2
C146 0.22uF 20% 6.3V CERM 402 1 2
C141 0.22uF 20% 6.3V CERM 402 1 2
C30 0.22uF 20% 6.3V CERM 402 1 2
C145 0.22uF 20% 6.3V CERM 402 1 2
C96 0.22uF 20% 6.3V CERM 402 1 2
C54 0.22uF 20% 6.3V CERM 402 1 2
C50 0.22uF 20% 6.3V CERM 402 1 2
C75 0.22uF 20% 6.3V CERM 402 1 2
C122 0.22uF 20% 6.3V CERM 402 1 2
C51 0.22uF 20% 6.3V CERM 402 1 2
C59 0.22uF 20% 6.3V CERM 402 1 2
C163 0.22uF 20% 6.3V CERM 402 1 2
C126 0.22uF 20% 6.3V CERM 402 1 2
C98 0.22uF 20% 6.3V CERM 402 1 2
C109 0.22uF 20% 6.3V CERM 402 1 2
C56 0.22uF 20% 6.3V CERM 402 1 2
C27 0.22uF 20% 6.3V CERM 402 1 2
C296 0.22uF 20% 6.3V CERM 402 1 2
C248 0.22uF 20% 6.3V CERM 402 1 2
C210 0.22uF 20% 6.3V CERM 402 1 2
C58 0.22uF 20% 6.3V CERM 402 1 2
C22 0.22uF 20% 6.3V CERM 402 1 2
C20 0.22uF 20% 6.3V CERM 402 1 2
C61 0.22uF 20% 6.3V CERM 402 1 2
C44 0.22uF 20% 6.3V CERM 402 1 2
C29 0.22uF 20% 6.3V CERM 402 1 2
C24 0.22uF 20% 6.3V CERM 402 1 2
C183 0.22uF 20% 6.3V CERM 402 1 2
C18 0.22uF 20% 6.3V CERM 402 1 2
C49 0.22uF 20% 6.3V CERM 402 1 2
C36 0.22uF 20% 6.3V CERM 402 1 2
C17 0.22uF 20% 6.3V CERM 402 1 2
C99 0.22uF 20% 6.3V CERM 402 1 2
C396 0.22uF 20% 6.3V CERM 402 1 2
C124 0.22uF 20% 6.3V CERM 402 1 2
C127 0.22uF 20% 6.3V CERM 402 1 2
C100 0.22uF 20% 6.3V CERM 402 1 2

Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 16 OF 44	

PCI1510 PULL-UPS

+3V_MAIN

R757 10K 5% 1/16W MF 402 — CBUS_PCI_PERR_L 17
R756 10K 5% 1/16W MF 402 — CBUS_PCI_SERR_L 17
R753 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU 17

+3V_MAIN

C813 10UF 20% 6.3V CERM 805
C795 0.22UF 20% 6.3V CERM 402
C798 0.22UF 20% 6.3V CERM 402
C790 0.22UF 20% 6.3V CERM 402
C796 0.22UF 20% 6.3V CERM 402
C797 0.22UF 20% 6.3V CERM 402
C791 0.22UF 20% 6.3V CERM 402

39 30 26 24 20 18 17 14 MAIN_RESET_L

THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD

R348 47 5% 1/16W MF 402

+3V_MAIN
+5V_MAIN

NO STUFF
R373 10K 5% 1/16W MF 402

U19
TPS2211
SSOI

NC	9		
V_12	5	AVPP	10
V_5_1	6		
V_5_2	3	AVCC0	11
V_3_1	4	AVCC1	12
V_3_2		AVCC2	13
VCCD0	1		
VCCD1	2		
VPPD0	15	CRITICAL	
VPPD1	14		
SHTDWN	16		
GND	7	OC	8 NC

+VPP_CBUS_SW 17 38
+VCC_CBUS_SW 17 38

C773 0.1UF 20% 10V CERM 402
C467 0.1UF 20% 10V CERM 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

TPS2211_SHDN_L_PU

R762 10K 5% 1/16W MF 402

+2_5V_MAIN

C789 0.22UF 20% 6.3V CERM 402

A7 C13 D5 E1 M1 N7 N11
VCC

NC H10 CLK_48_RSVD/NC
PCI1510_VR_EN_L D4 VR_EN*
L8 VR_PORT

CRITICAL
U26
PCI1510GGU
BGA

CLAMP FOR PC-CARD
CLAMP FOR PCI

VCCCB	B11	
VCCP	L3	
VCCD0*	N13	CBUS_VCCD0_L
VCCD1*	L12	CBUS_VCCD1_L
VPPD0	K9	CBUS_VPPD0
VPPD1	M11	CBUS_VPPD1

CD1*/CCD1*	L13	CBUS_DET_1_L 17 39
CD2*/CCD2*	B5	CBUS_DET_2_L 17 39
IORD*/CAD13	F12	CBUS_IORD_L 17
IOWR*/CAD15	C11	CBUS_IOWR_L 17
OE*/CAD11	G10	CBUS_OE_L 17
CE1*/CC/BE0*	H13	CBUS_CE1_L 17
VS1*/CVS1	B2	CBUS_VS1 17
VS2*/CVS2	A9	CBUS_VS2 17
WE*/CGNT*	D13	CBUS_WE_L 17
RDY/IREQ*/CINT*	A6	CBUS_READY 17
RESET/CRST*	D8	CBUS_RESET_L 17
REG*/CC/BE3*	A8	CBUS_REG_L 17
BVD1/CSTSCHG/STSCHG*/RI*	C6	CBUS_BVD1_L 17
BVD2/SPKR*/CAUDIO	D6	CBUS_BVD2_L 17
INTEGRATED PULL-UP WP/IOIS16*/CCLKRUN*	A5	CBUS_WP_L 17
CE2/CAD10*	G13	CBUS_CE2_L 17
INPACK/CREQ*	B8	CBUS_INPACK_L 17
WAIT/CSERR*	B6	CBUS_WAIT_L 17

A0/CAD26	C7	CBUS_ADDR<0> 17
A1/CAD25	D7	CBUS_ADDR<1> 17
A2/CAD24	B7	CBUS_ADDR<2> 17
A3/CAD23	D10	CBUS_ADDR<3> 17
A4/CAD22	B12	CBUS_ADDR<4> 17
A5/CAD21	C8	CBUS_ADDR<5> 17
A6/CAD20	C9	CBUS_ADDR<6> 17
A7/CAD18	A12	CBUS_ADDR<7> 17
A8/CC/BE1*	E11	CBUS_ADDR<8> 17
A9/CAD14	F11	CBUS_ADDR<9> 17
A10/CAD9	G11	CBUS_ADDR<10> 17
A11/CAD12	G12	CBUS_ADDR<11> 17
A12/CC/BE2*	D9	CBUS_ADDR<12> 17
A13/CPAR	E12	CBUS_ADDR<13> 17
A14/CPERR*	D12	CBUS_ADDR<14> 17
A15/CIRDY*	C10	CBUS_ADDR<15> 17
A16/CCLK	B13	CBUS_ADDR_16_UF
A17/CAD16	F10	CBUS_ADDR<17> 17
A18/RSVD	E13	CBUS_ADDR<18> 17
A19/CBLOCK*	A13	CBUS_ADDR<19> 17
A20/CSTOP*	E10	CBUS_ADDR<20> 17
A21/CDEVSEL*	D11	CBUS_ADDR<21> 17
A22/CTRDY*	C12	CBUS_ADDR<22> 17
A23/CFRAME*	A10	CBUS_ADDR<23> 17
A24/CAD17	B10	CBUS_ADDR<24> 17
A25/CAD19	B9	CBUS_ADDR<25> 17

D0/CAD27	A4	CBUS_DATA<0> 17
D1/CAD29	C4	CBUS_DATA<1> 17
D2/RSVD	A3	CBUS_DATA<2> 17
D3/CAD0	K11	CBUS_DATA<3> 17
D4/CAD1	K12	CBUS_DATA<4> 17
D5/CAD3	J13	CBUS_DATA<5> 17
D6/CAD5	J10	CBUS_DATA<6> 17
D7/CAD7	H12	CBUS_DATA<7> 17
D8/CAD28	C5	CBUS_DATA<8> 17
D9/CAD30	B4	CBUS_DATA<9> 17
D10/CAD31	B3	CBUS_DATA<10> 17
D11/CAD2	M12	CBUS_DATA<11> 17
D12/CAD4	J11	CBUS_DATA<12> 17
D13/CAD6	K13	CBUS_DATA<13> 17
D14/RSVD	J12	CBUS_DATA<14> 17
D15/CAD8	H11	CBUS_DATA<15> 17

R750 47 5% 1/16W MF 402 — CBUS_ADDR<16> 17

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C783 2.2UF 20% 10V CERM 805
C776 2.2UF 20% 10V CERM 805

39 37 26 24 12 9 PCI_AD<0> N8 AD0
39 37 26 24 12 9 PCI_AD<1> M7 AD1
39 37 26 24 12 9 PCI_AD<2> L7 AD2
39 37 26 24 12 9 PCI_AD<3> N6 AD3
39 37 26 24 12 9 PCI_AD<4> K4 AD4
39 37 26 24 12 9 PCI_AD<5> M6 AD5
39 37 26 24 12 9 PCI_AD<6> L6 AD6
39 37 26 24 12 9 PCI_AD<7> N5 AD7
39 37 26 24 12 9 PCI_AD<8> N4 AD8
39 37 26 24 12 9 PCI_AD<9> M2 AD9
39 37 26 24 12 9 PCI_AD<10> M5 AD10
39 37 26 24 12 9 PCI_AD<11> L4 AD11
39 37 26 24 12 9 PCI_AD<12> N3 AD12
39 37 26 24 12 9 PCI_AD<13> K5 AD13
39 37 26 24 12 9 PCI_AD<14> L5 AD14
39 37 26 24 12 9 PCI_AD<15> M4 AD15
39 37 26 24 12 9 PCI_AD<16> J4 AD16
39 37 26 24 12 9 PCI_AD<17> H1 AD17
39 37 26 24 12 9 PCI_AD<18> H3 AD18
39 PCI_AD<19> H2 AD19
39 37 26 24 12 9 PCI_AD<20> G2 AD20
39 37 26 24 12 PCI_AD<21> G4 AD21
39 37 26 24 12 PCI_AD<22> F1 AD22
39 37 26 24 12 PCI_AD<23> C3 AD23
39 37 26 24 12 9 PCI_AD<24> F3 AD24
39 37 26 24 12 9 PCI_AD<25> E2 AD25
39 37 26 24 12 9 PCI_AD<26> F4 AD26
39 37 26 24 12 9 PCI_AD<27> B1 AD27
39 37 26 24 12 9 PCI_AD<28> D2 AD28
39 37 26 24 12 9 PCI_AD<29> E4 AD29
39 37 26 24 12 9 PCI_AD<30> D3 AD30
39 37 26 24 12 9 PCI_AD<31> E3 AD31

R767 22 5% 1/16W MF 402

39 37 26 24 12 PCI_CBE<0> K6 C/BE0*
39 37 26 24 12 PCI_CBE<1> M3 C/BE1*
39 37 26 24 12 PCI_CBE<2> J2 C/BE2*
39 37 26 24 12 PCI_CBE<3> A1 C/BE3*

39 37 26 24 12 PCI_PAR N1 PAR
39 37 26 24 12 PCI_IRDY_L K1 IRDY
17 CBUS_PCI_SERR_L L2 SERR
CBUS_PCI_IDSEL F2 IDSEL
17 CBUS_PCI_PERR_L K3 PERR
39 37 26 24 12 PCI_FRAME_L J1 FRAME
39 37 26 24 12 PCI_STOP_L L1 STOP
39 37 26 24 12 PCI_TRDY_L J3 TRDY
39 37 26 24 12 PCI_DEVSEL_L K2 DEVSEL
CBUS_PCI_RESET_L G3 PRST
12 CBUS_PCI_REQ_L C2 REQ
12 CBUS_PCI_GNT_L C1 GNT
36 12 CLK33M_CBUS G1 PCLK

NO STUFF
R764 47 5% 1/16W MF 402

30 27 26 23 IO_RESET_L

R766 47 5% 1/16W MF 402

39 30 26 24 20 18 17 14 MAIN_RESET_L

NC M9 SPKROUT
NC M8 RI_OUT/PME
17 CBUS_SUSPEND_PU N10 SUSPEND

14 CBUS_INT_L K7 MFUNC0
17 CBUS_MFUNC1_PD N9 MFUNC1
17 CBUS_MFUNC2_PD L9 MFUNC2
17 CBUS_MFUNC3_PD K10 MFUNC3
17 CBUS_MFUNC4_PD M10 MFUNC4
17 CBUS_MFUNC5_PD N12 MFUNC5
17 CBUS_MFUNC6_PD L10 MFUNC6

L11 GRST

RP39 10K 5% 1/32W 25V SM

5 10 6 4 7 3 9 8 2 1
CBUS_MFUNC1_PD 17
CBUS_MFUNC2_PD 17
CBUS_MFUNC3_PD 17
CBUS_MFUNC4_PD 17
CBUS_MFUNC5_PD 17
CBUS_MFUNC6_PD 17

GND
A2 A11 D1 F13 H4 K8 M13 N2

PC CARD/CARDBUS CONNECTOR

CRITICAL
J9
QT500806-L111
M-ST-SM1

	2	1	CBUS_DATA<3> 17
39 17 CBUS_DET_1_L	4	3	CBUS_DATA<4> 17
17 CBUS_DATA<11>	6	5	CBUS_DATA<5> 17
17 CBUS_DATA<12>	8	7	CBUS_DATA<6> 17
17 CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7> 17
17 CBUS_DATA<14>	14	13	CBUS_CE1_L 17
17 CBUS_DATA<15>	16	15	CBUS_ADDR<10> 17
17 CBUS_CE2_L	18	17	CBUS_OE_L 17
17 CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11> 17
17 CBUS_IORD_L	24	23	CBUS_ADDR<9> 17
17 CBUS_IOWR_L	26	25	CBUS_ADDR<8> 17
17 CBUS_ADDR<17>	28	27	CBUS_ADDR<13> 17
17 CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14> 17
17 CBUS_ADDR<19>	34	33	CBUS_WE_L 17
17 CBUS_ADDR<20>	36	35	CBUS_READY 17
17 CBUS_ADDR<21>	38	37	+VCC_CBUS_SW 17 38
38 17 +VCC_CBUS_SW	40	39	
	42	41	+VPP_CBUS_SW 17 38
38 17 +VPP_CBUS_SW	44	43	CBUS_ADDR<16> 17
17 CBUS_ADDR<22>	46	45	CBUS_ADDR<15> 17
17 CBUS_ADDR<23>	48	47	CBUS_ADDR<12> 17
17 CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7> 17
17 CBUS_ADDR<25>	54	53	CBUS_ADDR<6> 17
17 CBUS_VS2	56	55	CBUS_ADDR<5> 17
17 CBUS_RESET_L	58	57	CBUS_ADDR<4> 17
17 CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3> 17
17 CBUS_INPACK_L	64	63	CBUS_ADDR<2> 17
17 CBUS_REG_L	66	65	CBUS_ADDR<1> 17
17 CBUS_BVD2_L	68	67	CBUS_ADDR<0> 17
17 CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0> 17
17 CBUS_DATA<8>	74	73	CBUS_DATA<1> 17
17 CBUS_DATA<9>	76	75	CBUS_DATA<2> 17
17 CBUS_DATA<10>	78	77	CBUS_WP_L 17
39 17 CBUS_DET_2_L	80	79	
	83	82	

CARDBUS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 17 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRPHCTLR,667BGA	U44	CRITICAL	M11_CSP128
338S0154	1	IC,ATI,M11-CSP64,GRPHSCTLR,667BGA	U44	CRITICAL	M11_CSP64

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0182	338S0158	M11_CSP128	U44	ALT FOR A16
338S0183	338S0154	M11_CSP64	U44	ALT FOR A16

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)

+3V_SLEEP
L4 FERR-EMI-100-OHM SM
38 +3V_ATI_OSC_SLEEP
C77 0.1uF 20% 10V CERM 402
C78 4.7uF 20% 6.3V CERM 805
NO STUFF R188 100K 5% 1/16W MF 402
CRITICAL
VCC
G2 27.0000M OSC SM-1
OE
OUT
GND
ATI_OSC_OE
ATI_CLK27M_OSC
(PLACE R200 CLOSE TO OSC)
GPU_SS R200 0 5% 1/16W MF 402
ATI_CLK27M_OSC_SS 18
R189 287 1% 1/16W MF 402
ATI_CLK27M_IN 19
R195 162 1% 1/16W MF 402

S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT

+3V_SLEEP
GPU_SS L3 FERR-EMI-100-OHM SM
38 +3V_ATI_SS
GPU_SS C70 10uF 20% 6.3V CERM 805
GPU_SS C71 0.1uF 20% 10V CERM 402
NO STUFF R173 0 5% 1/16W MF 402
GPU_SS R181 0 5% 1/16W MF 402
GPU_SS CRITICAL
VDD U47 CY25811 SOI
ATI_CLK27M_OSC_SS 18
XIN/CLKIN
XOUT
SSCLK
ATI_SSCLK_UF
NC
NC
FRSEL
CY25811_S1
CY25811_S0
S1
S0
VSS
GPU_SS R201 33 5% 1/16W MF 402
ATI_SSCLK_IN 19
NO STUFF R37 0 5% 1/16W MF 402
NO STUFF R38 0 5% 1/16W MF 402

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (1 OF 6)

37 12 AGP_AD<31>	AB30	AD31	
37 12 AGP_AD<30>	AB27	AD30	
37 12 AGP_AD<29>	AA29	AD29	
37 12 AGP_AD<28>	AB28	AD28	
37 12 AGP_AD<27>	AA30	AD27	
37 12 AGP_AD<26>	AA27	AD26	
37 12 AGP_AD<25>	Y30	AD25	
37 12 AGP_AD<24>	AA28	AD24	
37 12 AGP_AD<23>	W30	AD23	
37 12 AGP_AD<22>	W27	AD22	
37 12 AGP_AD<21>	V30	AD21	
37 12 AGP_AD<20>	V28	AD20	
37 12 AGP_AD<19>	V29	AD19	
37 12 AGP_AD<18>	V27	AD18	
37 12 AGP_AD<17>	U30	AD17	
37 12 AGP_AD<16>	U28	AD16	
37 12 AGP_AD<15>	R27	AD15	
37 12 AGP_AD<14>	R29	AD14	
37 12 AGP_AD<13>	P28	AD13	
37 12 AGP_AD<12>	P30	AD12	
37 12 AGP_AD<11>	P27	AD11	
37 12 AGP_AD<10>	P29	AD10	
37 12 AGP_AD<9>	N28	AD9	
37 12 AGP_AD<8>	N30	AD8	
37 12 AGP_AD<7>	M30	AD7	
37 12 AGP_AD<6>	M27	AD6	
37 12 AGP_AD<5>	M29	AD5	
37 12 AGP_AD<4>	L28	AD4	
37 12 AGP_AD<3>	L30	AD3	
37 12 AGP_AD<2>	L27	AD2	
37 12 AGP_AD<1>	L29	AD1	
37 12 AGP_AD<0>	K28	AD0	
37 12 AGP_CBE<3>	W28	CBEB3	
37 12 AGP_CBE<2>	U29	CBEB2	
37 12 AGP_CBE<1>	R30	CBEB1	
37 12 AGP_CBE<0>	N27	CBEB0	
36 12 CLK66M_GPU_AGP	AG30	PCICLK	
37 12 AGP_FRAME_L	U27	FRAMEB	
37 12 AGP_IRDY_L	T30	IRDYB	
37 12 AGP_TRDY_L	T28	TRDYB	
37 12 AGP_STOP_L	T27	STOPB	
37 12 AGP_DEVSEL_L	T29	DEVSELB	
37 12 AGP_PAR	R28	PAR	
37 12 AGP_REQ_L	AF29	REQB	
37 12 AGP_GNT_L	AF27	GNTB	
14 AGP_INT_L	AH29	INTAB	
AGP_ATI_RESET_L	AH30	RSTB	
12 AGP_WBF_L	AE27	WBF	
AGP_ATI_VREFG	AK3	VREFG	
AGP_ATI_VREF	D8	MVREF	

AD_STB0	N29	AGP_AD_STB<0>	12 37
AD_STB1	W29	AGP_AD_STB<1>	12 37
AD_STBB0	M28	AGP_AD_STB_L<0>	12 37
AD_STBB1	Y29	AGP_AD_STB_L<1>	12 37
AGP_BUSYB	AG28	AGP_BUSY_L	12
AGPREF	K30		
AGPTEST	K29	GPU_AGP_TEST	
AGP8X_DETB	U25	AGP8X_DET_PU	
SUS_STAT	AJ28	AGP_SUS_STAT_L_PU	
ST0	AF30	AGP_ST<0>	12
ST1	AF28	AGP_ST<1>	12
ST2	AE29	AGP_ST<2>	12
SBA7	AC28	AGP_SBA<7>	12 37
SBA6	AB29	AGP_SBA<6>	12 37
SBA5	AC27	AGP_SBA<5>	12 37
SBA4	AC30	AGP_SBA<4>	12 37
SBA3	AD27	AGP_SBA<3>	12 37
SBA2	AD30	AGP_SBA<2>	12 37
SBA1	AE28	AGP_SBA<1>	12 37
SBA0	AD29	AGP_SBA<0>	12 37
RBFB	AE30	AGP_RBF_L	12 37
STP_AGPB	AG29	AGP_STP_L	
SB_STB	AC29	AGP_SB_STB	12 37
SB_STBS	AD28	AGP_SB_STB_L	12 37
RSTB_MSK	AD24	ATI_RSTB_MSK	
DBI_LO	Y25	ATI_DBI_LO_PU	
DBI_HI	Y27	ATI_DBI_HI_PU	

38 21 19 18 12 +3V_GPU
38 21 19 18 16 15 12 +1_5V_AGP
R119 47 5% 1/16W MF 402
R127 10K 5% 1/16W MF 402
R159 20K 5% 1/16W MF 402
INT_AGP_VREF 12 38
C62 0.1uF 20% 16V CERM 402
C63 0.01uF 20% 16V CERM 402
(PLACE C1002 CLOSE TO AGPREF PIN)
OMIT
38 21 19 18 12 +3V_GPU
R172 20K 5% 1/16W MF 402
R158 0 5% 1/16W MF 402
38 21 19 18 12 +3V_GPU
MAIN_RESET_L IS TOGGLED FOR SLEEP
R54 10K 5% 1/16W MF 402
24 20 17 14 39 30 26 MAIN_RESET_L
R53 47 5% 1/16W MF 402
21 19 18 12 38 +3V_GPU
R43 1K 1% 1/16W MF 402
R44 1K 1% 1/16W MF 402
38 21 18 +GPU_MEM
R45 1K 1% 1/16W MF 402
R46 1K 1% 1/16W MF 402
PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN
C11 0.1uF 20% 16V CERM 402
C37 10uF 20% 6.3V CERM 805
38 21 20 19 +1_8V_GPU
ATI_MEMIO_LO R55 4.7K 5% 1/16W MF 402
ATI_MEMIO_HI R104 4.7K 5% 1/16W MF 402
ATI_MEMVMODE0
ATI_MEMVMODE1
ATI_MEMIO_HI R70 4.7K 5% 1/16W MF 402
ATI_MEMIO_LO R105 4.7K 5% 1/16W MF 402
FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V
+1_5V_AGP
R126 47K 5% 1/16W MF 402
R138 47K 5% 1/16W MF 402

D+	AC10	GPU_THERM_DP_TP	
D-	AC11	GPU_THERM_DM_TP	
		+GPU_MEM	18 21 38
TEST_YCLK	E8	(PULL-UP to GPU_MEM_IO)	
TEST_MLCK	J6		
MEMTEST	C8	ATI_MEMTEST	
PLLTEST	AC22	NC	

R118 45.3 1% 1/16W MF 402

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (6 OF 6)

OMIT

	M2		
	P3		
	A21		
	B19		
	M15		
	N15		
	P15		
VSS	R15		
	T15		
	T12		
	T13		
	T14		
	W16		
	V16		
	U16		
	T16		
	R16		
	R17		
	R18		
	R19		
	U6		
	AE15		
VDDCI	F18		
	P25		

39 38 19 GPU_VCORE
L2 60-OHM-EMI SM
38 GPU_VCORE_VDDCI
C64 0.01uF 20% 16V CERM 402
C67 10uF 20% 6.3V CERM 805
C65 0.01uF 20% 16V CERM 402
C68 0.01uF 20% 16V CERM 402
C66 0.01uF 20% 16V CERM 402
C69 0.01uF 20% 16V CERM 402

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (2 OF 6)

OMIT

B26		A17	
A26		B16	
B25		A16	
A25		B14	
C22		A14	
D21		B13	
C21		A13	
D20		D13	
C20		C13	
D22		D12	
C23		C12	
D23		D10	
A27		C10	
B27		D9	
H2		C9	
H1		B12	
J2		A12	
J1		B11	
K4		A11	
K3		B9	
L4		A9	
M3		B8	
L3	VSS	A8	VSS
M4		C7	
N2		D7	
N1		C6	
N4		D6	
N3		C4	
G30		D4	
G28		C3	
B30		D3	
D26		A5	
D16		B5	
B15		A4	
D11		B4	
B10		A2	
D5		B2	
B3		A1	
G3		B1	
E1		E4	
U1		E3	
V3		F3	
AB1		F4	
AC3		H3	
J30		H4	
J29		J3	
H30		J4	
H29		C1	
F30		C2	
F29		D1	
E30		D2	
E29		F1	
J28		F2	
J27		G1	
H28		G2	
H27		R1	
F28		R2	
F27		T1	
E28		T2	
E27		V1	
D30	VSS	V2	VSS
D29		W1	
C30		W2	
C29		T3	
A30		T4	
A29		U3	
A28		U4	
B28		W3	
D28		W4	
C28		Y3	
D27		Y4	
C27		Y1	
D25		Y2	
C25		AA1	
D24		AA2	
C24		AC1	
D18		AC2	
C18		AD1	
D17		AD2	
C17		AA3	
D15		AA4	
C15		AB3	
D14		AB4	
C14		AD3	
B17		AD4	
		AE3	
		AE4	

M10 AGP INTERFACE

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 18 OF 44	

TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (3 OF 6)

OMIT

EXT_TMDS R228 10K 5% 1/16W MF 402 — +1_8V_GPU
INT_TMDS R234 10K 5% 1/16W MF 402 — +3V_GPU
ZV_LCDDATA20_PU

GPU_DVOD<0> … GPU_DVOD<11> → ZV_LCDDATA0 … ZV_LCDDATA23

GPU_DVO_VSYNC → ZV_LCDCNTL0
GPU_DVO_HSYNC → ZV_LCDCNTL1
GPU_DVOD_DE → ZV_LCDCNTL2
GPU_DVO_CLKP → ZV_LCDCNTL3

ATI_AGP_FBSKEW<0> → GPIO0
ATI_AGP_FBSKEW<1> → GPIO1
ATI_X1CLK_SKEW<0> → GPIO2
ATI_X1CLK_SKEW<1> → GPIO3
ATI_BUS_CFG<0> → GPIO4
ATI_BUS_CFG<1> → GPIO5
ATI_BUS_CFG<2> → GPIO6
ATI_GPIO7_SPN → GPIO7
ATI_GPIO8_RD (NO ICT TEST) → GPIO8
ATI_GPIO9_SPN (NO ICT TEST) → GPIO9
ATI_GPIO10_SPN (NO ICT TEST) → GPIO10
ATI_GPIO11_SPN (NO ICT TEST) → GPIO11
ATI_GPIO12_SPN (NO ICT TEST) → GPIO12
ATI_GPIO13_SPN → GPIO13
HPD_PWR_SNS_EN → GPIO14
GPU_VCORE_CNTL_L → GPIO15
ATI_SSCLK_IN → GPIO16

NO STUFF R223 10K 5% 1/16W MF 402 — +3V_GPU
R221 1K 1% 1/16W MF 402

ATI_TMDS_DN<0> → TX0M
ATI_TMDS_DP<0> → TX0P
ATI_TMDS_DN<1> → TX1M
ATI_TMDS_DP<1> → TX1P
ATI_TMDS_DN<2> → TX2M
ATI_TMDS_DP<2> → TX2P
ATI_TMDS_CLKN → TXCM
ATI_TMDS_CLKP → TXCP

ATI_CLK27M_IN → XTALIN
R229 1K 5% 1/16W MF 402 — XTALOUT
ATI_TESTEN → TESTEN
SSIN

VSS B24, VSS B20, VSS A24

ROMCSB AE5 NC
R AK28 — GPU_R
G AK27 — GPU_G
B AK26 — GPU_B
VSYNC AG27 — ATI_VSYNC
V2SYNC AG25 NC
HSYNC AG26 — ATI_HSYNC
H2SYNC AG24 NC
RSET AK25 — ATI_RSET
R2SET AJ24 — ATI_R2SET
Y_G AK23 — GPU_Y
C_R AK24 — GPU_C
COMP_B AK22 — GPU_COMP
DIGON AE13 — FP_PWR_EN
BLON AF13 — INV_ON_PWM
HPD1 AF11 — +3V_GPU

R240 75 1% 1/16W MF 402
R246 75 1% 1/16W MF 402
R249 75 1% 1/16W MF 402
R256 715 1% 1/16W MF 402
R257 499 1% 1/16W MF 402
R245 75 1% 1/16W MF 402
R248 75 1% 1/16W MF 402
R254 75 1% 1/16W MF 402
R711 10K 5% 1/16W MF 402

AUXWIN AJ27 — GPU_AUXWIN
R247 10K 5% 1/16W MF 402
R253 10K 5% 1/16W MF 402

DDC1DATA AH28 — GPU_DVI_DDC_DATA
DDC1CLK AH27 — GPU_DVI_DDC_CLK
DDC2DATA AE12 — LVDS_DDC_DATA
DDC2CLK AF12 — LVDS_DDC_CLK
DDC3DATA AH26 — SI_DDC_DATA
DDC3CLK AH25 — SI_DDC_CLK

TXOUT_U0N AH18 — LVDS_U0N
TXOUT_U0P AG18 — LVDS_U0P
TXOUT_U1N AH19 — LVDS_U1N
TXOUT_U1P AG19 — LVDS_U1P
TXOUT_U2N AH20 — LVDS_U2N
TXOUT_U2P AG20 — LVDS_U2P
TXOUT_U3N AH22 — LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P AG22 — LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN AH21 — CLKLVDS_UN
TXCLK_UP AG21 — CLKLVDS_UP
TXOUT_L0N AK16 — LVDS_L0N
TXOUT_L0P AJ16 — LVDS_L0P
TXOUT_L1N AK17 — LVDS_L1N
TXOUT_L1P AJ17 — LVDS_L1P
TXOUT_L2N AK18 — LVDS_L2N
TXOUT_L2P AJ18 — LVDS_L2P (NO ICT TEST)
TXOUT_L3N AK20 — LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P AJ20 — LVDS_L3P_TP
TXCLK_LN AK19 — CLKLVDS_LN
TXCLK_LP AJ19 — CLKLVDS_LP
SSOUT AJ25 NC

VSS A20, VSS B21

+1_5V_AGP → Q77 SI3446DV TSOP → GPU_CORE_OK
+GPU_VDD15_UF
L24 FERR-220-OHM 0805 — +1_5V_GPU_VDD15 (500mA)
C166 1000pF 10% 25V X7R 402

C222 C256 C299 C305 0.01uF 20% 16V CERM 402
C328 10uF 20% 6.3V CERM 805
C232 C269 C300 C306 0.01uF 20% 16V CERM 402

VDD15: F12, L6, T6, AB6, F17, G25, R25, AB25
OMIT: AJ3, AF25, AG4, AH4, AF5, F6, G6, H6, P6, AD26, V6, W6, AC6, AD6, AE6, F7, F10, AE10, F11, AE11, F13, F14, AE14, AF14, W26, AF15, AE17, AC25, AE18, F23, F24, AE24, F25, M25, N25, W25, V25
VDDC: G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G17, G18, G19, G20, G21, G22, G23, G24, H7, H8, H23, H24, J7, J24, K7, K24, L7, L24, M7, M24, N7, N24, P7, P24, R7, R24, T7, T24, U7, U24, V7, V24, W7, W24, Y7, Y24, AA7, AA24, AB7, AB24, AC7, AC8, AC23, AC24, AD7, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23
VSS: G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G17, G18, G19, G20, G21, G22, G23, G24, H7, H8, H23, H24, J7, J24, K7, K24, L7, L24, M7, M24, N7, N24, P7, P24, R7, R24, T7, T24, U7, U24, V7, V24, W7, W24, Y7, Y24, AA7, AA24, AB7, AB24, AC7, AC8, AC23, AC24, AD7, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

GPU_VCORE
C167 C219 C252 C270 C301 C307 C329 10uF 20% 6.3V CERM 805
C332 0.22uF 20% 6.3V CERM 402
C186 C220 C253 C271 C302 C311 C330 C333 0.22uF 20% 6.3V CERM 402
C187 C221 C254 C282 C303 C326 C331 C338 0.22uF 20% 6.3V CERM 402

M10 Power Shut down Sequencing

+2_5V_SLEEP
XW21 SM — DP6 BAS16TW SOT-363 — XW24 SM
+1_8V_ATI_PVDD
+1_8V_PVDD_NECK
XW20 SM — DP6 BAS16TW SOT-363 — +1_5V_AGP_NECK
GPU_VCORE
GPU_VCORE_NECK
XW22 SM — DP6 BAS16TW SOT-363 — XW23 SM
+GPU_VDD15_UF
+GPU_VDD15_NECK

R258 R260 10K 5% 1/16W MF 402 — +3V_GPU
NO STUFF R262 R265 R269 R271 R273 10K 5% 1/16W MF 402
NO STUFF R259 R261 R263 R266 R270 R272 R274 10K 5% 1/16W MF 402

(GPIO0) ATI_AGP_FBSKEW<0>
(GPIO1) ATI_AGP_FBSKEW<1>
(GPIO2) ATI_X1CLK_SKEW<0>
(GPIO3) ATI_X1CLK_SKEW<1>
(GPIO4) ATI_BUS_CFG<0>
(GPIO5) ATI_BUS_CFG<1>
(GPIO6) ATI_BUS_CFG<2>

GPU VCORE SUPPLY

+PBUS

R389 1M 5% 1/16W MF 402
R430 1 5% 1/16W MF 603
R339 576K 1% 1/16W MF 402

C762 C766 4.7UF 20% 25V CERM 1206

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)

Q51 SI7860DP SO-8-PWRPK CRITICAL

NO STUFF R388 0 5% 1/16W MF 402
NO STUFF R341 63.4K 1% 1/16W MF 402
C473 4.7UF 20% 10V CERM 1206 — 1778_GND
1778_VCC
1778_VIN
C494 0.1uF 20% 25V CERM 603

+5V_MAIN
U16 LTC1778 SSOP — CRITICAL
EXT_VCC INT_VCC VIN
RUN/SS ITH VRNG FCB PGOOD SGND PGND
TG BOOST SW BG VFB ION
1778_ITH 1778_VRNG 1778_FCB GPU_CORE_OK 1778_SHDN_L 1778_BST 1778_TG 1778_BG 1778_VFB 1778_ION

R236 100K 5% 1/16W MF 402
R390 0 5% 1/16W MF 402
R340 20K 1% 1/16W MF 402
C451 220pF 5% 25V CERM 402
C448 470pF 10% 50V CERM 402
R311 R332 0 5% 1/16W MF 402
C483 0.1uF 20% 10V CERM 402

D5 SM MBR0540
R416 2.2 5% 1/16W MF 603
1778_BST_RC
C514 0.1uF 20% 25V CERM 603
NO STUFF C882 0.0022UF 20% 10V CERM 402
OMIT XW2 SM

CRITICAL Q48 SI7892DP SO-8-PWRPK
GPU_VCORE_SW
L30 2.1UH-11A SM
D24 SMB B340LB

C708 22uF 20% 10V CERM 1210
C719 330UF 20% 6.3V POLY SMD
C721 330UF 20% 6.3V POLY SMD
C720 330UF 20% 6.3V POLY SMD

R352 4.99K 1% 1/16W MF 402 — 1778_VFB
R451 18.2K 1% 1/16W MF 402 — GPU_PWRMSR
R351 20K 1% 1/16W MF 402 — HIGH_VCORE
R804 1.82K 1% 1/16W MF 402
R307 100K 5% 1/16W MF 402
C902 0.1UF 20% 10V CERM 402
R410 10K 5% 1/16W MF 402 — VCORE_CNTL_RC
C515 0.1uF 20% 10V CERM 402
Q80 2N7002DW SOT-363

R203 33K 5% 1/16W MF 402
Q5 2N3904 SM
Q6 2N3904 SM
R294 10K 5% 1/16W MF 402
R306 R316 100K 5% 1/16W MF 402
DP1 BAS16TW SOT-363 — GPU_VCORE_PWR_SEQ
SLEEP_L_LS5
DCDC_EN
1778_SHDN_L_D3COLD

+5V_MAIN
+1_5V_AGP
GPU_VCORE_SEQ_L
GPU_VCORE_SEQ

M10 CORE PWR/LVDS/TMDS

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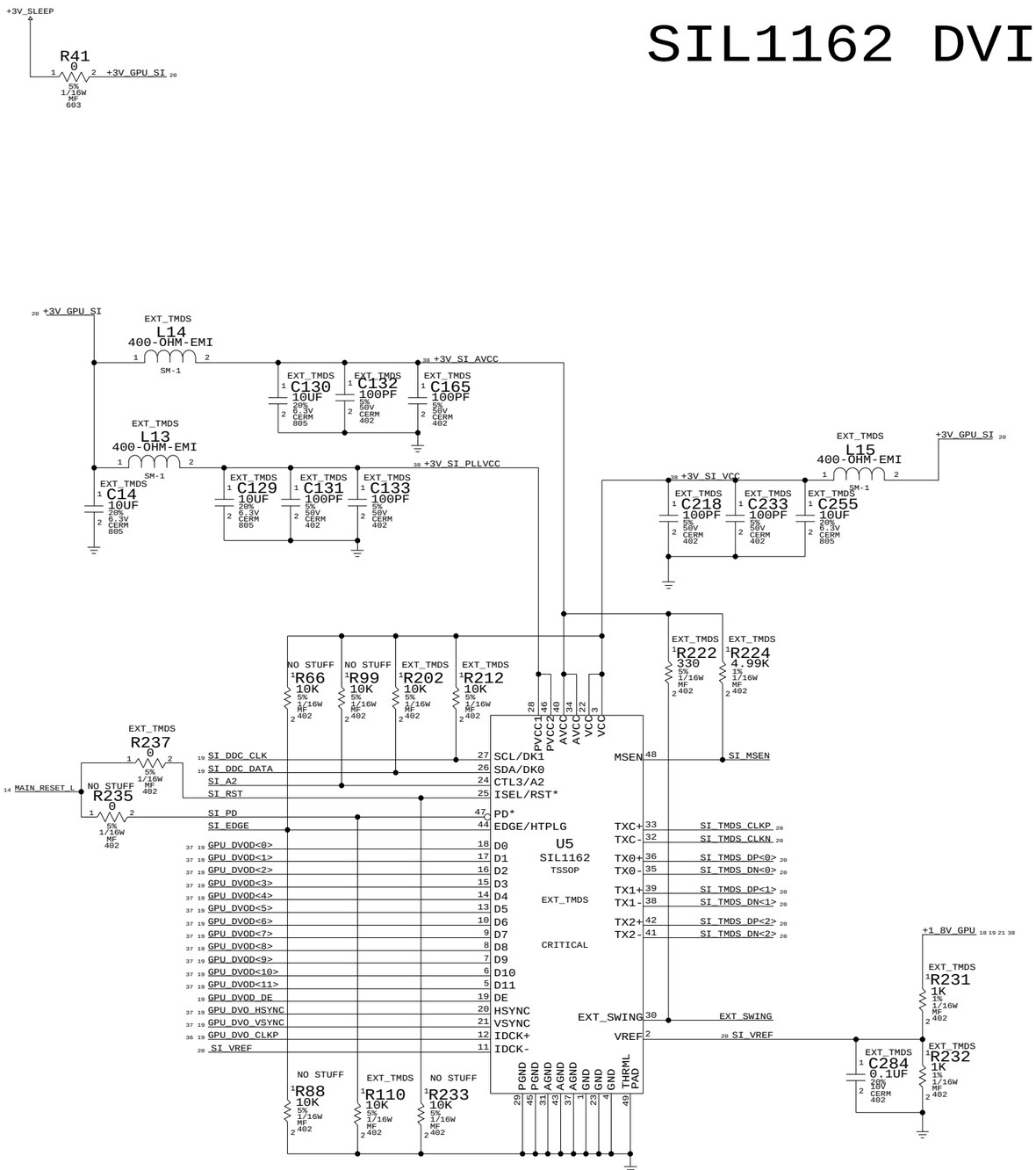
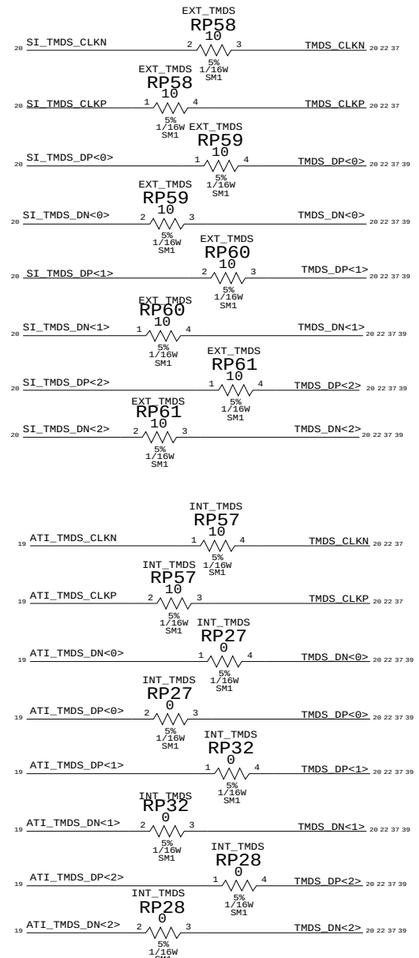
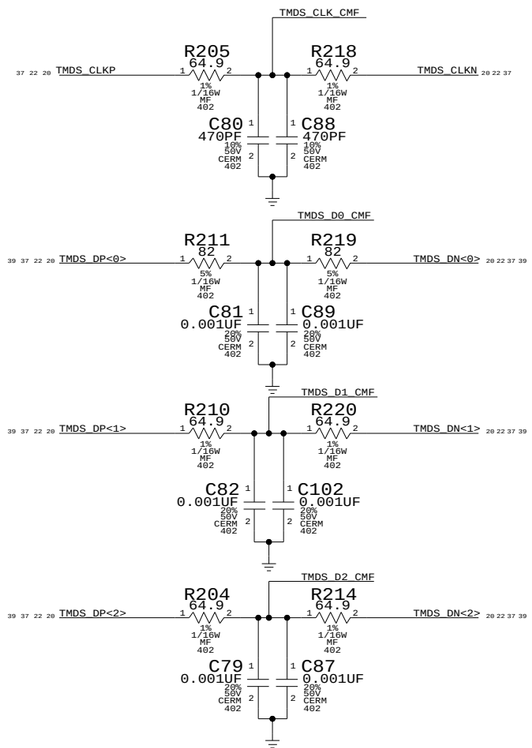
SCALE: NONE	SHT 19 OF 44	

SIL1162 DVI TRANSMITTER







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SIZE	DRAWING NUMBER	REV.
D	051-6654	C

SCALE	SHT	OF
NONE	20	44

GPU PLL - 1.8V

U55 MM1571J (100mA MAX) SOT-25A CRITICAL
(Total PVDD = 66mA)
+2_5V_GPU → VIN; VOUT → +1_8V_ATI_PVDD
GPU_CORE_OK; CONT; NOISE; ATI_PVDD_BYP; GND
C889 1UF 10% 6.3V CERM 603
C379 0.01uF 20% 16V CERM 402
C380 10uF 20% 6.3V CERM 805

L65 FERR-220-OHM 0402: +1_8V_ATI_PVDD → +1_8V_GPU_PLL
C438 10uF 20% 6.3V CERM 805
C865 0.1uF 20% 10V CERM 402
C716 0.01uF 20% 16V CERM 402 (21mA)

L66 FERR-220-OHM 0402: +1_8V_GPU → +1_8V_GPU_AVDD
C415 10uF 20% 6.3V CERM 805
C437 0.01uF 20% 16V CERM 402
C870 0.01uF 20% 16V CERM 402
(AVDD+VDDDI=75mA)

L58 FERR-220-OHM 0402: +2_5V_GPU → +2_5V_GPU_A2VDD (140mA)
C360 10uF 20% 6.3V CERM 805
C364 0.01uF 20% 16V CERM 402
C374 0.01uF 20% 16V CERM 402

L55 FERR-220-OHM 0402: +1_8V_GPU → +1_8V_GPU_AVDDQ (2mA)
C339 10uF 20% 6.3V CERM 805
C363 0.01uF 20% 16V CERM 402

L56 FERR-220-OHM 0402: +1_8V_GPU → +1_8V_GPU_VDDDI (AVDD+VDDDI=75mA)
C358 10uF 20% 6.3V CERM 805
C361 0.01uF 20% 16V CERM 402
C372 0.01uF 20% 16V CERM 402

L57 FERR-220-OHM 0402: +GPU_MEM → +GPU_MCLK
C359 10uF 20% 6.3V CERM 805
C362 0.01uF 20% 16V CERM 402
C373 0.01uF 20% 16V CERM 402

+1_5V_SLEEP → R722 0 5% 1/10W FF 805 → +1_5V_AGP
1.5V

+1_8V_SLEEP → R284 0 5% 1/10W FF 805 → +1_8V_GPU
1.8V

+1_8V_SLEEP; +2_5V_SLEEP; ATI_MEMIO_LO → R729 0 5% 1/4W FF 1210; ATI_MEMIO_HI → R728 0 5% 1/4W FF 1210 → +GPU_MEM
1.8V 2.5V

AGP 4X I/O - 1.5V

+1_5V_AGP → L59 FERR-10-OHM-500MA SM → +1_5V_AGP_GPU (20mA)
C381 0.1uF 20% 10V CERM 402
C420 0.1uF 20% 10V CERM 402
C446 0.1uF 20% 10V CERM 402
C543 0.1uF 20% 10V CERM 402
C871 10uF 20% 6.3V CERM 805
C382 0.01uF 20% 16V CERM 402
C421 0.01uF 20% 16V CERM 402
C447 0.01uF 20% 16V CERM 402
C671 0.01uF 20% 16V CERM 402

MEMORY CORE - 2.5V

+GPU_MEM → L63 FERR-220-OHM 0805 → +GPU_MEMCORE (1800mA)
C383 0.1uF 20% 10V CERM 402
C425 0.1uF 20% 10V CERM 402
C866 0.1uF 20% 10V CERM 402
C672 0.1uF 20% 10V CERM 402
C715 10uF 20% 6.3V CERM 805
C408 0.01uF 20% 16V CERM 402
C426 0.01uF 20% 16V CERM 402
C450 0.01uF 20% 16V CERM 402
C701 0.01uF 20% 16V CERM 402

LVDS PLL - 1.8V

+1_8V_ATI_PVDD → L61 FERR-220-OHM 0402 → +1_8V_GPU_PNLPLL (40mA)
C409 10uF 20% 6.3V CERM 805
C428 0.01uF 20% 16V CERM 402
C867 0.01uF 20% 16V CERM 402
EXT_TMDS R279 0 5% 1/16W MF 603 → +1_8V_GPU_TP_PLL
C877 10uF 20% 6.3V CERM 805
C878 0.01uF 20% 16V CERM 402

MEMORY PLL - 1.8V

+1_8V_ATI_PVDD → L62 FERR-220-OHM 0402 → +1_8V_GPU_MEMPLL (20mA)
C411 10uF 20% 6.3V CERM 805
C429 0.01uF 20% 16V CERM 402

LVDS - 2.5V

+2_5V_GPU → NO STUFF L64 FERR-10-OHM-500MA SM
+3V_GPU → U8 MAX8860 UMAX (OMIT)
IN; SHDN*; SET; GND; OUT1; OUT2; FAULT*; CC
C910 2.2UF 20% 6.3V CERM1 603
C911 0.033UF 20% 10V X7R 402
R635 100K 5% 1/10W MF 402 → +2_8V_GPU_LVDS_LDO
C912 2.2UF 20% 6.3V CERM1 603
MAX8860_CC; MAX8860_FAULT
L17 FERR-10-OHM-500MA SM
C412 10uF 20% 6.3V CERM 805
C434 0.01uF 20% 16V CERM 402
C868 0.01uF 20% 16V CERM 402
(350mA)

LVDS/TMDS - 1.8V

+1_8V_GPU → L60 FERR-220-OHM 0402 → +1_8V_GPU_PNLIO (180mA)
C413 10uF 20% 6.3V CERM 805
C435 0.1uF 20% 10V CERM 402
C864 0.1uF 20% 10V CERM 402
C704 0.1uF 20% 10V CERM 402
C414 0.1uF 20% 10V CERM 402
C436 0.01uF 20% 16V CERM 402
C869 0.01uF 20% 16V CERM 402

+2_5V_SLEEP → R721 0 5% 1/10W FF 805 → +2_5V_GPU
2.5V

+3V_SLEEP → R299 0 5% 1/10W FF 805 → +3V_GPU
3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0828	1	IC,MAX8860,LDO,2.77V	U8	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S0828	?	U8	ALT FOR 2.82V PART

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (4 OF 6) (OMIT)

AK29 PVDD	PVSS AK30	
AF23 AVDD0	AVSSQ AF22	
AF24 AVDD1	A2VSSQ AJ22	
AE21 A2VDD0	AVSSN0 AE22	
AF21 A2VDD1	AVSSN1 AE23	
AJ23 A2VDDQ	A2VSSN0 AE19	
AH23 VDD1DI	A2VSSN1 AE20	
AF20 VDD2DI	VSS1DI AG23	
F19 VDDRH0	VSS2DI AF19	
N6 VDDRH1	VSSRH0 F20	
K25	VSSRH1 M6	
L25	F5	
T25	G5	
Y28	H5	
K27	J5	
AA25	K5	
K26	L5	
L26	M5	
M26	N5	
N26	P5	
P26 VDDP	R5	
R26	T5	
T26	U5	
U26	V5	
V26	W5	
Y26	Y5	
AA26	AA5	
AB26	AB5	
AC26	AC5	
	AD5	
	G26	
	K6	
	R6	
	Y6	
	AA6	
E5	F8	
E6	F9	
E12	F15	
E13	F16	
E18 VDDM	F21	
E19	F22	
E20	H25	
E26	J25	
F26	J26	
E7	AF6	
H26	AE7	
E9	AF7	
E10	AE8	
E11	AF8	
E14	AE9	
E15	AF9	
E16 VDDR1	AF10	
E17	AD25	
E21	AE25	
E22	AE26	
E23	AF26	
E24	LPVSS AJ21	
E25	TPVSS AJ11	
AK21 LPVDD	MPVSS A6	
AK11 TPVDD	LVSSR0 AH16	
A7 MPVDD	LVSSR1 AG17	
AE16 LVDDR_18	LVSSR2 AH17	
AF16 LVDDR_18	LVSSR3 AF18	
AG16 LVDDR_25	DVOVMODE AH12	
AF17 LVDDR_25	TXVSSR1 AH13	
AG12 TXVDDR0	TXVSSR2 AH14	
AG13 TXVDDR1	TXVSSR3 AH15	
AG14 TXVDDR2		
AG15 TXVDDR3		

MEMORY I/O

+2_5V_GPU → U54 MM1571J (CRITICAL) SOT-25A
INT_TMDS GPU_CORE_OK; CONT; NOISE; ATI_TPVDD_BYP; GND
C879 1UF 10% 6.3V CERM 603
+1_8V_ATI_TPVDD → L69 FERR-220-OHM 0402 → +1_8V_GPU_TP_PLL
C881 10UF 20% 6.3V CERM 805
C880 0.01UF 10% 16V CERM 402

+GPU_MEM → L67 FERR-220-OHM 0805
(1200mA) +GPU_MEM_IO_FLT
C872 10uF 20% 6.3V CERM 805
C875 0.1uF 20% 10V CERM 402
C850 0.1uF 20% 10V CERM 402
C855 0.1uF 20% 10V CERM 402
C860 0.1uF 20% 10V CERM 402
C873 0.1uF 20% 10V CERM 402
C876 0.1uF 20% 10V CERM 402
C851 0.1uF 20% 10V CERM 402
C856 0.1uF 20% 10V CERM 402
C861 0.1uF 20% 10V CERM 402
C874 0.1uF 20% 10V CERM 402
C847 0.1uF 20% 10V CERM 402
C852 0.1uF 20% 10V CERM 402
C857 0.1uF 20% 10V CERM 402
C862 0.01uF 20% 16V CERM 402

3.3V IO SUPPLY

(Max Current varies, depends on usage)

+1_8V_DVO_F
C304 10uF 20% 6.3V CERM 805
C327 0.1uF 20% 10V CERM 402
C647 0.1uF 20% 10V CERM 402

EXT_TMDS → L16 FERR-10-OHM-500MA SM → +1_8V_GPU
INT_TMDS R268 0 5% 1/16W MF 603

+3V_GPU ← L68 FERR-10-OHM-500MA SM ← +3V_GPU_FLT
C722 10uF 20% 6.3V CERM 805
C848 0.1uF 20% 10V CERM 402
C853 0.1uF 20% 10V CERM 402
C858 0.1uF 20% 10V CERM 402
C863 0.1uF 20% 10V CERM 402
C725 0.1uF 20% 10V CERM 402
C849 0.1uF 20% 10V CERM 402
C854 0.1uF 20% 10V CERM 402
C859 0.1uF 20% 10V CERM 402

EXT_TMDS R255 0 5% 1/16W MF 402 → +1_8V_GPU
INT_TMDS R251 0 5% 1/16W MF 402

M10 SHUT DOWN POWER SEQUENCING

+2_5V_SLEEP → XW27 SM (OMIT) → DP7 BAS16TW SOT-363 → +3V_SLEEP_NECK → XW30 SM (OMIT) → +3V_SLEEP
+1_8V_SLEEP → XW28 SM (OMIT) → DP7 BAS16TW SOT-363 → +1_8V_SLEEP_NECK
+1_5V_SLEEP → XW29 SM (OMIT) → DP7 BAS16TW SOT-363 → +1_5V_SLEEP_NECK

M10 POWER

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D	051-6654	C
SCALE: NONE	SHT 21 OF 44	

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 CRITICAL LCFILTER SM-220MHZ — GPU_B → VGA_B
FL1 CRITICAL LCFILTER SM-220MHZ — GPU_G → VGA_G
FL3 CRITICAL LCFILTER SM-220MHZ — GPU_R → VGA_R
C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

+3V_MAIN
CRITICAL U56 74AHC1G32 SM — ATI_HSYNC → R718 33 5% 1/10W MF 402 → VGA_HSYNC_BUF → VGA_HSYNC
CRITICAL U57 74AHC1G32 SM — ATI_VSYNC → R714 33 5% 1/10W MF 402 → VGA_VSYNC_BUF → VGA_VSYNC

VGA VSYNC BUFFERS

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP

Isolation required for DVI power switch

D21 SM MBR0530 — DDC_CLK_ISO

CRITICAL J14 QH1112 F-RT-TH

TMDS_CONN_DN<0>	17	1	TMDS_CONN_DN<2>
	9	2	TMDS_CONN_DP<2>
TMDS_CONN_DP<0>	18	10	TMDS_CONN_DP<1>
	19	3	
(TMDS_DN<5>)	NC 20	4 NC	(TMDS_DN<4>)
	NC 12	5 NC	(TMDS_DN<3>)
(TMDS_DP<5>)	NC 21	11 NC	(TMDS_DP<4>)
	13	6	(TMDS_DP<3>)
	22	14	(+5V_DDC_SLEEP)
TMDS_CONN_CLKP	23	7	DVI_DDC_DATA_UF
TMDS_CONN_CLKN	24	15	DVI_DDC_CLK_UF
	16	8	VGA_VSYNC
VGA_B	C3	C1	VGA_R
VGA_HSYNC	C4	C5A	
	C5B	C2	VGA_G
	34	32	
		35	

R661 4.7K 5% 1/16W MF 402 — R655 4.7K 5% 1/16W MF 402
R670 100 5% 1/16W MF 402 — DVI_DDC_CLK
R649 100 5% 1/16W MF 402 — DVI_DDC_DATA
R650 100 5% 1/16W MF 402 — DVI_HPD
C706 100pF 5% 50V CERM 402
C669 100pF 5% 50V CERM 402
C1 100pF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
R706 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
CHGND5 CHGND1

3V LEVEL SHIFTERS

+3V_SLEEP
Q38 2N7002DW SOT-363 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
Q38 2N7002DW SOT-363 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
Q35 2N7002DW SOT-363 — DVI_HPD → GPU_HPD
R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, +5V_will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q40 TP0610 SM — DVI_DDC_CLK_UF → DVI_TURN_ON → DVI_TRUN_ON_ILIM
R690 680 5% 1/16W MF 402
R688 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
R691 10K 5% 1/16W MF 402 — DVI_TURN_ON_BASE
Q42 2N3904 SM — SOFT_PWR_ON_L

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R680 68.1K 1% 1/16W MF 402 — HPD_4V_REF
C696 0.1UF 20% 10V CERM 402
U46 LMC7211 SM CRITICAL — DVI_HPD_UF → DVI_HPD_DIV → HPD_PWR_SW → HPD_ON
R663 10K 1% 1/16W MF 402
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
Q41 2N7002DW SOT-363
R703 330 5% 1/16W MF 402
+PBUS
Q45 TP0610 SM — COMP_ENABLE
R696 100K 5% 1/16W MF 402 — COMP_DISABLE
R704 100K 5% 1/16W MF 402
HPD_ON_RC
R700 20K 5% 1/16W MF 402 — HPD_BASE
Q44 2N3904 SM
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
HPD_PWR_SNS_EN
Q41 2N7002DW SOT-363
R213 100K 5% 1/16W MF 402

TMDS FILTERING PLACE CLOSE TO CONNECTOR

CRITICAL L72 90-OHM-300MA 2012H SYM_VER-1 — TMDS_DN<0> → TMDS_CONN_DN<0>
CRITICAL L73 90-OHM-300MA 2012H SYM_VER-1 — TMDS_DP<0> → TMDS_CONN_DP<0>
CRITICAL L21 165-OHM SM SYM_VER-2 OMIT — TMDS_CLKP → TMDS_CONN_CLKP; TMDS_CLKN → TMDS_CONN_CLKN
CRITICAL L74 90-OHM-300MA 2012H SYM_VER-1 — TMDS_DN<2> → TMDS_CONN_DN<2>
CRITICAL L73 90-OHM-300MA 2012H SYM_VER-1 — TMDS_DP<1> → TMDS_CONN_DP<1>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
155S0147	1	370OHM COMMON MODE CHOKE	L21	?

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

LCD INTERFACE

LVDS INTERFACE

C416 0.001uF 20% 50V CERM 402 — CHGND4
CRITICAL J6 G-501973 F-RT-SM 34
+3V_SLEEP
R342 100K 5% 1/16W MF 402 — LVDS_DDC_CLK
R320 100K 5% 1/16W MF 402 — LVDS_DDC_DATA
+3V_LCD — (LVDS DDC POWER) — NC
NO STUFF
C449 0.001uF 20% 50V CERM 402
C452 0.001uF 20% 50V CERM 402 — CHGND4

LVDS_L0N	8	
LVDS_L0P	9	
LVDS_L1N	11	
LVDS_L1P	12	
LVDS_L2N	14	
LVDS_L2P	15	
CLKLVDS_LN	17	
CLKLVDS_LP	18	
LVDS_U0N	20	
LVDS_U0P	21	
LVDS_U1N	23	
LVDS_U1P	24	
LVDS_U2N	26	
LVDS_U2P	27	
CLKLVDS_UN	29	
CLKLVDS_UP	30	

C500 0.001uF 20% 50V CERM 402 — CHGND4

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6 — +5V_INV_UF_SW
R317 100K 5% 1/16W MF 402 — FP_PWR_EN_L
L32 400-OHM-EMI SM-1
C440 10UF 20% 6.3V CERM 805
Q7 FDG6324L SC70-6 — FP_PWR_EN
+5V_INV_SW
CRITICAL J7 SM-2MT
C746 0.001UF 20% 50V CERM 402
C749 0.001UF 20% 50V CERM 402
L31 400-OHM-EMI SM-1 — BRIGHT_PWM
C739 0.001UF 20% 50V CERM 402
CHGND2
+3V_PMU
C552 0.1UF 20% 10V CERM 402
74LVC32 TSSOP — INV_ON_PWM → U24 32 → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01uF 20% 50V CERM 603 — CHGND2

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1 → TV_GND1
L26 FERR-10-OHM-500MA SM
C712 0.01UF 20% 50V CERM 603
L25 3.3UH 0603 — GPU_Y → TV_C
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
L29 3.3UH 0603 — GPU_C → TV_Y
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
CRITICAL J15 MINIDIN RT-TH MH1177 — TV_COMP
L27 3.3UH 0603 — GPU_COMP
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402
XW13 SM — GPU_TV_GND2
L28 FERR-10-OHM-500MA SM — TV_GND2
C717 0.01UF 20% 50V CERM 603
CHGND1

Place GND shorts at graphics controller

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603
R391 100K 5% 1/16W MF 402 — LCD_PWREN_L
+3V_LCD_SW
L6 FERR-250-OHM SM
C474 0.001uF 20% 50V CERM 402 — CHGND4
LCD_DIGON_L
SI3443DV TSOP Q11
Q8 2N7002 SM — FP_PWR_EN

VIDEO CONNECTORS

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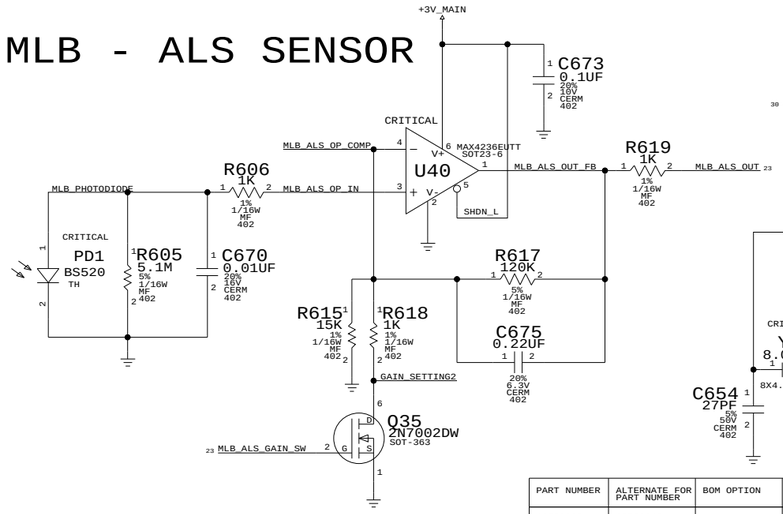
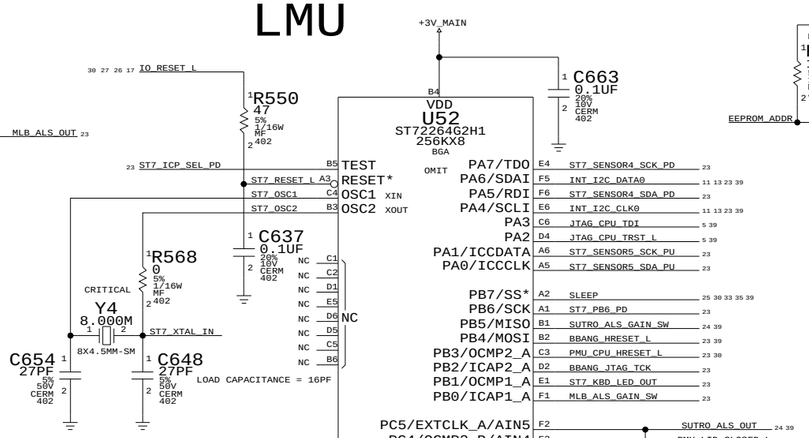
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

MLB - ALS SENSOR



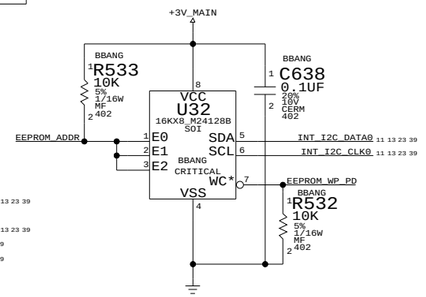
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U40	ALT FOR SUPPLY PROBLEM

LMU

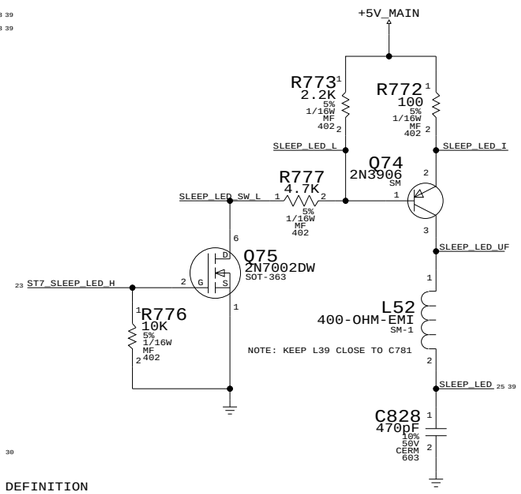


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

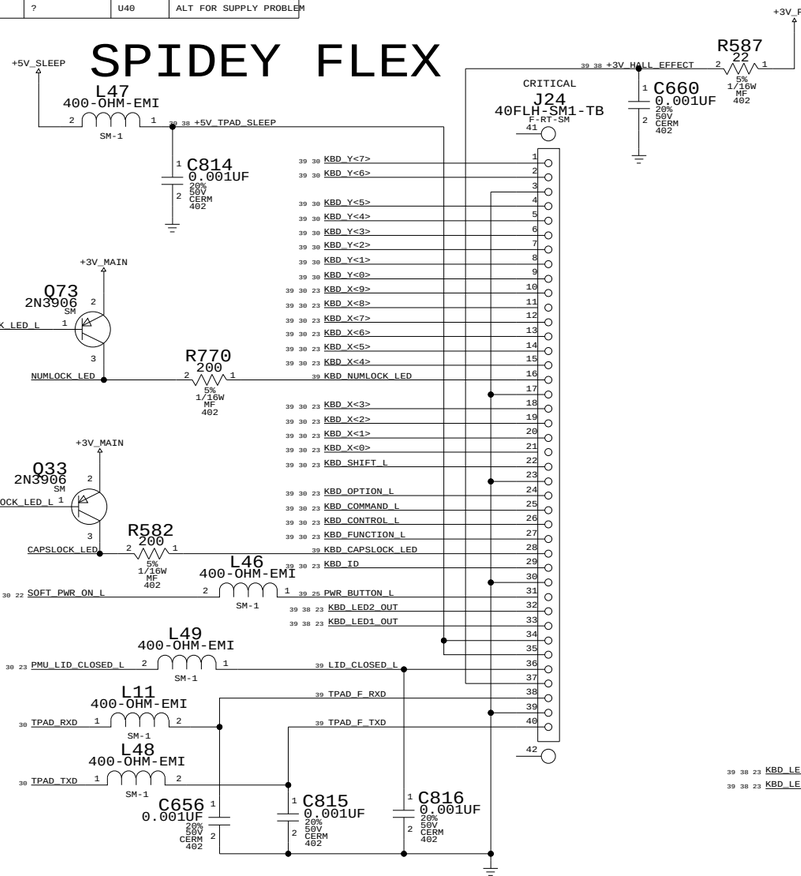
BOOT BANGER E2PROM



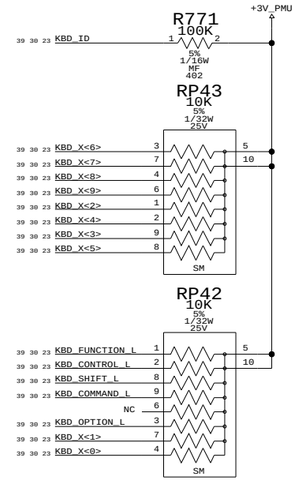
SLEEP LED



SPIDEY FLEX

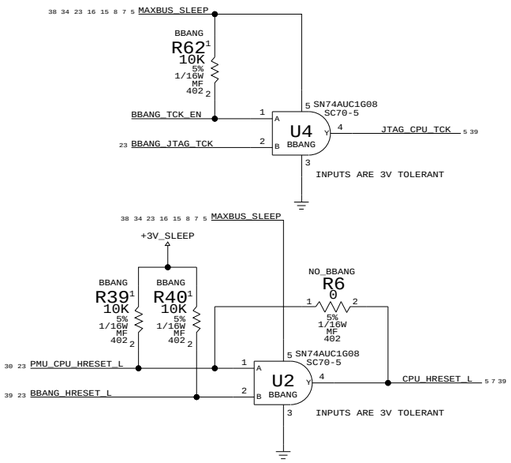


KEYBOARD PULLUPS

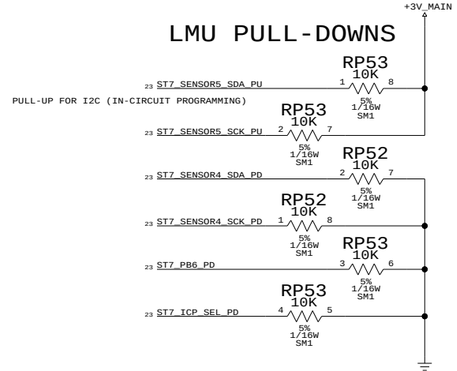


BOOT BANGING SIGNAL DEFINITION

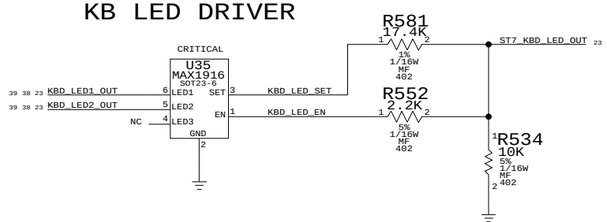
1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)



LMU PULL-DOWNS



KB LED DRIVER



LMU/BOOTBANGER/SPIDEY

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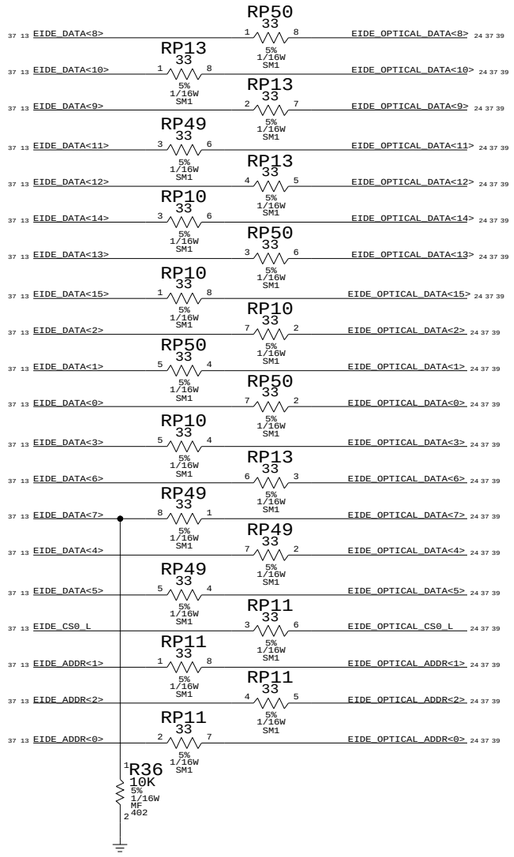
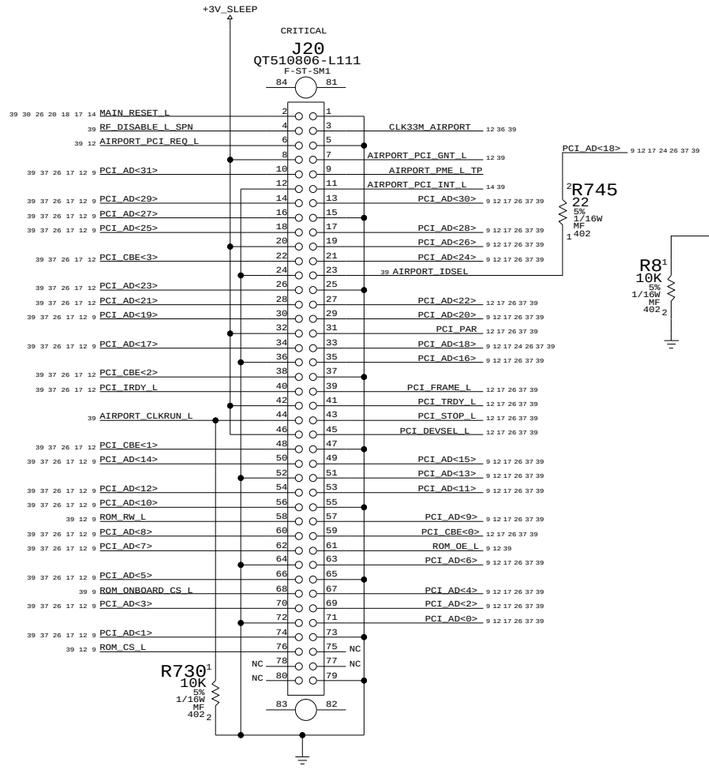
HARD DRIVE INTERFACE (UATA100)

EIDE SERIES TERMINATION

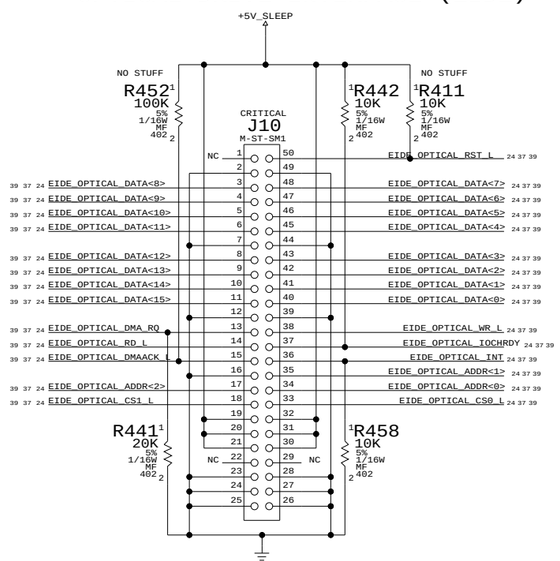
PLACE TERMINATORS NEAR INTREPID



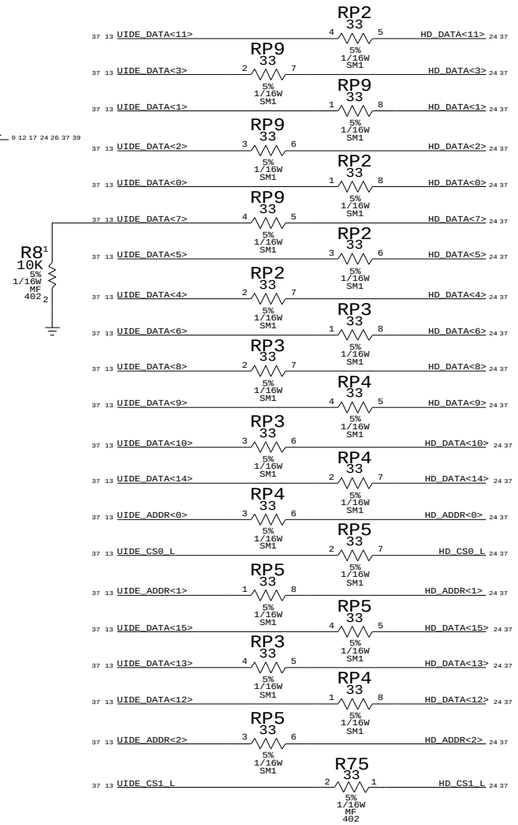
WIRELESS INTERFACE



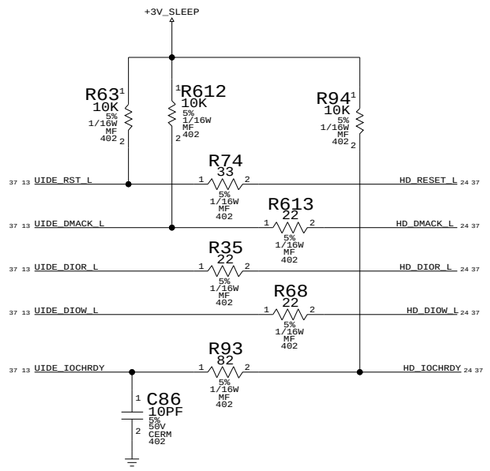
OPTICAL DRIVE INTERFACE (EIDE)



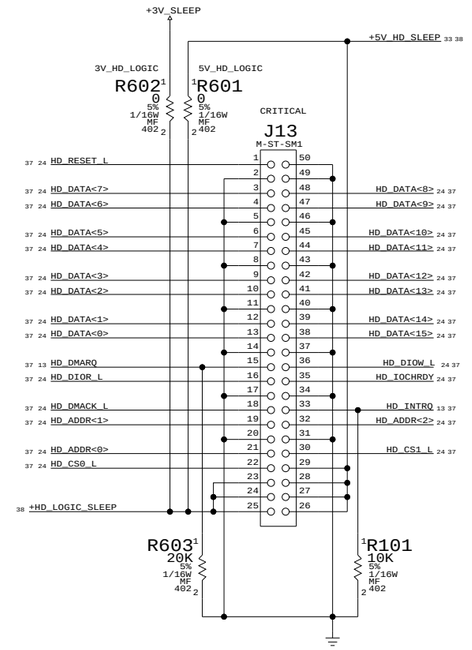
PLACE SERIES R CLOSE TO INTREPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

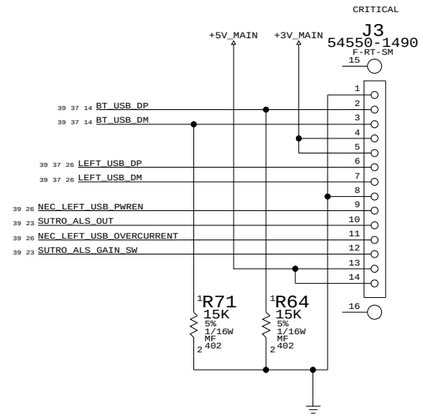


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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SOUND BOARD (SOUSAPHONE)

AUDIO - SNAPPER
SND - INTREPID

L77 FERR-220-OHM 0402 — SND_SYNC — SND_SYNC_F
L80 FERR-220-OHM 0402 — SND_CLKOUT — SND_CLKOUT_F
L81 FERR-220-OHM 0402 — INT_AUDIO_TO_SND — INT_AUDIO_TO_SND_F
L82 FERR-220-OHM 0402 — SND_TO_AUDIO — SND_TO_AUDIO_F
L76 FERR-220-OHM 0402 — SND_AMP_MUTE — SND_AMP_MUTE_F
L78 FERR-220-OHM 0402 — SND_HW_RESET_L — SND_HW_RESET_L_F
L79 FERR-220-OHM 0402 — SND_SCLK — SND_SCLK_F

C895 NO STUFF 0.01UF 20% 16V CERM 402
C899 NO STUFF 0.01UF 20% 16V CERM 402
C896 NO STUFF 0.01UF 20% 16V CERM 402
C897 NO STUFF 0.01UF 20% 16V CERM 402
C898 NO STUFF 0.01UF 20% 16V CERM 402
C900 NO STUFF 0.01UF 20% 16V CERM 402
C901 NO STUFF 0.01UF 20% 16V CERM 402

CRITICAL
J12 QT510306-L111 F-ST-SM1
INT_AUDIO_TO_SND_F, SND_TO_AUDIO_F, SND_HP_SENSE_L, INT_I2C_CLK2, SND_LIN_SENSE_L, SND_SCLK_F, SND_AMP_MUTE_F, SND_CLKOUT_F, SLEEP, SND_SYNC_F, INT_I2C_DATA2, SND_HW_RESET_L_F, SLEEP_LED, SND_HP_MUTE_INV

XW9 SM — SND_AGND

+3V_MAIN, +5V_MAIN

PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

MAIN1
C681 0.001UF 20% 50V CERM 402
Q66 2N3904 SM
SUPPLY_M_DP, SUPPLY_M_DM

PLACE CLOSE TO CPU
MAIN2
C668 0.001UF 20% 50V CERM 402
Q39 2N3904 SM
CPU_M_DP, CPU_M_DM

PLACE UNDERNEATH UPPER RAM
ALTERNATE1
C678 NO STUFF 0.001UF 20% 50V CERM 402
Q47 NO STUFF 2N3904 SM
THERM1_A_DP, THERM1_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2
C651 NO STUFF 0.001UF 20% 50V CERM 402
Q62 NO STUFF 2N3904 SM
THERM2_A_DP, THERM2_A_DM

CAPS FOR EMI EXPERIMENTATION ONLY

FAN INTERFACE

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R719 0 5% 1/16W MF 402 — CPU_M_DP — THERM1_DP
R725 0 5% 1/16W MF 402 — CPU_M_DM — THERM1_DM
R713 0 5% 1/16W MF 402 — SUPPLY_M_DP — THERM2_DP
R716 0 5% 1/16W MF 402 — SUPPLY_M_DM — THERM2_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R628 NO STUFF 0 5% 1/16W MF 402 — CPU_THERM_DP — THERM1_DP
R620 NO STUFF 0 5% 1/16W MF 402 — CPU_THERM_DM — THERM1_DM
R723 0 5% 1/16W MF 402 — THERM1_A_DP — THERM1_DP
R726 NO STUFF 0 5% 1/16W MF 402 — THERM1_A_DM — THERM1_DM
R710 0 5% 1/16W MF 402 — THERM2_A_DP — THERM2_DP
R717 NO STUFF 0 5% 1/16W MF 402 — THERM2_A_DM — THERM2_DM

+5V_MAIN
RP44 100K 5% 1/16W SM1 — SND_AMP_MUTE
026 2N7002DW SOT-363 — SND_AMP_MUTE_L
AMP_CONTROL
RP44 100K 5% 1/16W SM1
026 2N7002DW SOT-363 — INT_PU_RESET_L

+3V_MAIN
RP44 100K 5% 1/16W SM1
R689 100K 5% 1/16W MF 402
SND_HP_MUTE_INV
031 2N7002DW SOT-363 — SND_HP_MUTE
031 2N7002DW SOT-363 — SND_HP_MUTE_L
AMP_CONTROL
RP44 100K 5% 1/16W SM1

THERM ISOLATION

+3V_MAIN
R811 100K 5% 1/16W MF 402
+3V_PMU_AVCC
R812 100K 5% 1/16W MF 402
THERM_L_OC
R813 100K 5% 1/16W MF 402
THERM_INV
Q87 2N7002DW SOT-363
Q87 2N7002DW SOT-363
C903 0.1UF 20% 10V CERM 402
ADT7460_THERM

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

+5V_MAIN
C767 10UF 20% 6.3V CERM 805
NO STUFF C513 0.1UF 20% 10V CERM 402
R405 10K 5% 1/16W MF 402
+3V_MAIN
NO STUFF C478 0.1UF 20% 10V CERM 402
C469 10UF 20% 6.3V CERM 805

CRITICAL
J8 QT510166-L010 F-ST-SM1
MOD_DTO, MOD_CLKOUT, COMM_RESET_L, COMM_SHUTDOWN, INT_I2C_CLK2, INT_I2C_DATA2
MOD_SYNC, INT_MOD_DTI, MOD_BITCLK, MODEM_USB_DM, MODEM_USB_DP, COMM_RING_DET_L

FAN CONTROLLER

+3V_MAIN
R814 10 5% 1/16W MF 402
ADT7460_VCC
C904 1UF 20% 10V CERM 603
C711 0.1UF 20% 10V CERM 402
VCC
U3 ADT7460 QSOP
+2.5V/ SMBALERT# SDA SCL
PWM1/ XTO TACH1 PWM2/ SMBALERT# TACH2 PWM3/ ADR ENABLE# TACH3 TACH4/ ADR SELECT/ THERM#
GND
ADT7460_VCORE_MON, INT_I2C_DATA1, INT_I2C_CLK1
THERM1_DP, THERM1_DM, THERM2_DP, THERM2_DM
ADT7460_FAN1_PWM, FANL_TACH, ADT7460_FAN2_PWM, FANR_TACH, ADT7460_ADR_EN_L, NC, ADT7460_THERM
R42 10K 5% 1/16W MF 402
R692 10K 5% 1/16W MF 402
R695 10K 5% 1/16W MF 402
+5V_SLEEP
Q78 2N7002DW SOT-363
Q78 2N7002DW SOT-363
C688 NO STUFF 0.001UF 20% 50V CERM 402
C690 NO STUFF 0.001UF 20% 50V CERM 402
C846 NO STUFF 0.001UF 20% 50V CERM 402
C905 NO STUFF 0.001UF 20% 50V CERM 402

LEFT FAN (CPU)

+5V_SLEEP
R679 10K 5% 1/16W MF 402
CRITICAL
J4 SM-2MT
FANL_TACH, FANL_GND
Q37 SI3446DV TSOP
PLACE CLOSE TO CONNECTOR
C134 4.7UF 20% 10V CERM 1206
FANL_PWM

SERIAL DEBUG INTERFACE

+5V_MAIN
SERIAL_DEBUG CRITICAL
J16 M-ST-5087 SM
COMM_TXD_L, COMM_TRXC, COMM_GPIO_L
COMM_DTR_L, COMM_RTS_L, COMM_RXD

DEBUG POWER BUTTON

NO STUFF
R527 0 5% 1/16W MF 603
PWR_BUTTON_L

DEBUG JUMPERS

+5V_SLEEP
R293 10K 5% 1/16W MF 402
R295 10K 5% 1/16W MF 402
FANL_PWM, FANR_PWM

NO STUFF
R537 0 5% 1/16W MF 603
PMU_NMI_BUTTON_L

NO STUFF
R553 0 5% 1/16W MF 603
PMU_RESET_BUTTON_L

RIGHT FAN (GPU)

+5V_SLEEP
R623 10K 5% 1/16W MF 402
CRITICAL
J2 SM-2MT
Q36 SI3446DV TSOP
FANR_GND, FANR_TACH
PLACE CLOSE TO CONNECTOR
C135 4.7UF 20% 10V CERM 1206
FANR_PWM

FAN/MODEM/SOUND/SLEEP LED/DEBUG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 25 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to facilitate NAND-tree testing

Low/Full/High Speed (External)

Low/Full/High Speed (External)

Tie to GND at ball N11

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

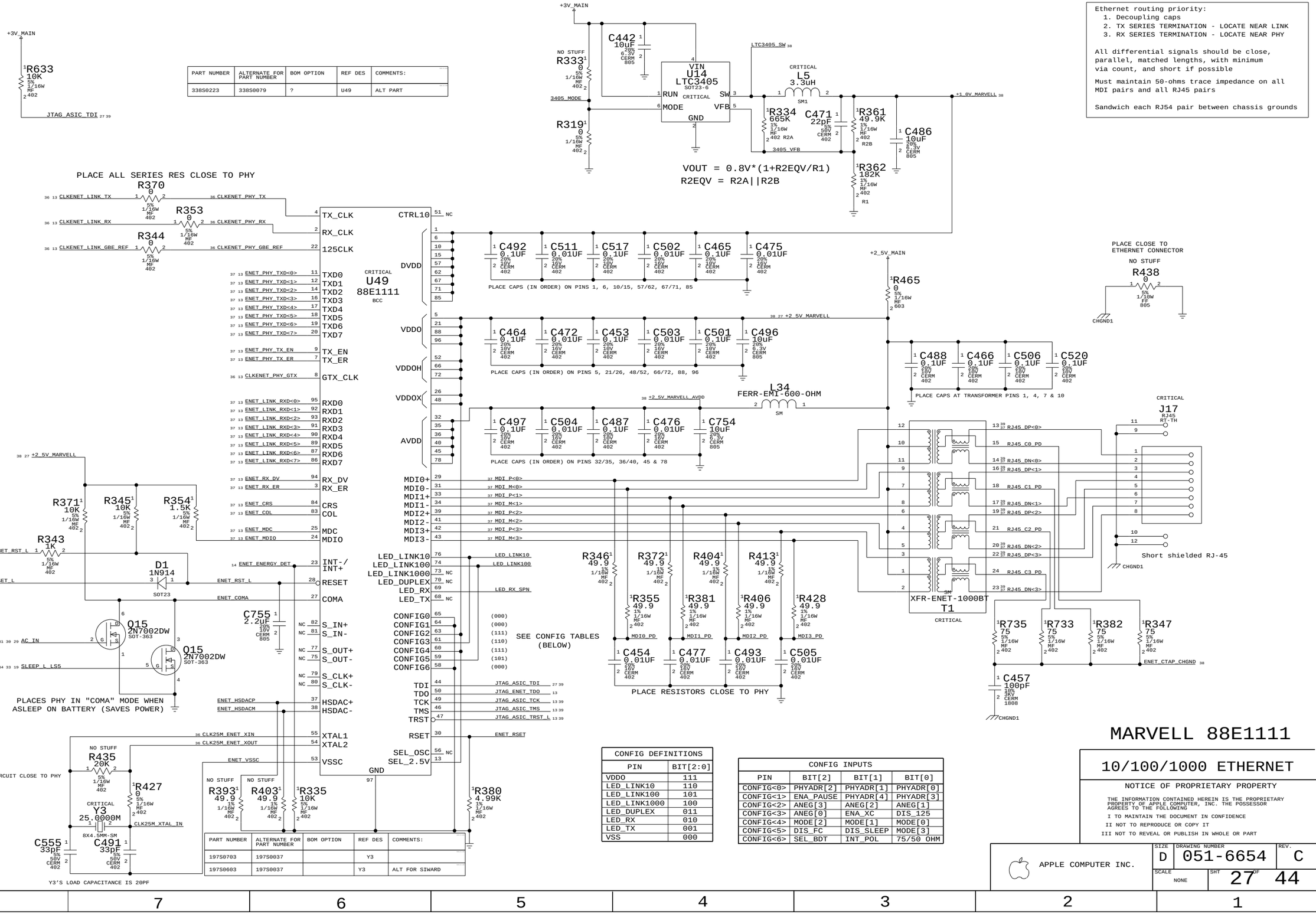
INTREPID USB CONSTRAINTS

USB_DAM	USB_DA	5 MIL SPACING	14
USB_DAP	USB_DA	5 MIL SPACING	14
USB_DCM	USB_DC	5 MIL SPACING	14
USB_DCP	USB_DC	5 MIL SPACING	14
USB_D1M	USB_D1	5 MIL SPACING	14 26
USB_D1P	USB_D1	5 MIL SPACING	14 26
USB_D2M	USB_D2	5 MIL SPACING	14 26
USB_D2P	USB_D2	5 MIL SPACING	14 26

USB 2.0

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 26 OF 44	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

0 -> BILINGUAL PORT

1 -> A-ONLY PORT

PLACE NEAR PHY

PLACE NEAR PHY

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

FIREWIRE

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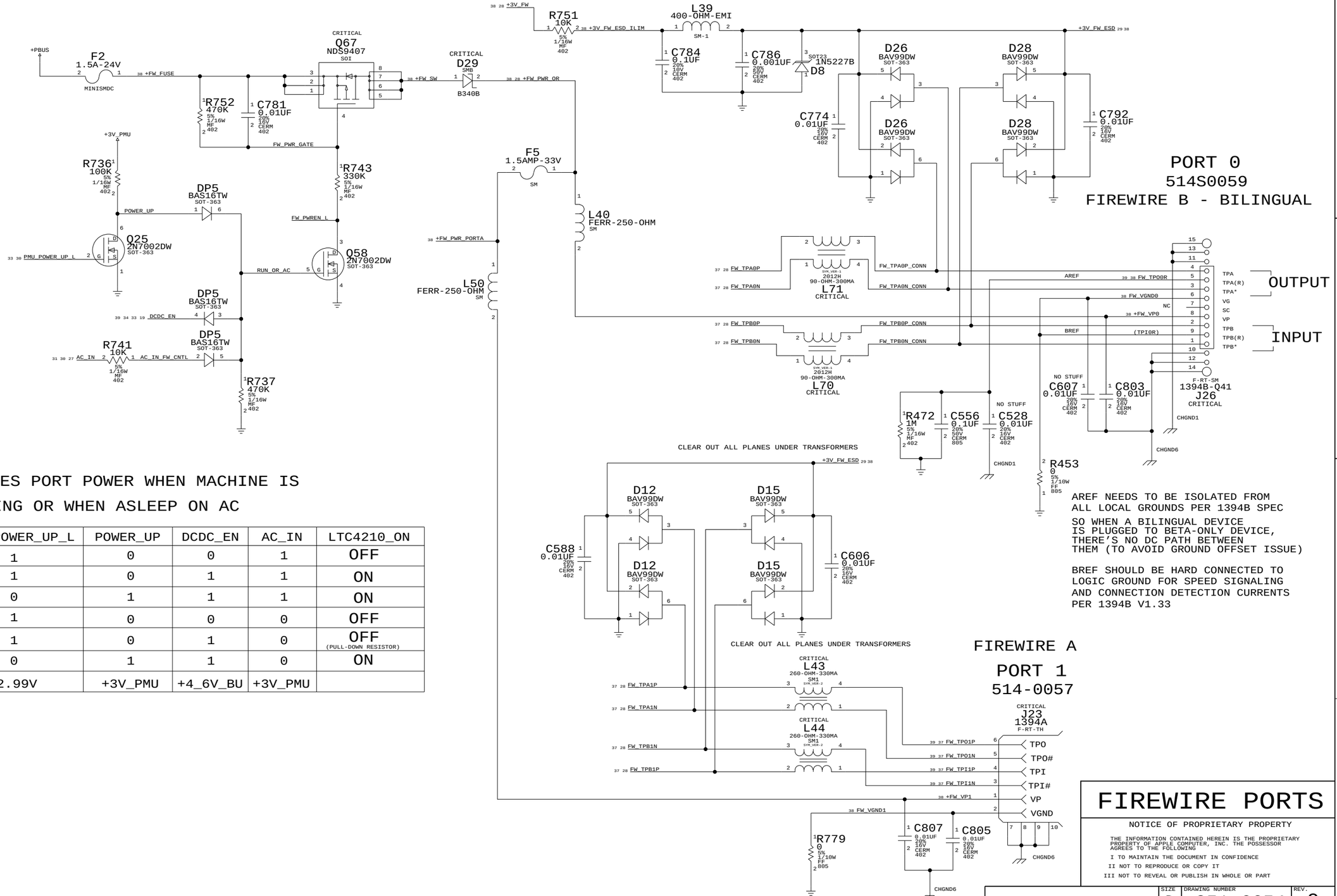
D	051-6654	C
SCALE: NONE	SHT 28 OF 44	

PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC

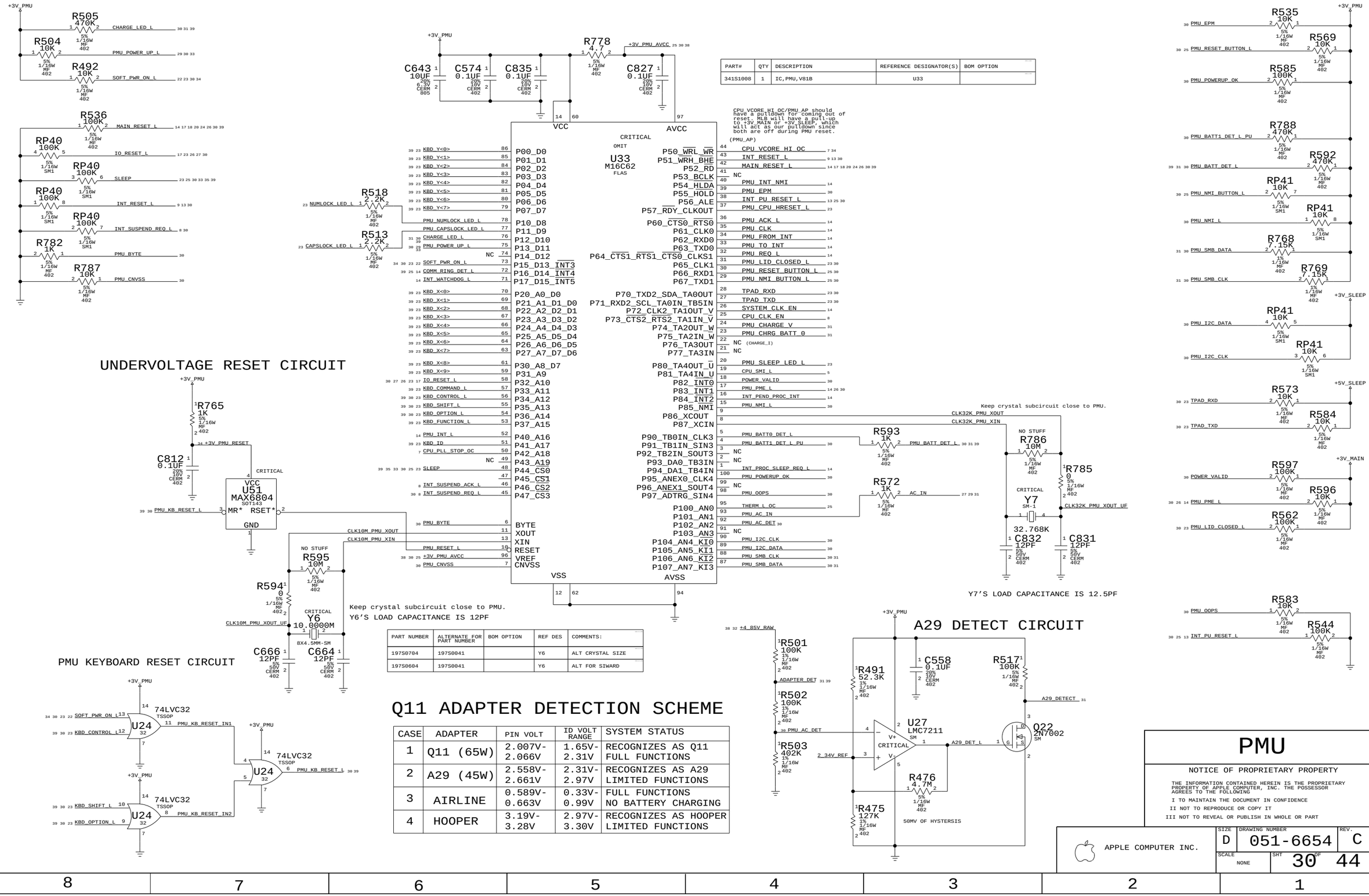
SO WHEN A BILINGUAL DEVICE IS PLUGGED TO BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

FIREWIRE PORTS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 29 OF 44	



DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

NO STUFF
C757 0.1UF 20% 50V CERM 805

PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402

DC INRUSH LIMITER

Q013 SI4435DY SOI
Q016 SI4435DY SOI

+ADAPTER_SW
+ADAPTER_SENSE

R414 330K 5% 1/16W MF 402
C458 0.1UF 20% 50V CERM 805
R474 47K 5% 1/16W MF 402
R374 470K 5% 1/16W MF 402
AC_ENABLE_GATE
AC_ENABLE_L

BCKFD_PROT_GATE
C592 0.1UF 20% 50V CERM 805
R499 68K 5% 1/16W MF 402
BCKFD_PROT_EN_L
Q021 2N7002DW SOT-363

C572 0.01UF 20% 50V CERM 603

PLACE U23 NEXT TO R460
U23 SENSE VOLTAGE DROP ACROSS R460

U23 MAX4172 TSSOP
RS+ RS- PG NC1 NC2 OUT GND
CRITICAL
MAX4172_OUT

+24V_PBUS
R454 2.21K 0.1% 1/10W MF 603
C883 0.1UF 10% 50V X7R 603-1

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
C771 0.1UF 20% 10V CERM 402
IAC_RC_COMP
+3V_PMU
C772 0.1UF 10% 16V CERM 402
R747 42.2K 0.1% 1/16W FF 603
IAC_FB
U50 LMC7111 SOT23-5
CRITICAL
DP4 BAS16TW SOT-363
LTC1625_ITH
R358 150 1% 1/16W MF 402
1_1625_COMP
ADAPTER_I_REG
R466 10K 1% 1/16W MF 402
CURRENT_THRESHOLD

PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

R738 42.2K 0.1% 1/10W FF 603
R734 82.5K 0.1% 1/10W FF 603
A29_CURRENT_ADJ
Q020 2N7002DW SOT-363
A29_DETECT
R739 51.1K 0.1% 1/16W FF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING
OVER_18V_ADJ
R748 100K 5% 1/16W MF 402
AC_GTR_18V
Q020 2N7002DW SOT-363
C775 1UF 20% 10V CERM 603
Q065 2N7002DW SOT-363
1772_ACOK_L

IF A29 ADAPTER USED, ADJUST CURRENT SETTING

R460 0.025 1% 1W MF 2512
R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN
C578 0.47UF 10% 16V CERM 1206
C579 0.47UF 10% 16V CERM 1206

R571 33 5% 1/8W FF 1206
D10 1N914 SOT23
1772_LDO
1772_BST_ESR
R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603
R774 4.7 5% 1/16W MF 603
C608 0.1UF 20% 50V CERM 805

BATTERY SWITCH-OVER CIRCUIT

+BATT
F4 5AMP-125V SM-2
F3 5AMP-125V SM-2
+24V_PBUS
+PBUS
+BATT_24V_FUSE
+BATT_14V_FUSE
CRITICAL
Q024 SI4435DY SOI
Q076 SUD45P03 TO-252
R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402
BATT_14V_GATE
BATT_24V_GATE
R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402
DP4 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN
Q021 2N7002DW SOT-363
AC_IN_L
R489 158K 1% 1/16W MF 402
DP4 BAS16TW SOT-363
AC_IN_L_RC
C593 10UF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

GREATER THAN 13.5V DETECT

R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
C468 0.01UF 20% 16V CERM 402
R363 10K 5% 1/16W MF 402
1V20_REF
U15 LMC7211 SM
CRITICAL
AC_IN
AC_DIV
R394 1M 5% 1/16W MF 402
AC_IN_L
Q010 2N7002DW SOT-363
R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402
R383 470K 5% 1/16W MF 402

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
R755 12.7K 1% 1/16W MF 402
C600 1UF 20% 50V CERM1 1210

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

+3V_PMU
R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402
R560 4.12K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402
R566 1K 1% 1/16W MF 402
R542 1K 1% 1/16W MF 402

U31 MAX1772 QSOP
CRITICAL
CSSP CSSN DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS REF CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT GND

1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
REF = 4.096V
1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN

R561 100K 5% 1/16W MF 402
BATTV_HIGH
BATTV_LOW
Q027 2N7002DW SOT-363
R580 5.23K 1% 1/16W MF 402
PMU_CHARGE_V
Q029 2N7002DW SOT-363
BATT_LOW_L
R526 1K 1% 1/16W MF 402
C622 0.01UF 20% 16V CERM 402
C616 0.01UF 20% 16V CERM 402
1772_CCV_RC
R497 1K 1% 1/16W MF 402
C621 0.1UF 20% 16V CERM 402
1772_REF
C630 1UF 20% 10V CERM 603
R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402
1772_CLS
R559 100K 5% 1/16W MF 402
C652 1UF 20% 10V CERM 603
C817 0.1UF 20% 25V CERM 603
C802 0.1UF 20% 25V CERM 603
NO STUFF
C906 0.0022UF 10% 50V CERM 402
XW19
1772_GND

Q030 2N7002DW SOT-363
R578 100K 5% 1/16W MF 402
CHARGE_DISABLE
PMU_CHRG_BATT_0

C615 0.1UF 20% 10V CERM 402
U38 LMC7211 SM
CRITICAL
BATT_LOW
R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
BATT_DIV
1V65_REF
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047UF 10% 16V CERM 402

R749 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
Q065 2N7002DW SOT-363
A29_DETECT

+BATT_VSNS

BATTERY CONNECTOR

CRITICAL
J25
87438-0833
M-RT-SM

+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
PMU_SMB_CLK
L8 FERR-EMI-100-OHM SM
PMU_SMB_DATA
L12 FERR-50-OHM SM

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

Q063 IRF7805 SM
Q064 IRF7811W SO-8
CRITICAL
C547 2.2UF 10% 16V CERM 1812
C562 2.2UF 10% 16V CERM 1812
C563 2.2UF 10% 16V CERM 1812
C557 2.2UF 10% 16V CERM 1812
C564 2.2UF 10% 16V CERM 1812
L42 10uH SM1
D30 MBRS140T3
R763 0.05 1% 1W MF 2512
+BATT_RSNS
R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603
C619 4.7UF 20% 25V CERM 1206
C631 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SM1

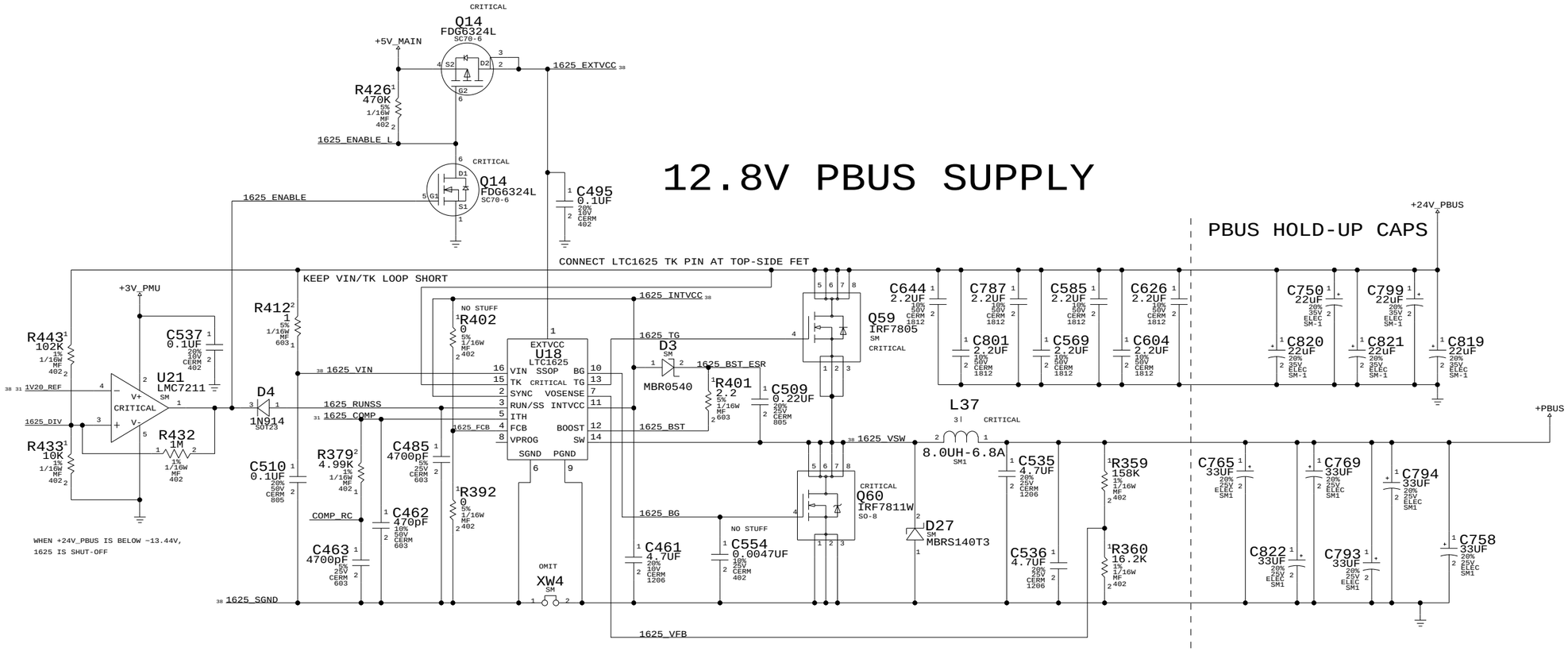
BATTERY CHARGER

APPLE COMPUTER INC.

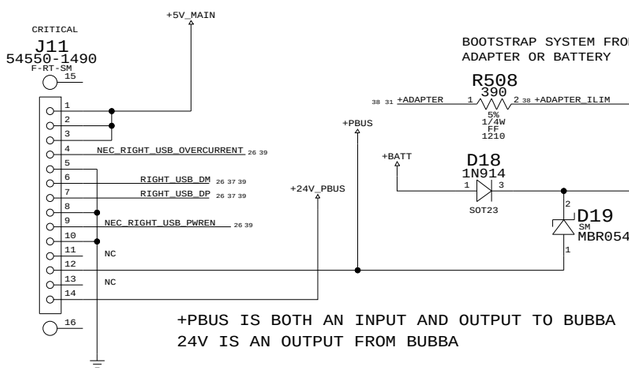
SIZE D | DRAWING NUMBER 051-6654 | REV. C

SCALE NONE | SHT 31 OF 44

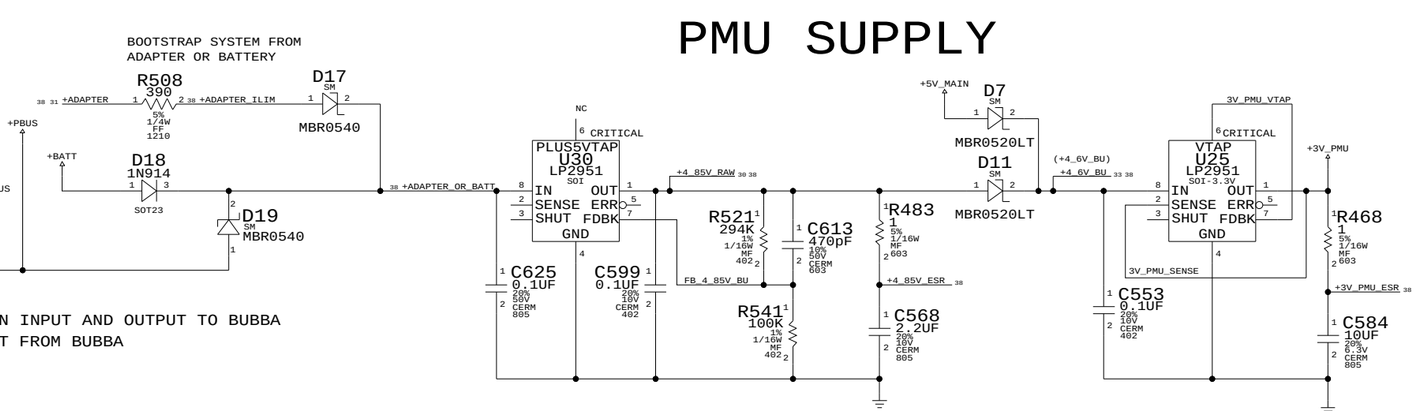
12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR



PMU SUPPLY



12.8V REGULATOR

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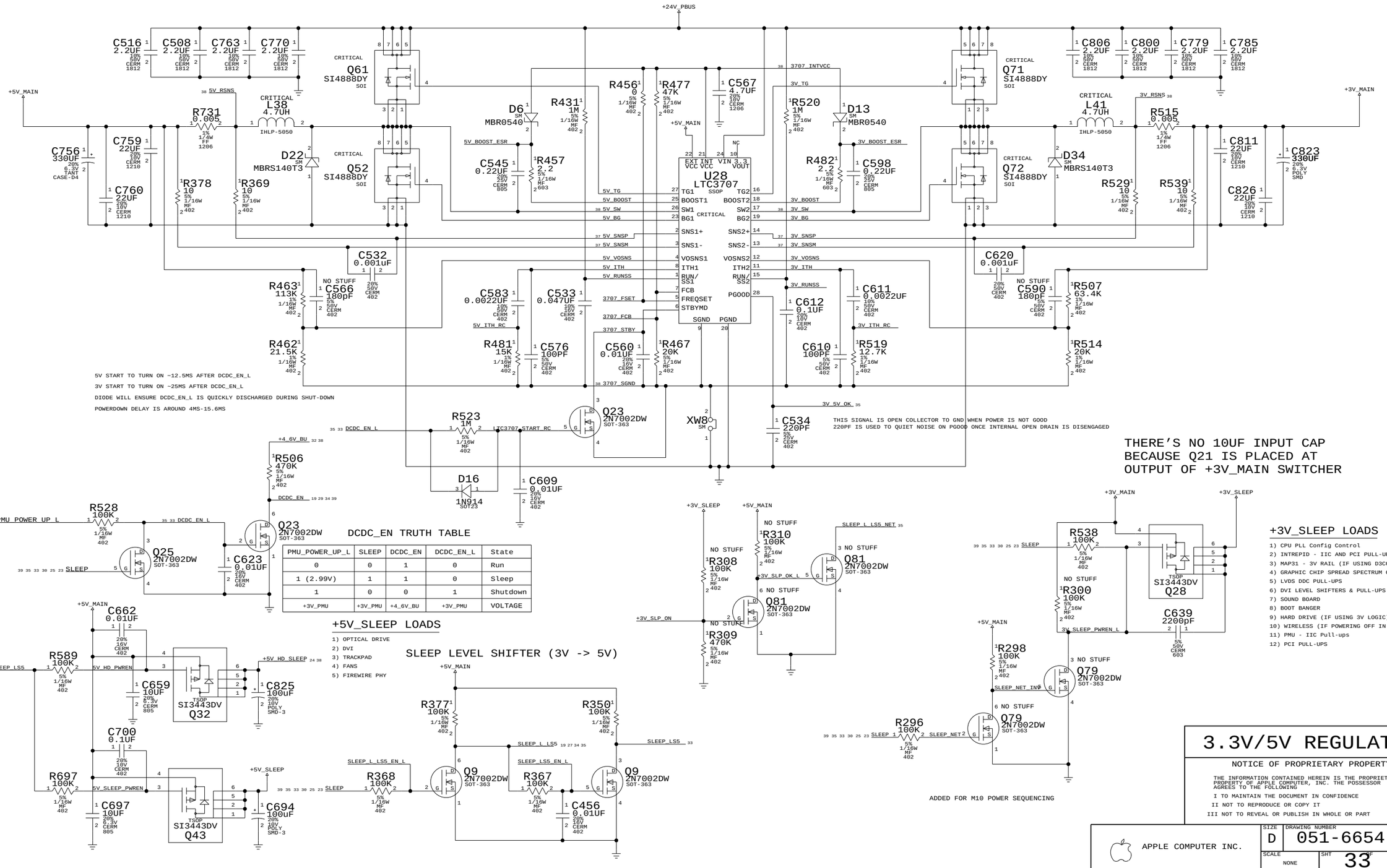
D	051-6654	C

SCALE: NONE

SHT 32 OF 44

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 33 OF 44	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 0.975V

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

Connect MAX1717 GND pin 13 to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0022	128S0034	?	C728,C729,C730,C731,C732,C733,C734,C884,C885	

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

FMAX CONNECTOR

CRITICAL
NO STUFF
J5
M-ST-SM-52465-1217

VCORE SUPPLY

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SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 34 OF 44	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

THERE'S 100K PULL-UP ON PG 31 ALREADY

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN
POWER DOWN DELAY 1.5MS TO 3.5MS

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

CONTINUOUS MODE

BURST MODE
NO STUFF

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C

SCALE: NONE | SHT 35 OF 44

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10 MIL SPACING			5 8
	CPU_ADDR<0..31>		5		250			83 MHZ	5 8
	CPU_ARTRY_L				250.0000	10 MIL SPACING			5 8
	CPU_BG_L				250.0000	10 MIL SPACING			5 8
	CPU_BR_L				250.0000	10 MIL SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83 MHZ	6 8
	CPU_DATA<32..63>		5		250			83 MHZ	6 8
	CPU_DBG_L		5		250.0000	10 MIL SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10 MIL SPACING			
	CPU_DRDY_L				250.0000	10 MIL SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10 MIL SPACING			5 8
	CPU_QACK_L		5		250.0000	10 MIL SPACING			5 8
	CPU_QREQ_L				250.0000	10 MIL SPACING			5 8
	CPU_TA_L				250.0000	10 MIL SPACING			5 8
	CPU_TBST_L		5		250.0000	10 MIL SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10 MIL SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0..4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167 MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167 MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167 MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167 MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167 MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167 MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167 MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167 MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167 MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQS_B<3..2>		4		200			167 MHZ	10 11
	MEM_DQM<3..2>		4		200			167 MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167 MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167 MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167 MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167 MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167 MHZ	10 11
	MEM_DQM<5..4>		4		200			167 MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167 MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167 MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167 MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167 MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167 MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167 MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167 MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83 MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
CONTROL	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10 MIL SPACING		8
	SYSCLK_CPU			4		200.0000	10 MIL SPACING		5 8
	INT_CPUFB_OUT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_SHORT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_NORM			3			10 MIL SPACING		8
	INT_CPUFB_IN_NORM			3			10 MIL SPACING		8
	INT_CPUFB_LONG			3			10 MIL SPACING		8
	INT_CPUFB_IN					200.0000	10 MIL SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10 MIL SPACING		14
	INT_REF_CLK_IN					200.0000	10 MIL SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10 MIL SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10 MIL SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10 MIL SPACING		12
	INT_AGP_FB_IN			4		200.0000	10 MIL SPACING		12
	CLK33M_CBUS_UF					200.0000	10 MIL SPACING		12
	CLK33M_CBUS		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10 MIL SPACING		12
	CLK33M_AIRPORT		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 24 39
	CLK33M_USB2_UF					200.0000	10 MIL SPACING		12
	CLK33M_USB2		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 26
	INT_PCI_FB_OUT					200.0000	10 MIL SPACING		12
	INT_PCI_FB_IN			3		200.0000	10 MIL SPACING		12
MAP31	GPU_CLK27M_OUT						10 MIL SPACING		
	GPU_CLK27M_UF						10 MIL SPACING		
	GPU_SSCLK_UF						10 MIL SPACING		
	GPU_SSCLK_IN						10 MIL SPACING		
	GPU_FBCLK0						10 MIL SPACING		
	GPU_FBCLK0_L						10 MIL SPACING		
	GPU_FBCLK1						10 MIL SPACING		
	GPU_FBCLK1_L						10 MIL SPACING		
	GPU_DVO_CLKP						10 MIL SPACING		19 20
CRYSTALS	CLK27M_GPU_XOUT						10 MIL SPACING		
	CLK27M_XTAL_IN						10 MIL SPACING		
	CLK27M_GPU_XIN						10 MIL SPACING		
	CLK18M_INT_XIN						10 MIL SPACING		14
	CLK18M_INT_XOUT						10 MIL SPACING		14
	CLK18M_XTAL_IN						10 MIL SPACING		14
	CLK18M_INT_EXT						10 MIL SPACING		14
	CLK25M_ENET_XIN						10 MIL SPACING		27
	CLK25M_ENET_XOUT						10 MIL SPACING		27
	NEC_XT1						10 MIL SPACING		26
	NEC_XT2		THERE'S ANOTHER 280MIL LEG				10 MIL SPACING		26
SOUND	SND_SCLK			7		200.0000	10 MIL SPACING		14 25 39
	SND_CLKOUT					200.0000	10 MIL SPACING		14 25 39
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			27
	CLKENET_LINK_RX			3		200.0000	10 MIL SPACING		13 27
	CLKENET_PHY_GBE_REF					200.0000			27
	CLKENET_LINK_GBE_REF			3		200.0000	10 MIL SPACING		13 27
	CLKENET_PHY_TX					200.0000			27
	CLKENET_LINK_TX			5		200.0000	10 MIL SPACING		13 27
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10 MIL SPACING		13 27
FIREWIRE	CLKFW_PHY_PCLK					200.0000			28
	CLKFW_LINK_PCLK			3		200.0000	10 MIL SPACING		13 28
	CLKFW_PHY_LCLK			3		200.0000	10 MIL SPACING		13 28
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10 MIL SPACING		28
	FW_OSC					200.0000	10 MIL SPACING		28

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C

SCALE: NONE

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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHZ	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHZ	12 18
	AGP_AD_STB<0>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		5	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHZ	12 18
	AGP_CBE<3..2>		5	100				66 MHZ	12 18
	AGP_AD_STB<1>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHZ	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		5	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..11>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHZ	9 12 17 24 26 39
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHZ	12 17 24 26 39
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_PAR					MIN_DAISY_CHAIN			12 17 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>				200			100 MHZ	13 24
	UIDE_DATA<7>				208				13 24
	UIDE_DATA<6..0>				200			100 MHZ	13 24
	UIDE_ADDR<2..0>				200			100 MHZ	13 24
	UIDE_RST_L				200.0000				13 24
	UIDE_DIOW_L				200.0000				13 24
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 24
	UIDE_DMACK_L				200.0000				13 24
	UIDE_CS0_L				200.0000				13 24
	UIDE_CS1_L				200.0000				13 24
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 24
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5		200			100 MHZ	24
	HD_ADDR<2..0>		5		208			100 MHZ	24
	HD_RESET_L		5		200.0000				24
	HD_DIOW_L		5		200.0000				24
	HD_DIOR_L		5	10 MIL SPACING	200.0000				24
	HD_DMACK_L		5		200.0000				24
	HD_CS0_L		5		200.0000				24
	HD_CS1_L		5		200.0000				24
	HD_DMARQ				200.0000				13 24
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				24
	HD_INTRQ		5						13 24
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 24
	EIDE_ADDR<2..0>							33 MHZ	13 24
	EIDE_CS0_L								13 24
	EIDE_CS1_L								13 24
	EIDE_RD_L								13 24
	EIDE_WR_L								13 24
	EIDE_IOCHRDY								13 24
	EIDE_INT								13 24
	EIDE_RST_L								13 24
	EIDE_DMACK_L								13 24
	EIDE_DMARQ								13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	24 39
	EIDE_OPTICAL_CS0_L								24 39
	EIDE_OPTICAL_CS1_L								24 39
	EIDE_OPTICAL_RD_L								24 39
	EIDE_OPTICAL_WR_L								24 39
	EIDE_OPTICAL_IOCHRDY								24 39
	EIDE_OPTICAL_INT								24 39
	EIDE_OPTICAL_RST_L								24 39
	EIDE_OPTICAL_DMAACK_L								24 39
	EIDE_OPTICAL_DMA_RQ								24 39
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 27
	ENET_RX_DV								13 27
	ENET_RX_ER								13 27
	ENET_PHY_TXD<7..0>		5						13 27
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 27
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 27
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 27
	ENET_MDC								13 27
	ENET_COL								13 27
	ENET_CRS								13 27
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 28
	FW_PHY_DATA<7..0>		5						28
	FW_LINK_CNTL<1..0>								13 28
	FW_PHY_CNTL<1..0>								28
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 28
	FW_PINT								13 28

NEED TO MATCH DELAY TO 250

TOTAL UIDE+HD SKEW <500MIL

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR		MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0					27
	MDI_P<0>	ENET_MDI0					27
	MDI_M<1>	ENET_MDI1		SPACING DELETED BECAUSE			27
	MDI_P<1>	ENET_MDI1		OF PHYSICAL CONSTRAINTS			27
	MDI_M<2>	ENET_MDI2		AROUND MARVELL PHY			27
	MDI_P<2>	ENET_MDI2					27
	MDI_M<3>	ENET_MDI3					27
	MDI_P<3>	ENET_MDI3					27
	RJ45_DN<0>	RJ45_DP0			10 MIL SPACING		27 39
	RJ45_DP<0>	RJ45_DP0			10 MIL SPACING		27 39
	RJ45_DN<1>	RJ45_DP1			10 MIL SPACING		27 39
	RJ45_DP<1>	RJ45_DP1			10 MIL SPACING		27 39
	RJ45_DN<2>	RJ45_DP2			10 MIL SPACING		27 39
	RJ45_DP<2>	RJ45_DP2			10 MIL SPACING		27 39
	RJ45_DN<3>	RJ45_DP3			10 MIL SPACING		27 39
	RJ45_DP<3>	RJ45_DP3			10 MIL SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA0P	FW_TPA0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0N	FW_TPB0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0P	FW_TPB0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI0N	FW_TPI0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA1P	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1N	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1P	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI1N	FW_TPI1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPI1P	FW_TPI1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1N	FW_TPO1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1P	FW_TPO1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L			10 MIL SPACING	4	19 22 39
	CLKLVDS_LP	CLKLVDS_L			10 MIL SPACING	4	19 22 39
	LVDS_L0N	LVDS_L0			10 MIL SPACING		19 22 39
	LVDS_L0P	LVDS_L0			10 MIL SPACING		19 22 39
	LVDS_L1N	LVDS_L1			10 MIL SPACING		19 22 39
	LVDS_L1P	LVDS_L1			10 MIL SPACING		19 22 39
	LVDS_L2N	LVDS_L2			10 MIL SPACING		19 22 39
	LVDS_L2P	LVDS_L2			10 MIL SPACING		19 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U			10 MIL SPACING	4	19 22 39
	CLKLVDS_UP	CLKLVDS_U			10 MIL SPACING	4	19 22 39
	LVDS_U0N	LVDS_U0			10 MIL SPACING		19 22 39
	LVDS_U0P	LVDS_U0			10 MIL SPACING		19 22 39
	LVDS_U1N	LVDS_U1			10 MIL SPACING		19 22 39
	LVDS_U1P	LVDS_U1			10 MIL SPACING		19 22 39
	LVDS_U2N	LVDS_U2			10 MIL SPACING		19 22 39
	LVDS_U2P	LVDS_U2			10 MIL SPACING		19 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS			10 MIL SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS			10 MIL SPACING	4	22 39
	TMDS_CLKN	CLKTMDS			10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS			10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0			10 MIL SPACING		20 22 39
	TMDS_DP<0>	TMDS_D0			10 MIL SPACING		20 22 39
	TMDS_DN<1>	TMDS_D1			10 MIL SPACING		20 22 39
	TMDS_DP<1>	TMDS_D1			10 MIL SPACING		20 22 39
	TMDS_DN<2>	TMDS_D2			10 MIL SPACING		20 22 39
	TMDS_DP<2>	TMDS_D2			10 MIL SPACING		20 22 39
USB	NEC_USB_DAM	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DAP	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DEM	USB_DE			5 MIL SPACING		14
	USB_DEP	USB_DE			5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DBP	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DFM	USB_DF			5 MIL SPACING		14
	USB_DFP	USB_DF			5 MIL SPACING		14
	BT_USB_DM	BT_USB_D			5 MIL SPACING		14 24 39
	BT_USB_DP	BT_USB_D			5 MIL SPACING		14 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	MODEM_USB_DM	MODEM_USB_D			5 MIL SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D			5 MIL SPACING		14 25 39
	LEFT_USB_DM	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
POWER SUPPLIES	1772_CSSN	1772_CSS			DIFF		31
	1772_CSSP	1772_CSS			DIFF		31
	1772_CSIN	1772_CSI			DIFF		31
	1772_CSIP	1772_CSI			DIFF		31
	3V_SNSM	3V_SNS			DIFF		33
	3V_SNSP	3V_SNS			DIFF		33
	5V_SNSM	5V_SNS			DIFF		33
	5V_SNSP	5V_SNS			DIFF		33
THERMOSTAT	THERM1_DM	THERM1			DIFF		25
	THERM1_DP	THERM1			DIFF		25
	THERM2_DM	THERM2			DIFF		25
	THERM2_DP	THERM2			DIFF		25
	THERM1_M_DM	THERM1_MAIN			DIFF		
	THERM1_M_DP	THERM1_MAIN			DIFF		
	THERM2_M_DM	THERM2_MAIN			DIFF		
	THERM2_M_DP	THERM2_MAIN			DIFF		
	THERM1_A_DM	THERM1_ALT			DIFF		25
	THERM1_A_DP	THERM1_ALT			DIFF		25
	THERM2_A_DM	THERM2_ALT			DIFF		25
	THERM2_A_DP	THERM2_ALT			DIFF		25

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.8OHM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 37 OF 44	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	25 30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
I/O AREA	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4 39
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	27

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 8 15 16 23 34
INTREPID PLLS	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	11
	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 39
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1534	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1535	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
1536	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1537	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1538	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1539	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1540	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1541	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1542	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1543	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1544	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1545	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
1546	+2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1547	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1548	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1549	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1550	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1551	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1552	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1553	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1554	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1555	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	+3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
1556	+3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
1557	+3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
FW	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
USB 2.0	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
INTREPID SSCG	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

MIN_NECK_WIDTH REDUCED FOR TESTPOINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	2_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_TON		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_SKIP		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_REF		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_CC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34 39
	VCORE_TIME		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_VGATE		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	14 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=15	34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	1778_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19 39
	1778_FCB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_VRNG		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SYNC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SHDN		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

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FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 27
FUNC_TEST=YES JTAG_ASIC_TDI 27
FUNC_TEST=YES JTAG_ASIC_TDO 13 14
FUNC_TEST=YES JTAG_ASIC_TCK 13 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39

FUNC_TEST=YES INT_I2C_CLK0 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 25
FUNC_TEST=YES INT_I2C_DATA1 13 14 25
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 37
FUNC_TEST=YES TMDS_DP<0> 20 22 37
FUNC_TEST=YES TMDS_DN<1> 20 22 37
FUNC_TEST=YES TMDS_DP<1> 20 22 37
FUNC_TEST=YES TMDS_DN<2> 20 22 37
FUNC_TEST=YES TMDS_DP<2> 20 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 37
FUNC_TEST=YES LVDS_L0P 19 22 37
FUNC_TEST=YES LVDS_L1N 19 22 37
FUNC_TEST=YES LVDS_L1P 19 22 37
FUNC_TEST=YES LVDS_L2N 19 22 37
FUNC_TEST=YES LVDS_L2P 19 22 37
FUNC_TEST=YES CLKLVDS_LN 19 22 37
FUNC_TEST=YES CLKLVDS_LP 19 22 37
FUNC_TEST=YES LVDS_U0N 19 22 37
FUNC_TEST=YES LVDS_U0P 19 22 37
FUNC_TEST=YES LVDS_U1N 19 22 37
FUNC_TEST=YES LVDS_U1P 19 22 37
FUNC_TEST=YES LVDS_U2N 19 22 37
FUNC_TEST=YES LVDS_U2P 19 22 37
FUNC_TEST=YES CLKLVDS_UN 19 22 37
FUNC_TEST=YES CLKLVDS_UP 19 22 37
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 25
FUNC_TEST=YES SND_SYNC 14 25
FUNC_TEST=YES SND_CLKOUT 14 25 36

FUNC_TEST=YES INT_AUDIO_TO_SND 14 25
FUNC_TEST=YES SND_SCLK 14 25 36
FUNC_TEST=YES SND_HW_RESET_L 14 25
FUNC_TEST=YES SND_HP_SENSE_L 14 25
FUNC_TEST=YES SND_LIN_SENSE_L 14 25
FUNC_TEST=YES INT_I2C_DATA2 14 25
FUNC_TEST=YES INT_I2C_CLK2 14 25
T290 FUNC_TEST=YES CHGND4 38
T291 FUNC_TEST=YES SLEEP_LED 23 25

FUNC_TEST=YES BT_USB_DM 14 24 37
FUNC_TEST=YES BT_USB_DP 14 24 37
FUNC_TEST=YES MODEM_USB_DM 14 25 37
FUNC_TEST=YES MODEM_USB_DP 14 25 37
FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37

FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<10> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<12> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<13> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<14> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<15> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<16> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<17> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<18> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<19> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<21> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<22> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<24> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<25> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37
FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37
FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37
FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37

FUNC_TEST=YES PCI_PAR 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37
T293 FUNC_TEST=YES SND_AMP_MUTE 25
T292 FUNC_TEST=YES SND_HP_MUTE_INV 25

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 25
FUNC_TEST=YES COMM_SHUTDOWN 14 25
FUNC_TEST=YES COMM_RING_DET_L 14 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=YES KBD_X<0> 23 30
FUNC_TEST=YES KBD_X<1> 23 30
FUNC_TEST=YES KBD_X<2> 23 30
FUNC_TEST=YES KBD_X<3> 23 30
FUNC_TEST=YES KBD_X<4> 23 30
FUNC_TEST=YES KBD_X<5> 23 30
FUNC_TEST=YES KBD_X<6> 23 30
FUNC_TEST=YES KBD_X<7> 23 30
FUNC_TEST=YES KBD_X<8> 23 30
T289 FUNC_TEST=YES SRCLK_TP 26
T288 FUNC_TEST=YES SRMOD_TP 26
T287 FUNC_TEST=YES TEB_TP 26
T286 FUNC_TEST=YES TEST_TP 26

FUNC_TEST=YES KBD_X<9> 23 30
FUNC_TEST=YES KBD_Y<0> 23 30
FUNC_TEST=YES KBD_Y<1> 23 30
FUNC_TEST=YES KBD_Y<2> 23 30
FUNC_TEST=YES KBD_Y<3> 23 30
FUNC_TEST=YES KBD_Y<4> 23 30
FUNC_TEST=YES KBD_Y<5> 23 30
FUNC_TEST=YES KBD_Y<6> 23 30
FUNC_TEST=YES KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FANR_GND 25 38
FUNC_TEST=YES FANL_GND 25 38
FUNC_TEST=YES FANL_TACH 25
T271 FUNC_TEST=YES FANR_PWM 25
T272 FUNC_TEST=YES FANL_PWM 25
FUNC_TEST=YES RJ45_DP<0> 27 37
FUNC_TEST=YES RJ45_DN<0> 27 37
FUNC_TEST=YES RJ45_DP<1> 27 37
FUNC_TEST=YES RJ45_DN<1> 27 37
FUNC_TEST=YES RJ45_DP<2> 27 37
FUNC_TEST=YES RJ45_DN<2> 27 37
FUNC_TEST=YES RJ45_DP<3> 27 37
FUNC_TEST=YES RJ45_DN<3> 27 37
FUNC_TEST=YES FW_TPO0R 29 38
T281 FUNC_TEST=YES VCORE_VID0
T282 FUNC_TEST=YES VCORE_VID1
T283 FUNC_TEST=YES VCORE_VID2
T285 FUNC_TEST=YES VCORE_VID3
T284 FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 29 37
FUNC_TEST=YES FW_TPO1N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 14 25
FUNC_TEST=YES COMM_TRXC 14 25
FUNC_TEST=YES COMM_GPIO_L 14 25
FUNC_TEST=YES COMM_DTR_L 14 25
FUNC_TEST=YES COMM_RTS_L 14 25
FUNC_TEST=YES COMM_RXD 14 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=YES +PBUS 38
FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=YES +1_8V_MAIN 38
FUNC_TEST=YES +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38
T280 FUNC_TEST=YES VCORE_MUX_EN 34

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 19 29 33 34
FUNC_TEST=YES BBANG_HRESET_L 23

FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 9 12 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 9 12 24
T273 FUNC_TEST=YES INT_MOD_DTI 14 25
T274 FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39
T275 FUNC_TEST=YES MOD_BITCLK 14 25
T276 FUNC_TEST=YES MOD_CLKOUT 14 25
T277 FUNC_TEST=YES MOD_DTO 14 25
T278 FUNC_TEST=YES MOD_SYNC 14 25
T279 FUNC_TEST=YES SLEEP 23 25 30 33 35
T280 FUNC_TEST=YES 1778_VFB 19 38

APPLE COMPUTER INC.

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REVISION HISTORY

12/11/03

1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
2) CHANGED CPU (U43) TO A7PW
3) CHANGED PLL CONFIG STUFFING FOR NEW CPU
4) CHANGED U41 TO M1T-CSP64 SYMBOL
5) ADDED CPU AVDD LDO (D5)
6) ADDED R284 AND R604 TO ADD OPTION FOR PD_L OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
7) ADDED R698 TO DISCONNECT INT_GPIO9 FROM CC FSET
8) CHANGED JTAG_ASIC_TDO TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
11) CHANGED PIN 11 OF J11 TO NC

12/16/03

12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
13) CHANGED CPU_TEMP_DN TO CPU_THERM_DM
14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
16) CHANGED GPU_THERM_DN TO GPU_THERM_DM_TP
17) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

18) CHANGED R657 (EXTPLL_SDWN_POL_BOOT_STRAP) TO NO_STUFF AND REMOVED NO_STUFF FROM R153
19) UPDATE DIFF_NET_SPACING_TYPE PROPERTY ON POWER_SUPPLY_SENSE AND THERMAL DIODE DIFF PAIRS
20) CHANGED FIREWIRE OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

2/10/04

22) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
23) CHANGED R657 TO STUFFED AND R153 TO NO STUFF
24) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW

** RELEASED FOR DVT **

3/24/04

25) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS

3/29/04

26) ADDED ALTERNATE FOR Q41A REV 1.1.1 CPU (U43)
27) ADDED ALTERNATES FOR 128MB AND 64MB A16 M1T'S
28) CHANGED TMDS SERIES RPAKS TO 0 OHMS (RPS7,RP27,RP32,RP28)
29) ADDED ALTERNATE FOR ALS OP-AMP (U40)

** RELEASED TO REV A **

30) CHANGED TMDS TERMINATION R,C AND LS TO PRODUCTION VALUES

** RELEASED TO REV A UNDER NEW PART NUMBER **

7/6/05

ADDED 338S0223 (88E1111 REV. B1) AS AN ALTERNATE OF 338S0079

8/22/05

REPLACED 740S0006 EITH 740S0018 (FUSE,1.5A,24V,SMD,LF)
ADDED 128S0022 (220 UF) AS AN ALTERNATE OF 128S0034 (330 UF) FOR MPU VCORE CAPS
ADDED LABELS WITH EEE

** RELEASED TO 051-6654-C **

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 40 OF 44	

8 7 6 5 4 3 2 1

D

*** Signal Cross-Reference for the entire design ***

+1_8V_MARVELL 27D2< 38B3>
+1_5V_AGP 12C5< 12D1< 12D4< 15D5< 16C8< 18C6< 18D6< 19A8< 19B4<> 19D5<> 21B8< 21D6< 38C3>
+1_5V_AGP_GPU 21C5< 38C3>
+1_5V_AGP_NECK 19B4<> 38B3>
+1_5V_GPU_VDD15 19D3< 38C3>
+1_5V_INTREPID_PLL 8D6< 12D4< 12D8< 14D6<> 38D3>
+1_5V_INTREPID_PLL1 14C3< 38D3>
+1_5V_INTREPID_PLL2 14D3< 38D3>
+1_5V_INTREPID_PLL3 14D3< 38D3>
+1_5V_INTREPID_PLL4 14D3< 38D3>
+1_5V_INTREPID_PLL5 12D3< 38D3>
+1_5V_INTREPID_PLL6 12D6< 38D3>
+1_5V_INTREPID_PLL7 8D5< 38D3>
+1_5V_INTREPID_PLL8 14D3< 38D3>
+1_5V_LDO 35D8< 38D6>
+1_5V_MAIN 38D6>
+1_5V_SLEEP 38D6>
+1_5V_SLEEP_NECK 21A3<> 38B3>
+1_5V_SLEEP_VIN 35D8<> 38D6>
+1_8V_ATI_PVDD 19C5<> 21B6< 21B6< 21D6<> 38C3>
+1_8V_ATI_TPVDD 21D2<>
+1_8V_DVO_F 21B2<
+1_8V_GPU 18A7< 19D8< 20A5< 21A2< 21A6< 21B1< 21B6< 21C8< 21D6< 21D8< 38C3>
+1_8V_GPU_AVDD 21D5< 38C3>
+1_8V_GPU_AVDDQ 21D4< 21D7< 38C3>
+1_8V_GPU_MEMPLL 21B5< 38C3>
+1_8V_GPU_PLL 21D5< 38C3>
+1_8V_GPU_PNLIO 21A5< 38C3>
+1_8V_GPU_PNLPLL 21B5< 38C3>
+1_8V_GPU_TP_PLL 21B4< 21D1<
+1_8V_GPU_VDDDI 21C7< 21D4< 38C3>
+1_8V_MAIN 38B6< 39A2>
+1_8V_PVDD_NECK 19B5<> 38B3>
+1_8V_SLEEP 38D6>
+1_8V_SLEEP_NECK 21A3<> 38B3>
+1_95V_FW_DVDD 28C4< 28C7<> 28D5< 38A3>
+1_95V_FW_DVDD_PORT1 28D6< 38A3>
+1_95V_FW_DVDD_RX0 28C5< 38A3>
+1_95V_FW_DVDD_TX0 28C5< 38A3>
+1_95V_FW_PLL400VDD 28D5< 38A3>
+1_95V_FW_PLL500VDD 28D5< 38A3>
+1_95V_FW_PLLVDD 28D5< 28D7<> 38A3>
+2_5V_CG_MAIN 14C8< 38A3>
+2_5V_GPU 21A8< 21B6< 21D3< 21D7< 21D8< 38B3>
+2_5V_GPU_A2VDD 21D4< 21D7< 38C3>
+2_5V_GPU_PNLIO 21A5< 38C3>
+2_5V_INTREPID 9A8< 10D3< 10D5< 10D6< 10D8< 15D7< 16B8< 38C3>
+2_5V_MAIN 38D6>
+2_5V_MARVELL 27B8< 27C4<> 38B3>
+2_5V_MARVELL_AVDD 27C4< 38B3>
+2_5V_SLEEP 38D6>
+2_5V_SLEEP_NECK1 19C4<> 38B3>
+2_5V_SLEEP_NECK2 21A3<> 38B3>
+2_8V_GPU_LVDS_LDO 21A6<>
+3V_ATI_OSC_SLEEP 18D2< 38C3>
+3V_ATI_SS 18B2< 38C3>
+3V_CG_PLL_MAIN 14C6< 38A3>
+3V_FW 28A3< 28D7<> 29D5< 38A3>
+3V_FW_AVDD 28C6< 38A3>
+3V_FW_AVDD_PORT0 28C6< 38A3>
+3V_FW_AVDD_PORT1 28C6< 38A3>
+3V_FW_AVDD_PORT2 28D6< 38A3>
+3V_FW_ESD 29B3<> 29D2<> 38B3>
+3V_FW_ESD_ILIM 29D4< 38B3>
+3V_FW_LP 28D7<> 38A3>
+3V_GPU 12D1< 18B8< 18C5< 18C7< 18D6< 19C4< 19C6< 19C7< 19D7< 21A7< 21B1< 21B8< 38C3>
+3V_GPU_FLT 21B2< 38C3>
+3V_GPU_SI 20C4< 20C6< 20D8<
+3V_HALL_EFFECT 23C6<> 38B6> 39C4>
+3V_INTREPID_USB 14C3< 38D3>
+3V_LCD 22B4<> 38B6>
+3V_LCD_SW 22A4<> 38B6>
+3V_MAIN 38D6>
+3V_NEC_VDD 26D7< 26D7< 38A3>
+3V_PMU 38D6> 39A2>
+3V_PMU_AVCC 25A4< 30B6< 30D5<> 38C6>
+3V_PMU_ESR 32A2< 38C6>
+3V_PMU_REG 30B7< 34A3<> 38C6>
+3V_SI_AVCC 20C7< 38B3>
+3V_SI_PLLVCC 20C7< 38B3>
+3V_SI_VCC 20C6< 38B3>
+3V_SLEEP 38D6>
+3V_SLEEP_NECK 21A3<> 38B3>
+3V_SLP_DK_L 33B4<>
+3V_SLP_ON 33A5<>
+4_6V_BU 32A3<> 33B7< 38C6>
+4_6V_ESR 32A4< 38C6>
+4_6V_RAW 30B4< 32A4<> 38C6>
+5V_DDC_SLEEP 22D3<> 22D5<> 38B6> 39A2>
+5V_DDC_SLEEP_UF 22D6< 38B6>
+5V_HD_SLEEP 24D1<> 33A7<> 38C6>
+5V_INV_SW 22B1<> 38B6> 39D1>
+5V_INV_UF_SW 22B2<> 38B6>
+5V_MAIN 38D6>
+5V_SLEEP 38D6>
+5V_SOUND_SLEEP 38B6>
+5V_TPAD_SLEEP 23C7<> 38B6> 39C4>
+12_8V_INV 22B1< 38B6> 39A2>
+24V_PBUS 38D6> 39B2>
+ADAPTER 31D8<> 32B7< 38C6>
+ADAPTER_ILIM 32B6<> 38C6>
+ADAPTER_OR_BATT 32A5<> 38C6>
+ADAPTER_SENSE 31D5<> 38C6>
+ADAPTER_SW 31D6<> 38C6>
+BATT 38D6>
+BATT_14V_FUSE 31D1<> 38C6>
+BATT_24V_FUSE 31B1< 31D2<> 38C6>
+BATT_POS 31A4<> 38C6> 39C3>
+BATT_RSNS 31B2< 38C6>
+BATT_VSNS 31A4< 38C6>
+FW_FUSE 29D7<> 38A3>
+FW_PWR_OR 28B8< 28D8<> 29D5<> 38A3>
+FW_PWR_PORTA 29C5< 38A3>
+FW_SW 29D5<> 38A3>
+FW_VP0 29C2<> 38A3>
+FW_VP1 29A3<> 38A3>
+GPU_MCLK 21C7< 21D4< 38C3>
+GPU_MEM 18A6<> 18B8< 21B4< 21B7< 21C6< 21C8< 21D2< 38C3>
+GPU_MEMCORE 21C5< 38C3>
+GPU_VDD15_NECK 19B5<> 38B3>
+GPU_VDD15_UF 19B5<> 19D4<> 38C3>
+HD_LOGIC_SLEEP 24C2<> 38C6>
+PBUS 38D6> 39B2>
+VCC_CBUS_SW 17B1<> 17B2<> 17D2<> 38D3>
+VPP_CBUS_SW 17B1<> 17B2<> 17D2<> 38C3>
1V20_REF 31C7< 32C8< 38D1>
1V65_REF 31A5<
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1_5V_DL 35B5<> 38C1>
1_5V_FB 35B5< 35B7< 38C1>
1_5V_ILIM 35C5<> 38C1>
1_5V_LX 35B5<> 38C1>
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1_5V_SLEEP_PWREN_L 35A3<>
1_8V_SW 35A5<> 38A1>
1_8V_VFB 38A1>
2_5V_BOOST 35C4<> 38D1>
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2_5V_DH 35C4<> 38D1>
2_5V_DL 35B4<> 38D1>
2_5V_ILIM 35C5<> 38C1>
2_5V_LX 35B4<> 38D1>
2_5V_SLEEP_PWREN_L 35C2<>
2_34V_REF 30A4<>
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3V_5V_OK_INV 35A8<>
3V_BG 33C4<>
3V_BOOST 33C4<>
3V_BOOST_ESR 33D3<>
3V_ITH 33C4<>
3V_ITH_RC 33C3<
3V_PMU_VTAP 32B3<
3V_RUNSS 33D2< 38D1>
3V_RUNSS 33C4<
3V_SLEEP_PWREN_L 33A3<>

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3V_SNSP 33C4< 37A2>
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3707_SGND 33B5<> 38D1>
3707_STBY 33C5<
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A29_CURRENT_ADJ 31C4<>
A29_DETECT 30A2<> 31A5<> 31C4<>
A29_DET_L 30A3<
AB_SEL_LOW 34A6<>
AC_DIV 31C6<
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AC_ENABLE_L 31C6<>
AC_GTR_18V 31C4<
AC_IN 27B8<> 29C7<> 30B3< 31C5<> 31C7<>
AC_IN_FW_CNTL 29C7<>
AC_IN_L 31C2<> 31C6<>
AC_IN_L_RC 31C2<>
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ADT7460_FAN1_PWM 25B3<>
ADT7460_FAN2_PWM 25B3<>
ADT7460_THERM 25A5<> 25B3<>
ADT7460_VCC 25C4<
ADT7460_VCORE_MON 5C8<> 25B4<>
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AGP_ATI_VREF 18B7<
AGP_ATI_VREFG 18B7<
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AGP_CBE<0> 12B2<> 18B7<>
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AGP_CBE<2> 12B2<> 18B7<>
AGP_CBE<3..2> 37D5>
AGP_CBE<3> 12B2<> 18C7<>
AGP_DEVSEL_L 12B2<> 12C2< 18B7<> 37D5>
AGP_FRAME_L 12B2<> 12C2< 18B7<> 37D5>
AGP_GNT_L 12C2<> 12D2< 18B7< 37D5>
AGP_INT_L 14B5<> 18B7<>
AGP_IRDY_L 12B2<> 12C2< 18B7<> 37D5>
AGP_PAR 12B2<> 18B7<> 37D5>
AGP_PIPE_L 12A2<> 12B2<
AGP_RBF_L 12A2<> 12C2< 18C6<> 37D5>
AGP_REQ_L 12C2< 12D2<> 18B7<> 37D5>
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AGP_STP_L 18C6<
AGP_SUS_STAT_L_PU 18C6<
AGP_TRDY_L 12B2<> 12C2< 18B7<> 37D5>
AGP_WBF_L 12A4<> 12B2< 18B7<
AIRPORT_CLKRUN_L 24C6<> 39C1>
AIRPORT_IDSEL 24C5<> 39B1>
AIRPORT_PCI_GNT_L 12D7<> 24D5<> 39C4>
AIRPORT_PCI_INT_L 14B5<> 14D7< 24D5<> 39C4>
AIRPORT_PCI_REQ_L 12A7< 12D7<> 24D6<> 39D4>
AIRPORT_PME_L_TP 24D5<>
AMP_CONTROL 25C5<> 25D5<>
ATI_AGP_FBSKEW<0> 19C2< 19C7<>
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ATI_CLK27M_OSC 18D2<
ATI_CLK27M_OSC_SS 18B2< 18D1<
ATI_DBI_HI_PU 18C6<
ATI_DBI_LO_PU 18C6<
ATI_GPIO7_SPN 19C7<>
ATI_GPIO8_PD 19C7<>
ATI_GPIO9_SPN 19C7<>
ATI_GPIO10_SPN 19C7<>
ATI_GPIO12_SPN 19C7<>
ATI_GPIO13_SPN 19C7<>
ATI_HSYNC 19D5<> 22C8<
ATI_MEMRST 18A6<>
ATI_MEMVMODE0 18A7<
ATI_MEMVMODE1 18A7<
ATI_OSC_OE 18D3<
ATI_PVDD_BYP 21D6<>
ATI_R2SET 19D6<
ATI_RSET 19D6<
ATI_SSCLK_IN 18D1< 19B7<
ATI_SSCLK_UF 18D2<
ATI_TESTEN 19B7<
ATI_TMDS_CLKN 19B7<> 20B4<
ATI_TMDS_CLKP 19B7<> 20B4<
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ATI_TMDS_DP<1> 19B7<> 20B4<
ATI_TMDS_DP<2> 19B7<> 20B4<
ATI_TPVDD_BYP 21D1<>
ATI_VSYNC 19D5<> 22C8<
ATI_XICLK_SKEW<0> 19C2< 19C7<>
ATI_XICLK_SKEW<1> 19B2< 19C7<>
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BATTV_LOW 31B8<>
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BATT_14V_GATE 31C1<>
BATT_24PBUS_EN 31C2<>
BATT_24V_GATE 31C1<>
BATT_CLK 31A4<> 39C3>
BATT_DATA 31A4<> 39C3>
BATT_DIV 31A5<
BATT_LOW 31A6<>
BATT_LOW_L 31B6<>
BATT_NEG 31A4<> 38C6> 39C3>
BBANG_HRESET_L 23A4<> 23C4<> 38C3>
BBANG_JTAG_TCK 23B3< 23C4<>
BBANG_TCK_EN 23B3<
BCKFD_PROT_EN_L 31C6<>
BCKFD_PROT_GATE 31D6<>
BRIGHT_PWM 22A1<> 39A7>
BRIGHT_PWM_UF 22A2<
BT_USB_DM 14B1< 24B2<> 37B2<> 39B6>
BT_USB_DP 14C1< 24B2<> 37B2<> 39B6>
CAPSLOCK_LED 23A8<
CAPSLOCK_LED_L 23B8< 30C7<
CBUS_ADDR<0> 17B1<> 17B4<
CBUS_ADDR<1> 17B1<> 17B4<
CBUS_ADDR<2> 17B1<> 17B4<
CBUS_ADDR<3> 17B1<> 17B4<
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CG_FSEL 14B7< 14C5<
CG_LOCK 14B7<
CG_RESET_L 14B7<

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CHARGE_LED_L 30C6<> 30D7< 31D8<> 39D2>
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CHGND2 38A6>
CHGND3 38A6>
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CHGND5 38A6>
CHGND6 38A6>
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CLK10M_PMU_XOUT 30B6<
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CLK18M_INT_XIN 14A5< 36B1>
CLK18M_INT_XOUT 14A5<> 36B1>
CLK25M_INT_EXT 14A4<> 36B1>
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CLK25M_XTAL_XIN 27A7< 36B1>
CLK25M_XTAL_XOUT 27A7<> 36B1>
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CLK27M_GPU_XOUT 36B1>
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CLK33M_AIRPORT_UF 12C7<> 36C1>
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CLK33M_CBUS_UF 12C7<> 36C1>
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CLK33M_USB2_UF 12C7<> 36C1>
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CLK66M_GPU_AGP_UF 12C7<> 36C1>
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CLKENET_LINK_GTX 13C5<> 36A1>
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CLKENET_PHY_TX 27D7<> 36B1>
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CLKLVDS_LP 19B5> 22A4<> 37C2> 39B7>
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COMM_GPIO_L 14C2<> 25D2<> 39C2>
COMM_RESET_L 14C5<> 25C4<> 39C4>
COMM_RING_DET_L 14B5<> 14C7< 25C3<> 30C6<> 39C4>
COMM_RTS_L 14C2< 25D1<> 39B2>
COMM_RXD 14C2< 25D1<> 39B2>
COMM_SHUTDOWN 14C5<> 25C4<> 39C4>
COMM_TRXC 14C2<> 25D2<> 39C2>
COMM_TXD_L 14C2<> 25D1<> 39C2>
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CPU_PLL_FS01 7C4<
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CPU_TBST_L 5A7< 8B6<> 36D5>
CPU_TEA_L 5B4< 8A4<> 8C2< 36D5>
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CPU_VCORE_PWR_SEQ 34D8<>
CPU_VCORE_SEQ 34D8<
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CPU_VCORE_SLEEP 5C3< 5D8<> 6C6<> 34C1< 34D2< 39D3>
CPU_VCORE_SLEEP_F 34C2<>
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CPU_WT_L 5A7< 8B6<> 36C5>
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CSLOT_IOWR_L_SPN 13C7<
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DCDC_EN_L 33B6< 33B7<> 35C7<>
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DDR_VREF 11D1< 11D3<> 11D5<> 11D6<> 11D8<> 38D3>
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DVI_DDC_CLK_UF 22C5<> 22D3<> 39C7>
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DVI_DDC_DATA_UF 22C5<> 39C7>
DVI_HPD 22C4<>
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DVI_TURN_ON_ILIM 22D2<>
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EIDE_OPTICAL_CS1_L 24A5<> 24B7< 37B5> 39D4>
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HD_DIOW_L 24A3< 24C1<> 37B5>
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HD_DMARQ 13C6< 24C2<> 37B5>
HD_INTRQ 13C6< 24C1<> 37B5>
HD_IOCHRDY 24A3< 24C1<> 37B5>
HD_RESET_L 24A3< 24D2<> 37B5>
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HPD_DIV 22C1<
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KBD_CONTROL_L 23A5< 23A7<> 30A8< 30C6<> 39B4>
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LTC3411_ITH 38A1>
LTC3411_ITH_RC 38A1>
LTC3411_SHDN 38A1>
LTC3411_SYNC 38A1>
LTC3411_VCC 38B1>
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MLB_ALS_OP_IN 23D7<
MLB_ALS_OUT 23C4<> 23D6<
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NEC_RIGHT_USB_PWREN 26B5<> 32A7<> 39C1>
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NEC_USB_DBP 26B4< 26C3<> 37B2>
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NEC_USB_RSDM2 26C5<> 37B2>
NEC_USB_RSDP1 26C5<> 37B2>
NEC_USB_RSDP2 26C5<> 37B2>
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PMU_AC_IN        30B4<>
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PMU_CHARGE_V     30C4<> 31B8<>
PMU_CHRG_BATT_B  30C4<> 31A8<>
PMU_CLK          14C2<> 30C4<>
PMU_CNVSS        30B6< 30C7<>
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PMU_EPM          30D2< 30D4<>
PMU_FROM_INT     14C2<> 30C4<>
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PMU_RESET_BUTTON_L  25B1< 30C4<> 30D2<
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RAM_MUXSEL_L     10A3< 10A5< 10B5> 10B7<> 36A5>
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RAM_WE_L         9A4< 11B3<> 11B8<> 36A5>
RF_DISABLE_L_SPN  24B6<> 39C1>
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RIGHT_USB_DP     26A3< 32A7<> 37A2> 39D1>
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ROM_OE_L         9B3< 12A5< 24C5<> 39B1>
ROM_ONBOARD_CS_L  9B3< 24C6<> 39B1>
ROM_RW_L         9B3< 12A5< 24C6<> 39B1>
ROM_WP_L         9B3<
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RSDM5_TP         26C5>
RSDP3_TP         26C5>
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SND_CLKOUT_F     25C7<> 25D7<
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SND_HW_RESET_L   14A7< 14B5<> 25C8< 39C6>
SND_HW_RESET_L_F  25C6> 25C7<
SND_LIN_SENSE_L  14B5<> 25D6<> 39C6>
SND_SCLK         14B1< 25C6< 36B1> 39C6>
SND_SCLK_F       25C7< 25D7<>
SND_SYNC         14B1< 25D8< 39D6>
SND_SYNC_F       25C7<> 25D7<
SND_TO_AUDIO     14B1< 25D8< 39D6>
SND_TO_AUDIO_F   25D6<> 25D7<
SOFT_PWR_ON_L    22D1< 23A8< 30A8< 30C6<> 30D7<
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SRCLK_TP         26A5> 39A4>
SRMOD_TP         26A5< 39A4>
ST7_ICP_SEL_PD   23A2< 23D6<
ST7_KBD_LED_OUT  23A4< 23C4<>
ST7_OSC1         23D5<
ST7_OSC2         23D5<>
ST7_PB6_PD       23B2< 23C4<>
ST7_RESET_L      23D5<>
ST7_SENSOR4_SCK_PD  23B2< 23D4<>
ST7_SENSOR4_SDA_PD  23B2< 23D4<>
ST7_SENSORS_SCK_PU  23B2< 23D4<>
ST7_SENSORS_SDA_PU  23B2< 23D4<>
ST7_SLEEP_LED_H  23C2<> 23C4<>
ST7_XTAL_IN      23C5<
STOP_AGP_L       12D2< 12D4<>
SUPPLY_M_DM      25B6< 25B8<
SUPPLY_M_DP      25B6< 25B8<
SUTRO_ALS_GAIN_SW  23C4<> 24B2<> 39C2>
SUTRO_ALS_OUT    23C4<> 24B2<> 39C2>
SYSCLK_CPU       5C4< 8A6< 36D1>
SYSCLK_CPU_UF    8A6<> 36D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 36D1>
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SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 36D1>
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SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 36C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 36D1>
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SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 36D1>
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THERM1_A_DP      25A6< 25A8< 37A2>
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THERM1_DP        25A5< 25A5< 25B5<> 25B5< 37A2>
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THERM1_M_DP      37A2>
THERM2_A_DM      25A6< 25A8< 37A2>
THERM2_A_DP      25A6< 25A8< 37A2>
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THERM2_M_DP      37A2>
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THERM_L_OC       25A4<> 30B4<>
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TMDS_CLKP        20B3< 20C2< 20C3< 22C7<> 37B2>
TMDS_CLK_CMF     20C1<
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TMDS_CONN_CLKP   22C6<> 22C7<> 37B2> 39D7>
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TMDS_CONN_DN<2>  22B6<> 22D5<>
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TPAD_F_TXD       23A7<> 39C4>
TPAD_RXD         23A8< 30C2< 30C4<>
TPAD_TXD         23A8< 30B2< 30C4<>
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TV_GND2          22A6<> 38B6> 39A7>
TV_Y             22A6<> 39D6>
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UIDE_DMACK_L     13C7<> 24A4< 37C5>
UIDE_DMARQ       13C7<> 37C5>
UIDE_INTRQ       13C7< 37C5>
UIDE_IOCHRDY     13C7< 24A4< 37C5>
UIDE_REF         13C7<> 38D3>
UIDE_RST_L       13C7<> 24A4< 37C5>
USB2_PCI_CNT_L   12C7<> 26B7<
USB2_PCI_INT_L   14B5<> 14C7< 26A8<
USB2_PCI_REQ_L   12A7< 12D7<> 26B7>
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USB_D2P          14D1< 26A4< 26A5>
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USB_DDP          14B2<> 14C2<
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USB_DEP          14B2<> 14C2< 37B2>
USB_DFM          14B2<> 14B2< 37B2>
USB_DFP          14B2<> 14B2< 37B2>
USB_OC_AB_L      14B2< 14C7<
USB_OC_CD_L      14B2< 14C7<
USB_OC_EF_L      14B2< 14D7<
USB_PWREN_AB_L   14B2<> 14C7<
USB_PWREN_CD_L   14B2<> 14C7<
USB_PWREN_EF_L   14B2<> 14D7<
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VCORE_BST        34C5<> 38C1>
VCORE_CC         34B6<> 38B1>
VCORE_CNTL_RC    19A3<>
VCORE_DH         34B5<> 38C1>
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VCORE_FB         34B5< 38B1> 39A2>
VCORE_GND        34B5<> 38B1>
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VCORE_GNDDIV     34A4< 34B5< 38B1>
VCORE_GNDDIV_TEST  34A3<>
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VCORE_ILIM       34C6<> 38C1>
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VCORE_MUX_EN     34D5<> 39A2>
VCORE_MUX_SEL    34D5<>
VCORE_REF        34B6<> 38C1>
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VCORE_TIME       34B4<> 38B1>
VCORE_TON        34B6< 38C1>
VCORE_VCC        34C6< 38C1>
VCORE_VGATE      148S< 148T< 34B4> 38B1>
VCORE_VID0       39A3>
VCORE_VID1       39A3>
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VCORE_VID4       39A3>
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VCORE_VID<4>     34A2<> 34B8< 34D4<>
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VGA_G            22C5<> 22D7< 39D7>
VGA_HSYNC        22C6<> 22C7< 39D7>
VGA_HSYNC_BUF    22C8<>
VGA_R            22C5<> 22D7< 39D7>
VGA_VSYNC        22C5<> 22C7< 39D7>
VGA_VSYNC_BUF    22C8<>
ZV_LCDDATA20_PU  19C7<>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 42 OF 44	

*** Part Cross-Reference for the entire design ***

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RP42	RPAK10P2C	23
RP43	RPAK10P2C	23
RP44	RPAK4P	25
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SP4	SPKR_CLIP_P84	4
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SP6	SPKR_CLIP_P84	4
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U4	SN74AUC1G08	23
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U6	FAN2558	5
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U16	LTC1778	19
U17	FEPR_1MX8	9
U18	LTC1625	32
U19	PWR_CNTRL_TPS2211	17
U20	MAX1717	34
U21	COMPARATOR_LMC7211	32
U22	MAX1715	35
U23	AMP_MAX4172	31
U24	7432	22 30
U25	VREG_LP2951	32
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Y5	CRYSTAL	26
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ZT82	HOLE_VIA	4
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